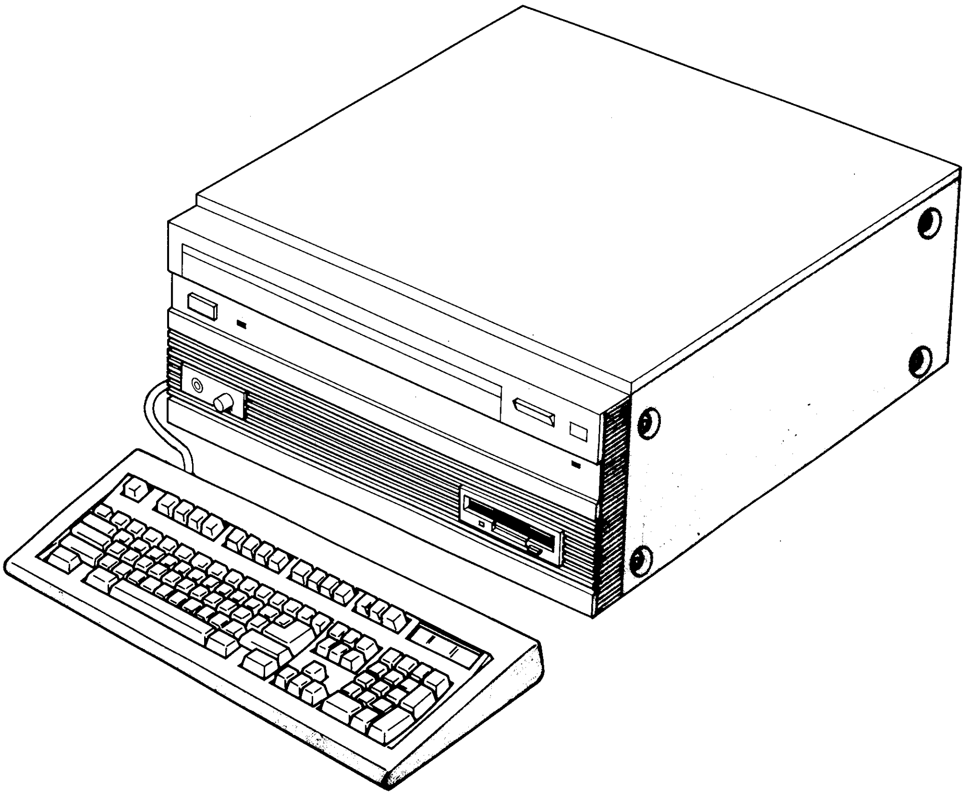
VIW-5000

SERVICE MANUAL

Internal Hard Disk Drive Unit
SCK-5015
Memory Expansion
SMI-5050
Graphics Memory Expansion
SMI-5051



Sony VIEW System

SONY®

使用時は添付資料も参照のこと
Refer to the additional documents

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CHAPTER 1
OPERATION

1-1. SYSTEM OUTLINE

1-1-1. Outline

The Sony VIW-5000 VIEW (Visual Information Enhanced Workstation) system is a computer-controlled video information system. It consists of a computer and a videodisc player with graphics and superimpose boards installed in a single unit, and a separate keyboard.
The Sony SMW-5001 VIEW/VGA Operating System Package is available for setting up and for the operating system of the VIW-5000.

16-bit microprocessor as the center of the system
Because the computer employs the 10MHz 80286 CPU, high-speed data transfer and quick data processing are possible.

Storage devices
This system employs a 3.5-inch micro folppydisk (1.44M bytes when formatted) for storage of the operating system program and application software. It provides a drive slot for installing an optional hard disk drive as a storage device.

System expansion
The system provides 2 slots on the mother board to install a Memory Expansion and a Graphics Memory Expansion. Besides, the system also provides 2 IBM PC/AT compatible bus slots to accommodate various commercially available optional boards for system expansion.

Control of the videodisc player
The videodisc player is controlled by the computer. Control codes from the computer allow various operations such as playback in various speeds, repeat, pause, or search. The Sony SMW-5001 VIEW/VGA Operating System Package includes programs to control the videodisc player.

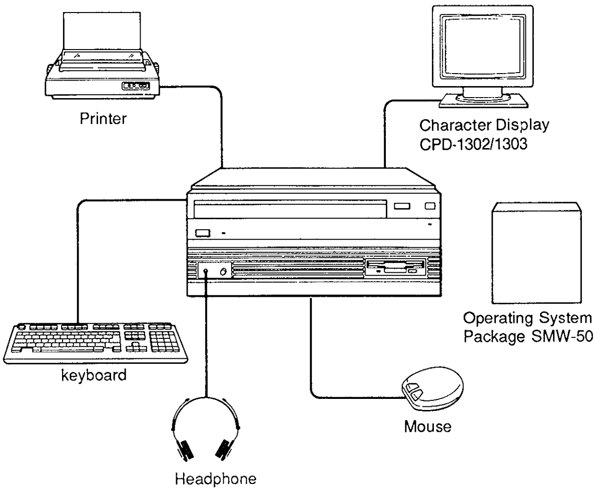
Software compatibility
Using the internal high scan superimposer board, the system supports all color display modes that are employed in IBM Personal System/2's graphics. You can use commercially available graphics software, courseware or authoring system for the IBM Personal System/2 on this the VIEW system.

High quality superimposed picture
Because the digital scan converter doubles the horizontal frequency, the high quality flickerless graphics display is obtained in all color display modes.
By installing an optional Graphics Memory Expansion to this the VIEW system, the Expanded color display modes (640 × 480 dots, 256 colors) is also available for more precise graphics display.
The internal superimposer board also allows the VGA color graphics or images reproduced by the videodisc player.

Line out and headphones jacks
For monitoring the audio when a display without speakers is connected, the system is equipped with line out and headphones jacks.

1-1-2. System Configuration

The typical configuration for the VIEW system is as shown below.
For the operating system, you need the Sony SMW-5001 VIEW/VGA Operating System Package.



1-1-3. System Expansion

The following optional peripheral devices are available for expanding the VIEW system.

1-1-3-1. Internal options

Internal Hard Disk Drive Unit SCK-5015
This unit can be mounted inside the computer. It provides additional storage capacity (40M bytes) and allows a higher rate of data access (access time: 29m sec). Refer to Chapter 10 "EXPLANATION OF SCK-5015."

Dual RS-232C Board SMI-3031
This unit provides two additional RS-232C ports, which operate in the asynchronous mode.

Memory Expansion SMI-5050
This card supplies an Expanded Memory (EMS) or Extended Memory whose capacity is 2M bytes (two cards). Refer to Chapter 11 "EXPLANATION OF SMI-5050."

Graphics Memory Expansion SMI-5051
This board enables the Expanded color display mode (640 × 480 dots, 256 colors). Refer to Chapter 12 "EXPLANATION OF SMI-5051."

1-1-3-2. External options

Mouse SMI-3062
For quick and easy control of a cursor.

Trinitron character display CPD-1302/1303
For display of the information from the computer and the videodisc player.

Printer for IBM PCs
For program listing and printing out of processing results.

1-1-3-3. Cables

RS-232C cable SMF-3031
For connection between the Dual RS-232C board and various devices (to Modem).

Null modem cable SMF-3036C
For connection between the RS-232C port and various devices (to Terminal).

Monitor cable CTG-PSII
For connection between the VIEW system and the character display.

Printer cable SMF-2120
For connection between the VIEW system and the printer.

1-2. BEFORE OPERATION

1-2-1. Precautions

1-2-1-1. On safety

- The unit operates on 120V AC, 60Hz.
- Should any solid object or liquid fall into the cabinet, unplug the unit and have it checked by the qualified personnel before operating it any further.
- Unplug the unit from the wall outlet if it will not be used for an extended period of time.
- To disconnect the cord, pull it out by the plug. Never pull the cord itself.

1-2-1-2. On installation

- The unit consists of high-precision electronic parts. Do not drop it or bump it against other object. Do not place it in a location subject to vibration or on an unstable base.
- Do not install the unit near a heat sources such as a radiator or an air duct, or in a place subject to direct sunlight, excessive dust, and/or moisture.
- Do not place the unit near electronic equipment as it may malfunction if affected by an electromagnetic field. The internal folppydisk unit is especially sensitive because it uses weak magnetic signals ; never place electronic equipment, such as a TV set, near it.
- Provide adequate air circulation to prevent internal hear build-up. Do not place the unit on surfaces (rugs, blankets) or near materials (curtains, draperies) that may block the ventilation slots.
- Use only the specified peripheral equipment ; otherwise, trouble may result. Before connecting peripheral equipment, be sure to turn the power off or the internal IC chip may be damaged.

1-2-1-3. On moisture condensation

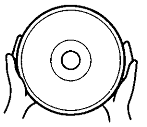
Do not operate the unit right after having transported it from a cold location to a warm location or in a room where the temperature rises suddenly, because moisture may condense in the operating sections of the unit. Wait for about an hour before turning the power on in the new location or keep the rise in room temperature gradual. If the unit is operate with moisture condensation, the unit and the disc may be damaged. Therefore, remove the disc immediately when there is a possibility of moisture condensation and no picture is obtained. To evaporate the moisture rapidly, leave the player turned on without a disc loaded.

1-2-1-4. On cleaning

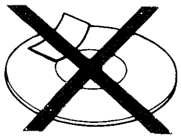
Clean the cabinet and keyboard with a soft, dry cloth, or a soft cloth lightly moistened with a mild detergent solution. Do not use any type of solvent, such as alcohol or benzine, which might damage the finish.

1-2-1-5. On handling videodiscs

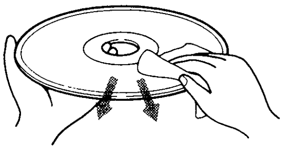
- Handling the disc by its edge, and to keep the disc clean, do not touch the rainbow colored surface.



- Do not stick paper or tape on the disc surface.



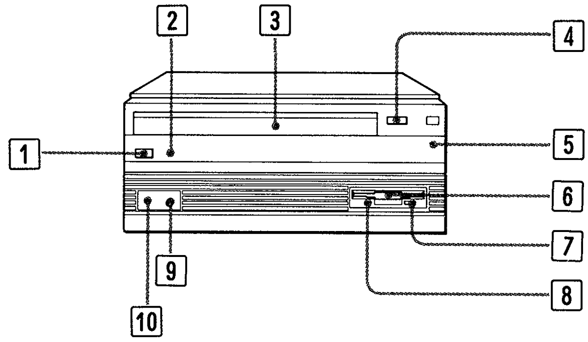
- Do not expose the disc to direct sunlight or heat sources such as hot air ducts, or leave it in a parked car in direct sunlight where a considerable rise in the temperature may occur.
- Before playing, clean the disc with the cleaning cloth. Wipe the disc from the center out.



- Do not use solvents (such as benzine or thinner) or commercially available cleaners or anti-static sprays intended for analog record discs.
- After playing, remove the disc and store it in its case.

1-2-2. Location and Function of Parts and Controls

1-2-2-1. Front panel



1 Power switch
Press this switch to turn on the unit. To stand by, press the switch again. This switch is active only when the **MAIN POWER** switch on the rear panel is on.

Note
Do not turn the switch on and off at intervals less than 5 seconds.

2 Power ON indicator
While the power of the unit is on, this indicator lights.

3 Videodisc compartment

4 OPEN/CLOSE button
Press to open the videodisc compartment, and press again to close it.
The compartment will also close automatically when it is pushed lightly. Be sure to push the center of the compartment for proper operation of the player.

5 DISC indicator
Blinks while loading or unloading a videodisc, or lights up when the videodisc is being played back within the player.

6 Micro folppydisk drive
Built-in drive for a 3.5-inch micro folppydisk.

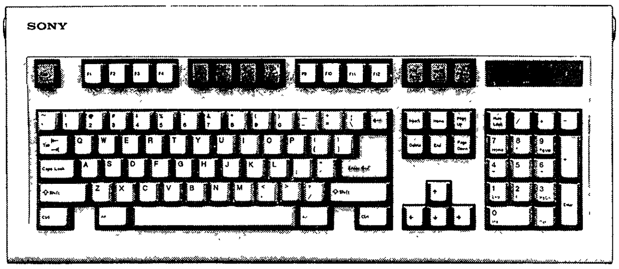
7 Eject button
Press this button to remove a folppydisk.

8 In-use indicator
When a micro folppydisk drive reads or writes data, this indicator lights. Do not press the eject button while this indicator is lit.

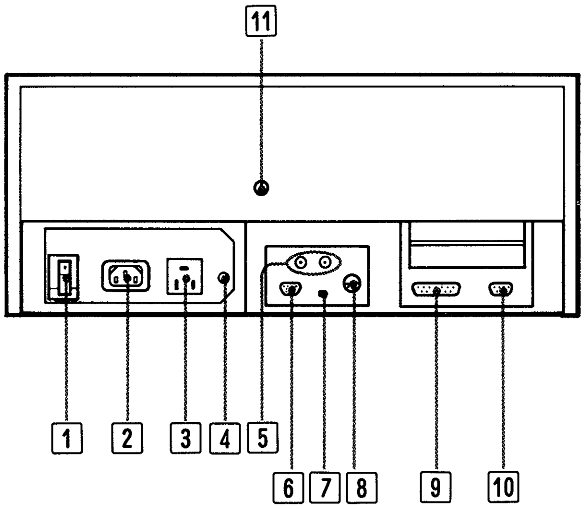
9 VOLUME control
Controls the volume of the computer sound from the built-in speaker and the computer and videodisc sound from the HEADPHONES jack.

10 HEADPHONES jack (mini jack)
Connect a headphone to this jack. The computer sound and the videodisc sound are mixed and output from this jack. The output sound is monaural.

1-2-2-2. Keyboard



1-2-2-3. Rear panel



1 MAIN POWER switch
the main switch to turn on and off the unit. When the unit will not be used for a long period of time, turn off this switch.

2 AC IN (inlet) connector
The supplied AC power cord, whose other end is connected to a wall outlet, is connected here.

3 AC OUT (outlet) connector
Connect equipment whose power consumption is no more than 3A. Power is supplied to the connected equipment only when the MAIN POWER switch on the rear panel and the power switch on the front panel of this unit are turned on.

4 Ground terminal
To reduce hum, ground the unit by connecting a ground wire to this terminal.

5 LINE OUT jacks (phone)
Connect active speakers (speakers with amplifier) to these jacks. The computer sound (monaural) and the videodisc sound (stereo) are output from these jacks.

6 MONITOR connector (analog RGB)
Connect a multiscan monitor such as Sony CPD-1302/1303.

7 HUE selection switch
Set this switch according to the monitor connected to the system. This switch adjusts the hue of the computer and videodisc pictures displayed on the monitor screen. (Default : right)

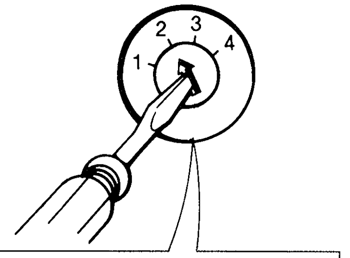
8 KEYBOARD jack (5-pin DIN)
Connect the supplied keyboard to this connector.

9 PRINTER connector (25-pin D-SUB)
Connect to a printer of the standard 8-bit parallel data transfer type (Centronics) for IBM PC.

10 RS-232C connector (9-pin D-SUB)
An asynchronous communication connector. Connect such a device as the SMI-3062 mouse or a modem. This port is accessed as "COM1".

11 BAUD RATE selector
Select the data transmission speed on the RS-232C line of the videodisc player part. The baud rate can be set to 9600, 4800, 2400, or 1200 baud. The initial setting at the factory is 9600.

Switch setting
1···1200 baud
2···2400 baud
3···4800 baud
4···9600 baud

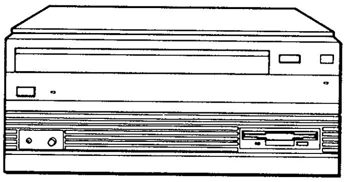


Set the arrow to point to the desired number using a tiny screw driver.

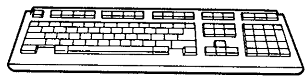
Be sure that the baud rate of the computer part (COM2) must be set to the same value as that of the videodisc player by software. Refer to the SMW-5001 VIEW/VGA Operating System Package's manual.

1-2-3. Contents of VIW-5000 Package

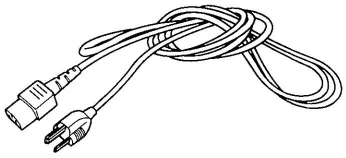
Main unit



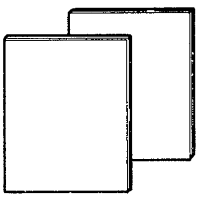
keyboard



AC power cord



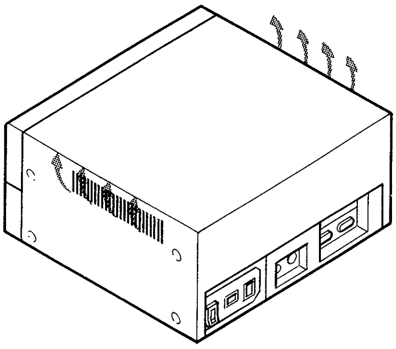
Operating instructions
Installation manual



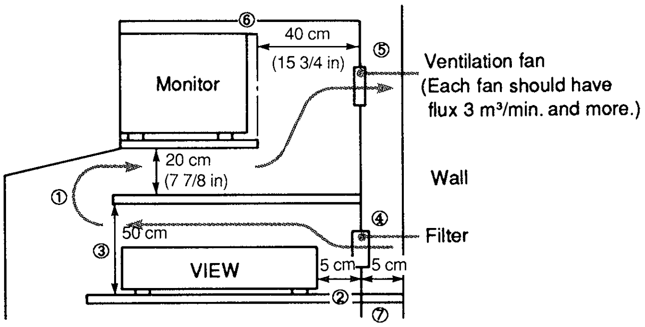
1-2-4. Note on Installing VIEW System in a Rack

When the VIEW system is installed in a rack, special consideration should be taken to prevent internal hear build-up.

1-2-4-1. Ventilation holes on the unit



1-2-4-2. Recommended ventilation when installed in a closed rack


⑥
40 cm
(15 3/4 in)
⑤
Ventilation fan
(Each fan should have
flux 3 m³/min. and more.)
Monitor
20 cm
(7 7/8 in)
①
Wall
④
Filter
50 cm
③
VIEW
5 cm
5 cm
②
⑦

① The air in the rack should be circulated from the bottom to the top as indicated above.
The temperature in the rack should not exceed 35℃ (95°F).

② Allow at least 5 cm (2 inches) between the rack the unit on both sides and at the back.

③ The distance between each shelf should be at least 50 cm (20 inches).

④ The holes located at the back of the rack should have filters to prevent dust from being drawn into the rack.

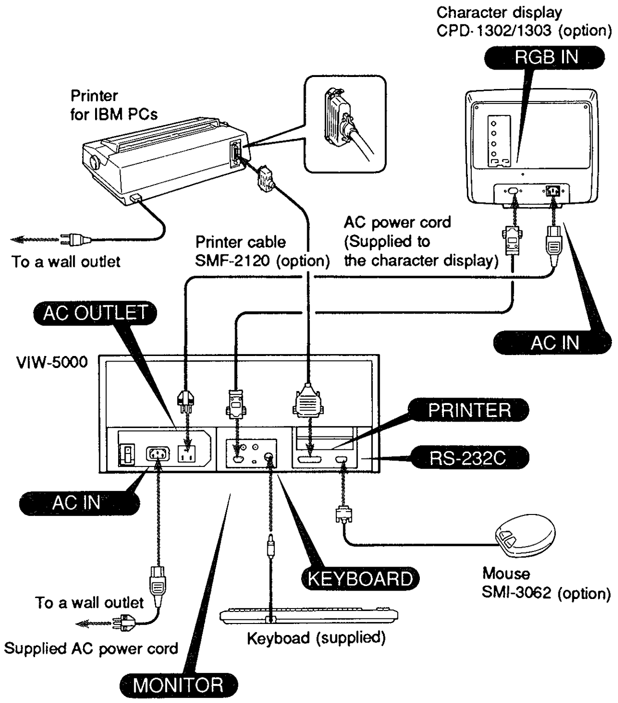
⑤ At least two ventilation fans should be used and should be installed in the back of the rack as indicated in the illustration.

⑥ If a monitor is installed in the same rack, care should be taken so that the heat from the monitor does not affect the VIEW system.

⑦ Allow at least 5 cm (2 inches) behind the rack when installing it against the wall.

1-2-5. Connecting External Options

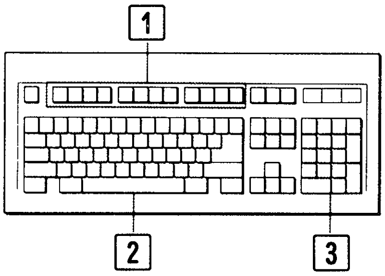
- Before connection, make sure that the power of the system is turned off.
- To assure the connection, insert the connectors firmly.


Character display
CPD-1302/1303 (option)
RGB IN
Printer
for IBM PCs
To a wall outlet
Printer cable
SMF-2120 (option)
AC power cord
(Supplied to
the character display)
AC OUTLET
AC IN
VIW-5000
PRINTER
RS-232C
AC IN
To a wall outlet
KEYBOARD
Mouse
SMI-3062 (option)
Supplied AC power cord
Keyboad (supplied)
MONITOR

1-3. BASIC OPERATION

1-3-1. Keyboard Operation

1-3-1-2. Keyboard arrangement



1 Alphanumeric keys
Alphanumeric keys are arranged in the standard (Q, W, E, R, T, Y) typewriter keyboard layout. The keyboard has character input keys (such as A to Z, 0 to 9, +, ?, <, >) which are displayed as they are entered, and control keys (such as Ctrl, Esc) which perform a certain task when they are pressed.

2 Numeric keys
These are numeric keys (0 to 9), arithmetic symbols (+, −, ∗, ∕) and ENTER key (↵). Numeric keys are arranged in the standard calculator layout.

3 Function keys
The keyboard has 12 function keys, from F1 to F12. The function of these keys are defined by the software. Therefore, their functions vary depending on the software used. Please refer to the respective software manual for details.

1-3-1-2. Key functions

This section describes the function of control keys defined by the BIOS of the computer. Other key functions vary depending on the MS-DOS and application programs. Please refer to the software's manual for details on them.

Control key

Ctrl

When this key is pressed together with another character key, a control code is generated. Because the valid control codes and their function depend on the software used, refer to the software's manual for detailed information on the control codes.

Shift key

⇧

When this key is pressed together with a character input key, the corresponding symbol in the shift position (upper symbol on the key) or the corresponding capital letter (or the letter on the key) is entered.

Alternate key

Alt

When this key is pressed together with the number key of the numeric keys 2, the ASCII code of the key pressed can be entered as a decimal value.
Example : Alt + 6 5 → A (41H = 65)

Capital lock key

Caps Lock

When this key is pressed, the indicator lights and all letters are entered in capitals. A small letter is entered when the Shift key is pressed. When this key is pressed again, it will unlock. This key will not affect the special character or numeric keys.

Enter key

←┘

Press this key to indicate the end of input of a data line or commands from the keyboard. Press this key every time you finish entering a line. The cursor moves to the next line and waits for the entry of the next data or command.

Back space key

←

When this key is pressed, the cursor moves one space to the left and the character in that position is deleted.

Print screen

Print Screen

When this key is pressed, the display on the screen will be printed out.

Ctrl + Alt + Delete
When the Ctrl, Alt and Delete keys are pressed simultaneously, the system restarts.

Ctrl + Alt + Esc
When the Ctrl, Alt and Esc keys are pressed simultaneously, the setup program in the system ROM is started. Refer to Section 1-3-3 for details.

Ctrl + Alt + ↑ or ↓
When the Ctrl, Alt and ↑ keys are pressed simultaneously, the CPU clock frequency is set to high (10MHz).
When the Ctrl, Alt and ↓ keys are pressed simultaneously, the CPU clock frequency is set to low (8MHz). When the system is reset to the status set in the setup RAM. To change the CPU clock frequency status in the setup RAM, use the setup program in the system ROM. Refer to Section 1-3-3 for details.

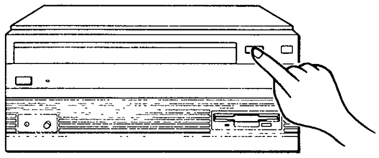
1-3-2. Using Videodisc Player

You can control the videodisc player using the program included in the SMW-5001 VIEW/VGA Operating System Package or some control program developed for the VIEW system or the IBM PC. Refer to the respective software's manual for details.

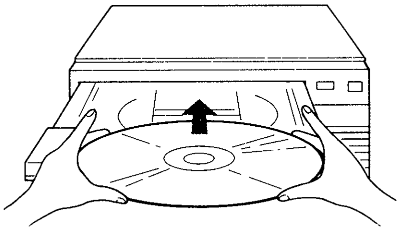
1-3-2-1. Inserting and removing the videodisc

1. Turn on the power of the system and start it. For details, refer to the SMW-5001's manual.

2. Press the OPEN/CLOSE button on the front to open the disc compartment.



3. Place the videodisc on the table with the desired program label up.



4. Press the OPEN/CLOSE button again. The compartment closes and the DISC indicator lights.

Notes

- To avoid damaging the disc, do not move the unit while it is operating or while it contains a disc.
- When the disc compartment is the open position, do not press down on it strongly, or place heavy objects on it.
- Remove the disc from the compartment after playing it, if the unit will not be used for any length of time.

1-3-2-2. Removing the videodisc

Press the OPEN/CLOSE button to stop playing of the disc, no matter what mode the player is in. The disc will stop rotating, and the disc compartment will be ejected.

1-3-3. Setup Program in System ROM

When you first start the system after purchase or after you change the hardware configuration, you must set up the system using the Installation Program included in the SMW-5001 VIEW/VGA Operating System Package. However, when you want to change the configuration for the keyboard to "not installed," for example when you do not need the keyboard for a VIEW system as the keyboard is not used for demonstration, or when you want to change the CPU clock frequency as the optional board requires, you must use the setup program in the system ROM. The procedure is described below.

1. Turn on the power of the system.

2. When the message "Strike the F1 key to continue, F2 to run the setup utility" appears on the screen, press the F2 key.
   When the MS-DOS has started, press the Ctrl, Alt and Esc keys simultaneously.
   The setup program will start.

3. Select the item to be set using the ↓ or ↑ key and then select the setting using the → or ← key.

4. After you have changed the setting, press the Esc key. The system will restart with the new setting.

Notes

- In step 3, the following items also appear and they can be changed. However, as they have already been set properly by using the SMW-5001 installation program, do not change their setting.

Diskette A :	3.5-inch, 1.44M bytes.
Diskette B :	Not Installed.
Hard disk drive 1 :	Type 17 when the SCK-5015 is installed or Not Installed.
Hard disk drive 2 :	Not Installed.
Base memory size	640K bytes.
Extended memory size	Specify the size or Not Installed. 2048K bytes when the SMI-5051 is installed.
Display	VGA/EGA
Coprocessor	"Not Installed" will be displayed.

- When an item is selected and you press the F1 key, the explanation for that item will be displayed on the screen.
- You can temporarily change the CPU clock frequency by pressing the Ctrl + Alt + ↑ or ↓.
- The setup program in the system ROM may not be started when the TSR (Terminate and Stay Resident) program which is started by pressing the Ctrl, Alt or Esc is in the memory.

1-4. MESSAGES

During or after the power-on process, an error or an informational massage may be displayed on the screen. The messages and how to correct the error are as shown below.

1-4-1. Setup Trouble Messages

When one of the following messages is displayed, set the correct configuration information executing the "Set SETUP RAM" of the Installation Program included in SMW-5001.

- Diskette configuration error
- Errors found disk X : Failed initialization
- Errors found incorrect configuration information memory size miscompare
- Hard disk configuration error
- Invalid configuration information – please run SETUP program
- Time-of-day clock stopped
- Time-of-day not set – please run SETUP program

1-4-2. Hardware Trouble Messages

When one of the following messages is displayed, turn off the unit and turn it on again. If the error message is displayed again, something must be wrong with the hardware.

Hardware trouble messages

- Diskette drive reset failed
- Diskette drive 0 seek failure
- Display adapter failed ; using alternate
- Gate A20 failure
- Hard disk failure
- Hard disk read failure – strike F1 to retry boot
- Keyboard clock line failure*
- Keyboard data line failure*
- Keyboard controller failure*
- Keyboard struck key failure*
- Memory address line failure at *hex-value*, read *hex-value*, expecting *hex-value*
- Memory data line failure at *hex-value*, read *hex-value*
- Memory high address line failure at *hex-value*, read *hex-value*, expecting *hex-value*
- Memory double word logic failure at *hex-value*, read *hex-value*, expecting *hex-value*
- Memory odd／even logic failure at *hex-value*, read *hex-value*, expecting *hex-value*
- Memory parity failure at *hex-value*, read *hex-value*, expecting *hex-value*
- Memory write／read logic failure at *hex-value*, read *hex-value*, expecting *hex-value*
- No timer tick interrupt
- *Hex-value* optional ROM bad checksum = *hex-value*
- Shutdown failure
- Timer chip counter 2 failed
- Timer or interrupt controller bad
- Unexpected interrupt in protected mode

* One of these message may be displayed when you press a key on the keyboard during the system start-up procedure.

1-4-3. Other Messages

The following are messages which are not explained above and the method of correcting the errors.

- Diskette driver 1 seek failure

You can install only one folppydisk drive in the VIW-5000. Check the item "Diskette B : " of the configuration information using the setup program in the system ROM. It should be set to "Not installed". If the setting is not correct, change it. If it is correct, turn off the unit and turn it on again. If the error message is displayed again, something must be wrong with the hardware.

- Diskette read failure - strike F1 to retry boot

Change the folppydisk to a bootable one and try starting the system again.

- Hard disk controller failure

Can check the item "Hard disk" of the configuration information using the SMW-5001 Installation Program. If it is correct, turn off the unit and turn it on again. If the error message is displayed again, something must be wrong with the hardware.

- No boot device available – strike F1 to retry boot

Insert the system disk in the folppydisk drive A and press F1 key.

- No boot sector on hard disk – strike F1 to retry boot

Format the drive C or make it bootable.

- Not a boot diskette – strike F1 to retry boot

Replace the disk with the bootable one and retry boot.

- I/O card parity interrupt at *address*. Type (S) hut off NMI, (R) eboot, other keys to continue
- Memory parity interrupt at *address*. Type (S) hut off NMI, (R) eboot, other keys to continue

Press the S key, and you will temporarily continue the operation. Then turn off the unit and turn it on again. If the error message is displayed again, something must be wrong with the hardware.

1-4-4. Informational Messages

The following are messages that provide information and require no action.

- *Hex-value* Base Memory

Shown the size of the base memory that was tested successfully.

- *Hex-value* Extended Memory

Shown the size of the extended memory that was tested successfully.

- Decreasing available memory

Displayed immediately after an error message, indicating that the memory chips failed. Refer to the solution for that error message.

- Memory tests terminated by keystroke

Indicates that you have pressed the space-bar during the memory tests and have stopped the memory tests.

- Strike the F1 key to continue

Indicates that an error was detected during the self-test diagnostics. Press the F1 key to attempt to boot.

1-5. TECHNICAL INFORMATION

1-5-1. Display Mode

This VIEW system features two VGA setups : Normal VGA and Superimposed VGA. The table on Section 1-5-1-5 show the various display modes in both VGA setup.

1-5-1-1. Normal VGA

When the power of the VIEW system is turned on, it starts up in the VGA setup. The Normal VGA setup is compatible with the VGA display adapter used by the IBM Personal System/2.

In this setup, the computer graphics cannot be superimposed on video images.

1-5-1-2. Superimposed VGA

This VGA setup is invoked when the VIEW/VGA Control Program or Superimpose Driver included in the SMW-5001 VIEW/VGA Operating System Package is installed. All display modes under the superimposed VGA setup are made compatible with 31.5KHz horizontal and 60Hz vertical frequencies to allow superimposing of computer graphics on video images. The monitor's display area is slightly smaller than the Normal VGA setup. The ratio between the display area's horizontal width and vertical height also differs.

Display Mode Table

Mode	Type	Colors[1]	Characters	Display buffer start	Dots per character	Max pages	Resolution
0 ,1	Character	16	40 × 25	B8000H	8 × 8	8	320 × 200[2]
0*,1*	Character	16	40 × 25	B8000H	8 × 14	8	320 × 350
0+,1+	Character	16	40 × 25	B8000H	9 × 16	8	360 × 400
2 ,3	Character	16	80 × 25	B8000H	8 × 8	8	640 × 200[2]
2*,3*	Character	16	80 × 25	B8000H	8 × 14	8	640 × 350
2+,3+	Character	16	80 × 25	B8000H	9 × 16	8	720 × 400
4 ,5	Graphics	4	40 × 25	B8000H	8 × 8	1	320 × 200[2]
6	Graphics	2	80 × 25	B8000H	8 × 8	1	640 × 200[2]
D	Graphics	16	40 × 25	A0000H	8 × 8	8	320 × 200[2]
E	Graphics	16	80 × 25	A0000H	8 × 8	4	640 × 200[2]
10	Graphics	16	80 × 25	A0000H	8 × 14	2	640 × 350
11	Graphics	2	80 × 30	A0000H	8 × 16	1	640 × 480
12	Graphics	16	80 × 30	A0000H	8 × 16	1	640 × 480
13	Graphics	256	40 × 25	A0000H	8 × 8	1	320 × 200[2]
5F[3]	Graphics	256	80 × 30	A0000H	8 × 16	1	640 × 480

* Enhanced mode of the IBM Enhanced Graphics Adapter
+ Enhanced mode of the IBM Personal System/2 VGA Display Adapter
1) Selectable from 262,144 colors for simultaneous display
2) 200-line vertical resolution modes are double-scanned to display 400 lines on the screen.
3) This mode is supported only when the optional SMI-5051 Graphics Memory Expansion is installed.

1-5-2. Tips on Videodiscs

1-5-2-1. Types of videodiscs

CAV (Constant Angular Velocity) disc

The CAV disc always rotates at a constant speed of 1800 r.p.m. and the laser beam moves from the inner part of the disc to the outer. Up to 30 minutes of playback (54,000 frames) is possible on one side of the disc.

Each frame of the playback picture is recorded on one track and is reproduced in one rotation. The frame number is recorded on the track.

Flexible playback operation such as variable speed playback and repeat play are possible using the frame numbers as reference.

CLV (Constant Linear Velocity) disc

With the CLV disc, the rotational speed varied from 600 r.p.m. to 1800 r.p.m. so that a constant linear velocity is maintained. The laser beam moves from the inner part of the disc to the outer as with CAV discs.

Playback of up to one hour is possible on one side of the disc, although only normal play, scan and search operations are possible. The elapsed playback time or the chapter number being played can be displayed on the monitor screen. Search for the beginning of chapters or specified time codes is possible.

1-5-2-2. Comparison of Sony videodisc code types

Type	Purpose	Location on disc	Capacity	Customer's creation method	Encoding method
I. CAV discs Vertical blanking (partial listing)					
– frame number*1)	frame access	all vertical blankings	00001 to 54000	not available	added automatically during mastering
(picture numbers)					
– picture stop*2)	automatic stop on a frame, during "play" and "slow" modes	designated vertical intervals	up to 54000	list of time codes on a master tape to have stops	added during mastering
– Chapter number*3)	divide content into chapters	designated vertical blankings	00 to 79 ; minimum = 30 tracks	list of first/last time codes on a master tape of all chapters	added during mastering
II. CLV discs Vertical blanking					
– time code number	time code access	all vertical blankings	00 hr 00 mins 00 sec to 01 hr mins	not available	added automatically during mastering
– chapter number	divide content into chapters	designated vertical blankings	00 to 79 ; minimum = 30 tracks	list of first/last time codes on a master tape of all chapters	added during mastering
III. CAV/CLV discs					
– Lead-in*4)	locate the beginning of the program on a disc	designated vertical blankings	–	not available	added during mastering
– Lead-out*4)	locate the end of the program on a disc	–	–	not available	added during mastering

*** 1) Frames**

The CAV discs have up to 54,000 "frames" which are numbered in sequence. One frame is recorded on one track, that is, a frame is played back with one rotation of the disc. You can search for a particular frame quickly or repeat a particular sequence of frames.

*** 2) Picture stop**

When the player detects this code, the playback enters the still mode. This code may be ignored in the scan and search modes.

*** 3) Chapters**

There are CAV and CLV discs on which "chapters," as the chapter of a book, are pre-recorded. If a chapter number is displayed after a frame number has been displayed (on a CAV disc) or after playback time is displayed in minutes (on a CLV disc) when you change the display mode, the data are pre-recorded in chapter.

You can easily search for a particular chapter and play it back repeatedly.

*** 4) Lead-in/Lead-out**

When the player detects the lead-out code, it returns to the beginning of a disc, detects the lead-in code and repeats playback or stops at the beginning of the program area according to the AUTO REPEAT switch setting.

When the player detects the lead-in code or lead-out cord in SCAN mode, the same result will be obtained.

1-5-3. Troubleshooting of Videodisc Player

Many apparent malfunctions may be caused by a misoperation or an oversight. If any difficulty arises in operation, check through this list of symptoms and causes. Should the difficulty persist, unplug the unit and contact your authorized Sony service facility.

Symptom	Cause
The disc compartment is ejected automatically.	• The videodisc is not placed correctly on the tray. • The videodisc is scratched or has dirt on its surface. • The disc is upside down. The side to be played back should be placed facing down.
The disc compartment does not come out.	• Power is not turned on.
Picture is not displayed, although the DISC indicator lights.	• The monitor is not turned on. • The connection of the monitor is not correct. • The disc is upside down. The side to be played back should be facing down.
Picture is not displayed, although the DISC indicator blinks.	• The videodisc is not placed correctly on the tray.
Poor picture quality	• The connection of the monitor is not correct. • An equipment is near the player to transmit noise and affect the picture quality of the videodisc. • The disc to be played back has a scratch or dirt on the surface. • There moisture condensation in the videodisc player.
No audio	• The speaker system is not connected correctly. • The volume setting of the amplifier is too low. • Audio is muted in all modes other than normal playback.
Playback of a certain section of the disc is not possible.	• The videodisc is scratched or has dirt on a section of it.
A certain section of the videodisc cannot be located by searching.	• The videodisc is scratched or has dirt on a section of it. Replace the defective disc with another one.
The picture is muted and the DISC indicator is lit.	• A search operation is taking place. If the specified number is invalid (not on the disc) or if a defective disc prevents the proper section from being found, the player remains in the search mode for about 20 seconds.
Fast forward or reverse playback is not possible.	• A CLV disc is used.

1-5-4. Specifications

1-5-4-1. CPU

Processor used	Intel 80286
Clock frequency	8MHz/10MHz (selectable by the software)
Interrupt	External interrupts (software initiated) INT instructions Instruction exceptions
Resetting	Automatic at power on

1-5-4-2. Memory

RAM	640K bytes (resident)
Video RAM	512K bytes (when SMI-5051 Graphics Memory Expansion in installed.)
ROM	128K bytes Initial program loader, Setup program Diagnostics program, and I/O driver
DMA	7-channel programmable DMA Channel 2 : folppydisk interface

1-5-4-3. CRT Display

Screen config.	Superimposition of VGA display over the video images
RGB video output	RGB analog signal, 0-0.7Vp-p, 75 Ω
Sync signal frequency	Horizontal : 31.5KHz Vertical : 60Hz for all superimposed VGA mode and modes 11, 12 and 5F in normal VGA mode 70Hz in normal VGA mode (except 11, 12 and 5F)

1-5-4-4. I/O Interface

Keyboard	5-pin DIN jack TTL level, serial transfer
RS-232C	9-pin connector, asynchronous Baud rate : Programmable up to 9600 baud (COM1)
RS-232C (Internal)	Asynchronous (TTL level), for controlling videodisc player part Baud rate : Programmable up to 9600 baud (COM2)
Printer	25-pin connector TTL level, 8-bit parallel transfer
Folppydisk	3.5-inch micro folppydisk 2HD type : 1.44M bytes (formatted) 3.5-inch micro folppydisk 2DD type : 720K bytes (formatted)
Timer/Calendar	DS1287 with back up function (5 years)

1-5-4-5. Playback System

Disc format	Laser Vision
Pick-up method	Laser beam (reflective)
Laser	Diode laser ($\lambda = 7800$ Å)
Emission duration	Continuous
Laser output	0.4 mW* max.
Videodisc	12" and 8"
Maximum playing time	CAV : 30 min/side CLV : 60 min/side
Spindle revolution	CAV : 1800 r.p.m. CLV : 1800 to 600 r.p.m.
Access time	CAV : 3 sec (by frame), 10 sec (by chapter) CLV : 10 sec
Control code	Compatible with the control codes for an Sony LDP-1200 Videodisc Player (Refer to the LDM-1200 Interface Manual)

* This output is the value measured at a distance of about 1.6 mm from the objective lens surface on the Optical Pick-up Block.

1-5-4-6. Audio

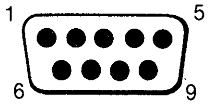
Output	Line out : −1.5dB (1KHz, 100 % MOD, load impedance 47kΩ) Load impedance 2k Ω and more unbalanced
S/N ratio	CX ON : 70dB and more CX OFF : 56dB and more
Frequency response	40Hz to 20KHz

1-5-4-7. General

Power requirement	120V AC ±10%, 60Hz
Current consumption	5A max. (VIW-5000 2A, OUTLET 3A)
Operating temperature	+5℃ to +35℃ (+41°F to +95°F)
Operating humidity	25% to 80% (at +25℃/+77°F)
Storage temperature	−20℃ to +60℃ (−4°F to +140°F)
Dimensions (w/h/d)	Approx. 430 × 190 × 410 mm $16\frac{15}{16} \times 7\frac{1}{2} \times 16\frac{1}{8}$ inches excluding projecting parts and controls
Weight	Approx. 17 kg excluding a keyboard

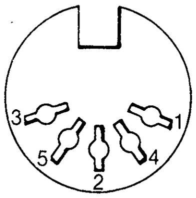
1-5-5. Pin Assignment of Connectors

1-5-5-1. RS-232C Connector



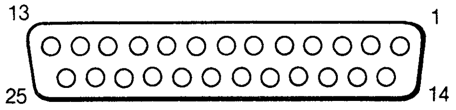
Pin No.	Signal name
1	CD
2	– RxD
3	– TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

1-5-5-2. KEYBOARD Jack



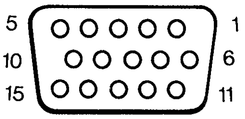
Pin No.	Signal name
1	KB CLK
2	KB DATA
3	N.C.
4	GND
5	+ 5V

1-5-5-3. PRINTER Connector



Pin No.	Signal name	Pin No.	Signal name
1	– STROBE	14	– AUTO FD
2 to 9	DATA 0 to 7	15	– ERROR
10	– ACK	16	– INIT
11	BUSY	17	– SLCT IN
12	P.E	18 to 25	GND
13	SLCT		

1-5-5-4. MONITOR Connector



Pin No.	Signal name	Pin No.	Signal name
1	R	8	B RTN (GND)
2	G	9	N.C.
3	B	10	GND
4	N.C.	11 and 12	N.C.
5	GND	13	H SYNC
6	R RTN (GND)	14	V SYNC
7	G RTN (GND)	15	N.C.

1-5-6. Memory Map

000000H	Main memory 640K bytes	
0A0000H	VGA video memory* 128K bytes	
0C0000H	Expanded memory Page frame** 128K bytes	
0E0000H	System ROM 128K bytes	VGA BIOS 32K bytes
0E8000H		Reserved 32K bytes
0F0000H		System BIOS 64K bytes
100000H	Extended memory** 2M bytes	
300000H	Reserved 12M + 896K bytes	
FE0000H	Code image of 0E0000H to 0FFFFFH 128K bytes	
FFFFFFH		

* You can access the 256K bytes (resident) or 512K bytes (when an optional SMI-5051 Graphics Memory Expansion is installed) memory area by banking in the 128K bytes VGA video memory.

** This area can be used when an SMI-5050 Memory Expansion is installed.

1-6. N.B.

1-6-1. Warning

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. it has been tested and found to comply with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

The shielded interface cable recommended in this manual must be used with this equipment in order to comply with the limits for a computing device pursuant to Subpart J of Part 15 of FCC rules.

1-6-2. Caution

The use of optical instruments with this product will increase eye hazard.

As the laser beam used in this videodisc player is harmful to the eyes, do not attempt to disassemble the cabinet. Refer servicing to qualified personnel only.

This apparatus complies with the Class A limits for radio noise emissions set out in Radio Interference Regulations.

The export of this product is subject to the authorization of the government of the exporting country.

1-6-3. Registered Trademarks

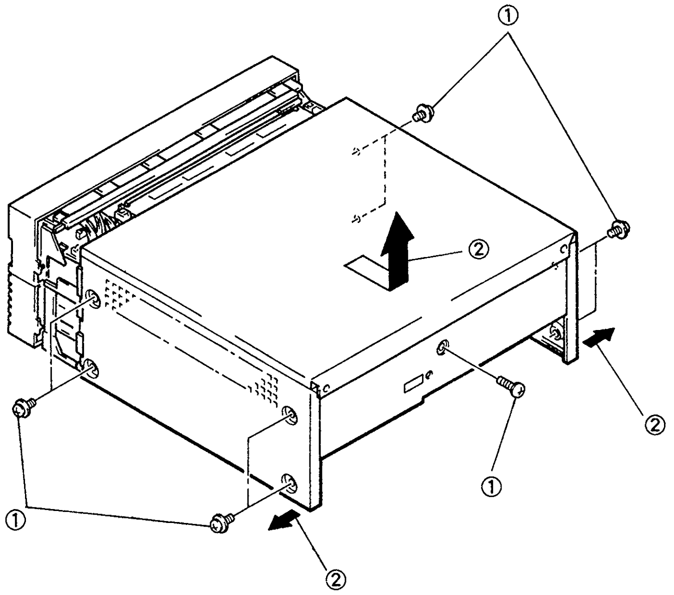
IBM is a registered trademark of International Business Machine Corporation.
IBM PC/AT and Personal System/2 are trademark of IBM.
MS-DOS® is a registered trademark of Microsoft Corporation.

CHAPTER 2
SERVICE INFORMATION

2-1. REMOVAL

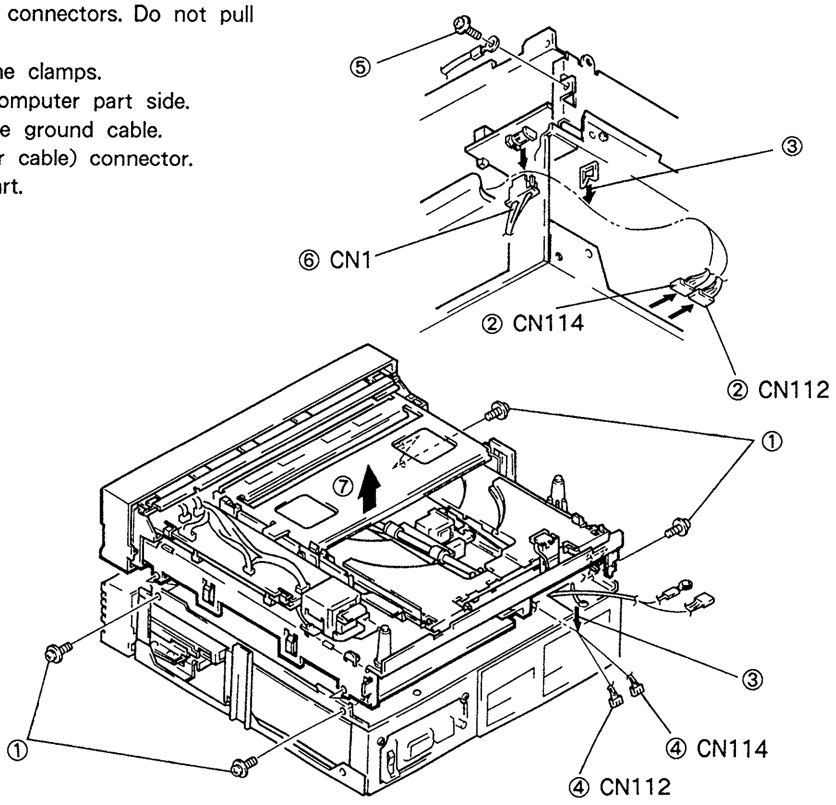
2-1-1. Cover Assembly

① Unscrew the nine screws.
② Gently lift the cover off the chassis holding its lower rear edges.



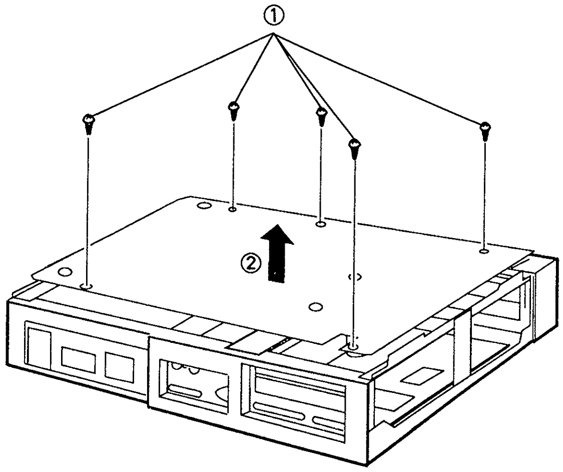
2-1-2. Videodisc Player Part

① Unscrew the four screws.
② Unplug the CN112 and CN114 connectors. Do not pull the cable.
③ Detach the data cables from the clamps.
④ Draw the data cables out of computer part side.
⑤ Remove the screw fastening the ground cable.
⑥ Unplug the CN1 (internal power cable) connector.
⑦ Remove the videodisc player part.



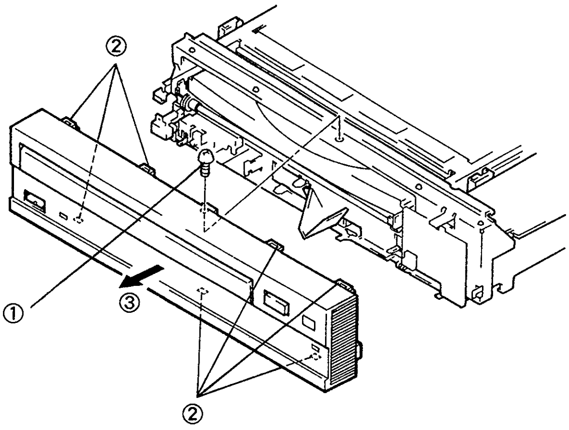
2-1-3. Shielding Sheet

① Unscrew the five screws.
② Remove the sheet.



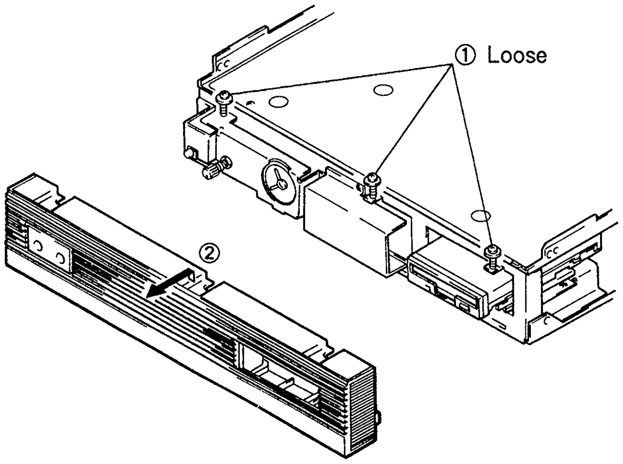
2-1-4. Front Panel Assembly of Videodisc Player Part

① Unscrew the screw.
② Remove the seven claws.
③ Remove the front panel assembly.



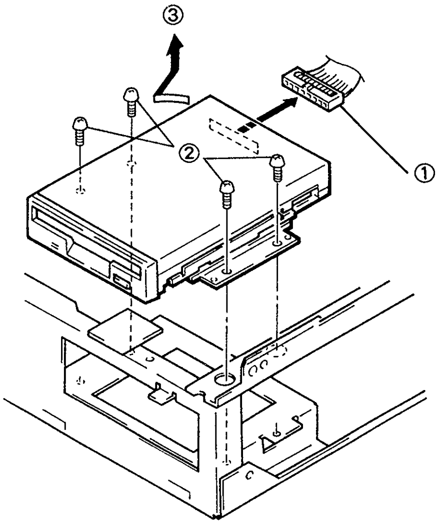
2-1-5. Front Panel of Computer Part

① Loose the three screws.
② Remove the front panel.



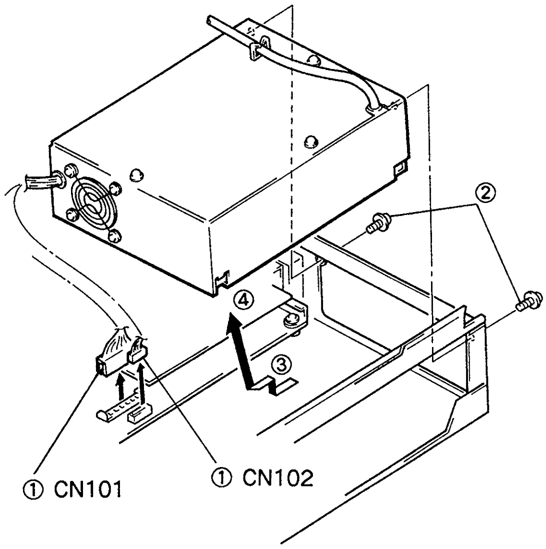
2-1-6. Micro Floppydisk Drive Part

① Unplug the connector. Do not pull the cable.
② Unscrew the four screws.
③ Gently lift the drive part off the chassis turning its posture.



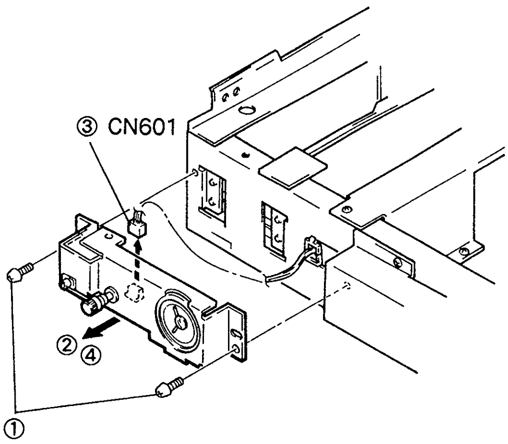
2-1-7. Switching Regulator Part

① Unplug the CN101 and CN102 connectors. Do not pull the cable.
② Unscrew the two screws.
③ Pull a little the regulator part.
④ Gently lift the regulator part off the chassis incline its posture.



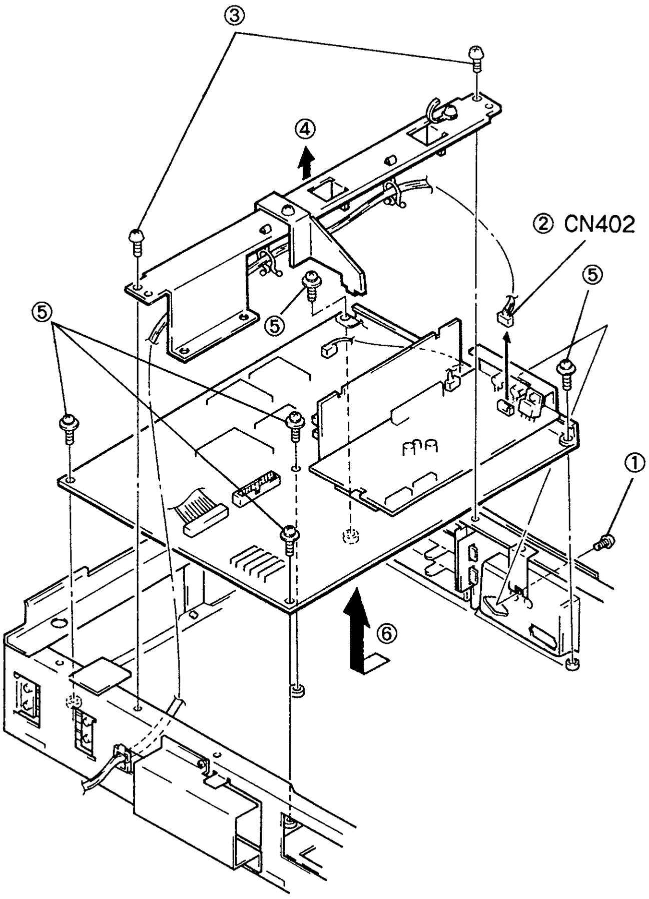
2-1-8. SP-7 Assembly

① Unscrew the two screws.
② Pull a little the SP-7 Assembly.
③ Unplug the CN601 connector. Do not pull the cable.
④ Remove the SP-7 assembly.



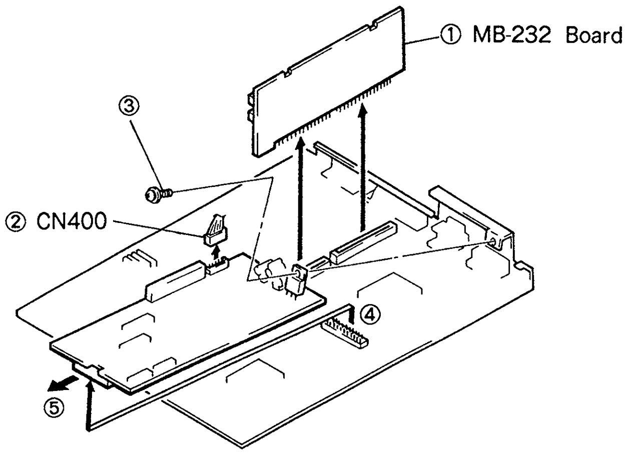
2-1-9. Center Stay and SY-143 Assembly

① Unscrew the screw.
② Unplug the CN402 connector. Do not pull the cable.
③ Unscrew the two screws.
④ Remove the stay.
⑤ Unscrew the five screws.
⑥ Remove the SY-143 assembly (including MB-232 and VS-39 boards).



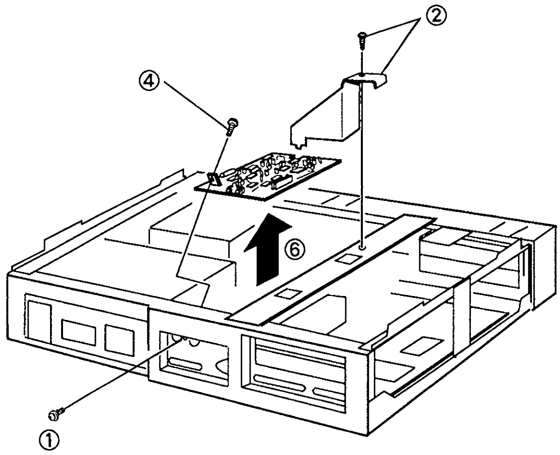
2-1-10. MB-232 Board and VS-39 Board

2-1-10-1. Remove they boards off the SY-143 assembly
Refer to right figure.
① Remove the MB-232 board.
② Unplug the CN400 connector. Do not pull the cable.
③ Unscrew the screw.
④ Unplug the CN401 connector.
⑤ Remove aslant the VS-39 board.



2-1-10-2. Each remove they boards off the chassis
VS-39 Board : Refer to right figure. See Section 2-1-9 for CN402, and Section 2-1-10-1 for CN401 and CN402.
① Unscrew the screw.
② Remove the screw fastening the retainer.
③ Unplug the CN400 and CN402 connectors. Do not pull the cable.
④ Unscrew the screw.
⑤ Unplug the CN401 connector.
⑥ Remove aslant the VS-39 board. See figure on Section 2-1-10-1.

MB-232 Board
① Remove the center stay. Refer to Nos. ② to ④ on Section 2-1-9.
② Remove the MB-232 board. See figure on Section 2-1-10-1.

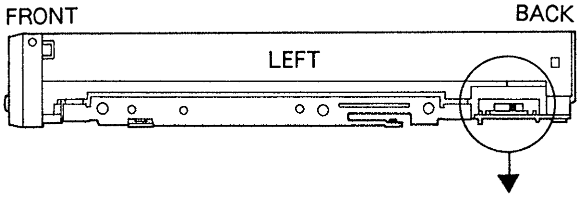


2-2. VIDEODISC PLAYER PART

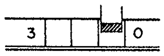
When servicing "Videodisc Player Part" of VIW-5000, use the LDP-1200 service manual (9-972-629-XX) together with one.
Be careful the video disc player part of LDP-1200 is different from that of VIW-5000 a little.
On this VIW-5000 service manual, computer sections are mainly described.

2-3. MICRO FLOPPYDISK DRIVE PART

When servicing "Micro Floppydisk Drive Part" of VIW-5000, use the service manual (9-975-189-XX) of MP-F17W together with one.



When using the micro floppydisk drive incorporated in VIW-5000, the setting switch is generally set to "1" position as shown at right.



SETTING SWITCH

2-4. INSTALLING INTERNAL OPTION

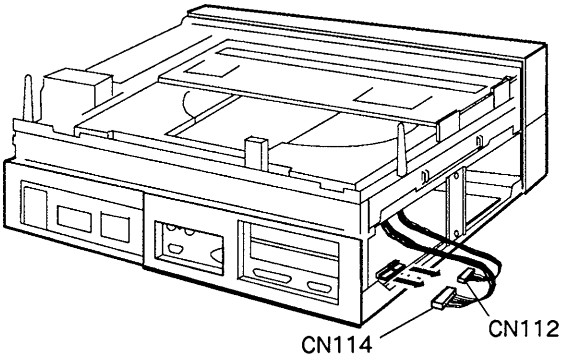
SCK-5015 : Refer to Chapter 10

SMI-5050 : Refer to Chapter 11

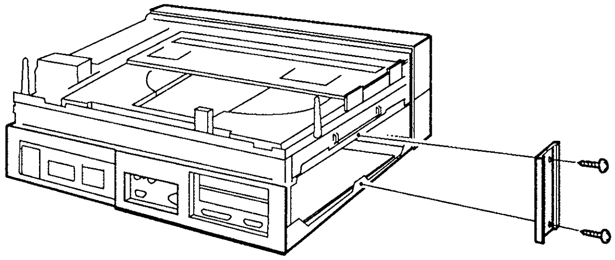
SMI-5051 : Refer to Chapter 12

For Bus Slots : As follows

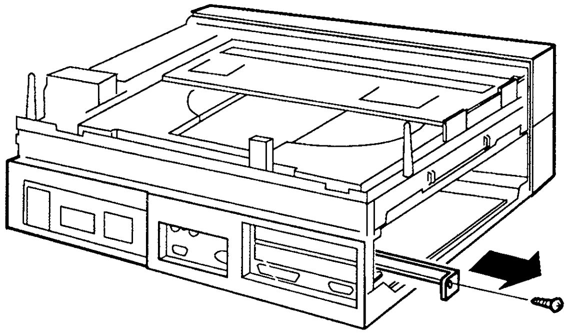
1. Remove the cover assembly. Refer to Section 2-1-1.
2. Unplug the CN112 and CN114 connectors. Do not pull the cable.



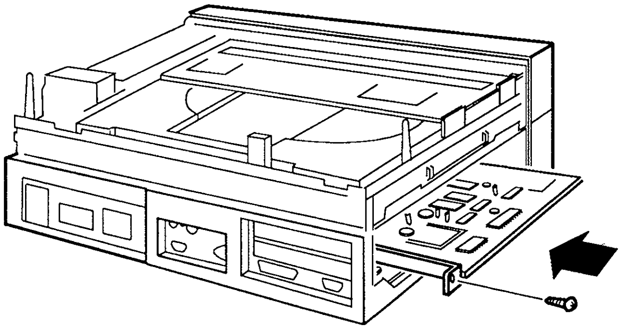
3. Remove the side plate.



4. Remove the plate from one of the slots.
   For each board installation, remove the plate from the lowest unoccupied expansion slot.



5. Insert the optional board while aligning it to the support brackets and push it forward until the edge connector properly enters the mating socket. Secure the optional board with the screw removed in step 4.



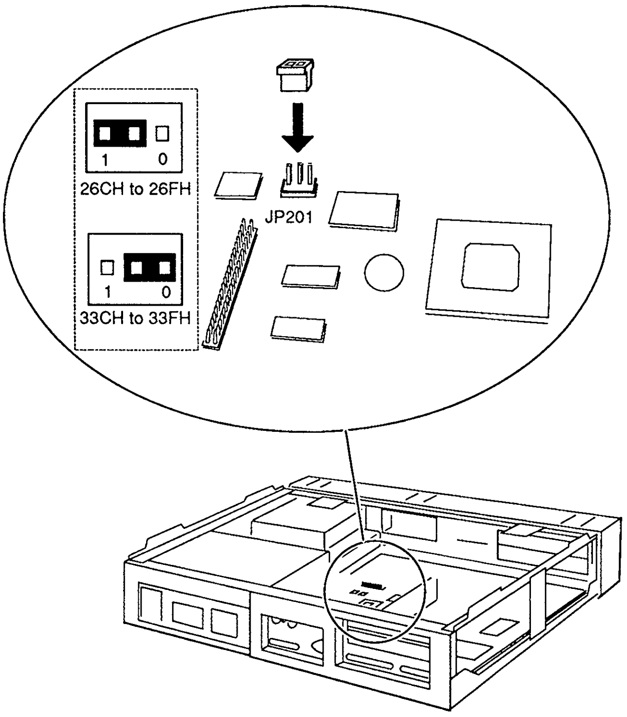
6. Attach the side plate removed step 2.
7. To change the superimposer I/O addresses, reset the jumper pins referring to the Section 2-5.
8. Plug in the CN112 and CN114 connectors.
9. Replace the cover assembly.

2-5. CHANGING SUPERIMPOSER I/O ADDRESSES

2-5-1. Remove the Parts

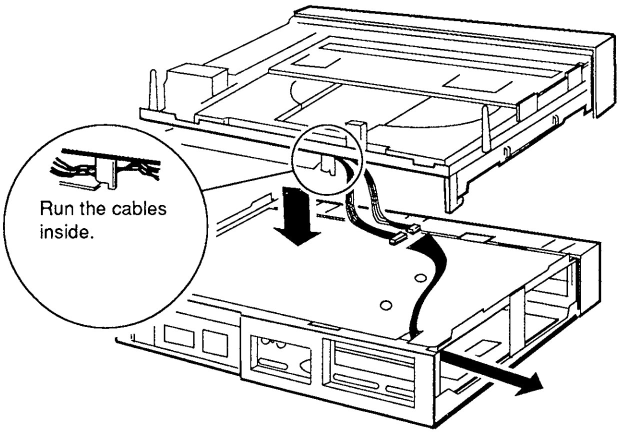
1. Remove the cover assembly.
   Refer to Section 2-1-1.
2. Remove the videodisc player part.
   Refer to Section 2-1-2.
3. Remove the shielding sheet.
   Refer to Section 2-1-3.
4. Remove the VS-39 board.
   Refer to Section 2-1-10-2.

2-5-2. Reset the Jumper Pins



2-5-3. Instruction the Parts

Follow the instructions provided in Section 2-5-1 in reverse order.
Be sure to the pass the data cables (Pull out in ④ of Section 2-1-2) inside the computer part.



Tips
When placing the videodisc player part in position, shift it slightly forward and then pull it backward on the computer part. This will make the operation easier.

Notes
- When reinstalling the VS-39 board, be sure to plug the VS-39 board's connector (CN401) into the mating connector (CN115) on the SY-143 board.
- Be sure to connect the internal cable before reinstalling the cover assembly.
- Be aware of internal wiring when placing the videodisc player part in position. Take a moment to check that no wires are squeezed under the unit.

2-6. REPAIR PARTS

1. Safety Related Components Warning.
   Components identified by shading marked with ⚠ on the schematic diagrams and repair parts list are critical to safe operation.
   Replace these components with Sony parts whose part numbers appear in this manual or in service bulletins and service manual supplements published by Sony.

2. Replacement Parts supplied from Sony Parts Center will sometimes have a different shape from the original parts. This is due to "accommodating the improved parts and /or engineering changes" or "standardization of genuine parts".
   This manual's repair parts list indicate the parts numbers of "the standardization of genuine parts at present".
   Regarding engineering parts changes in our engineering department, refer to Sony service bulletins and service manual supplements.

3. Items marked "＊" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.

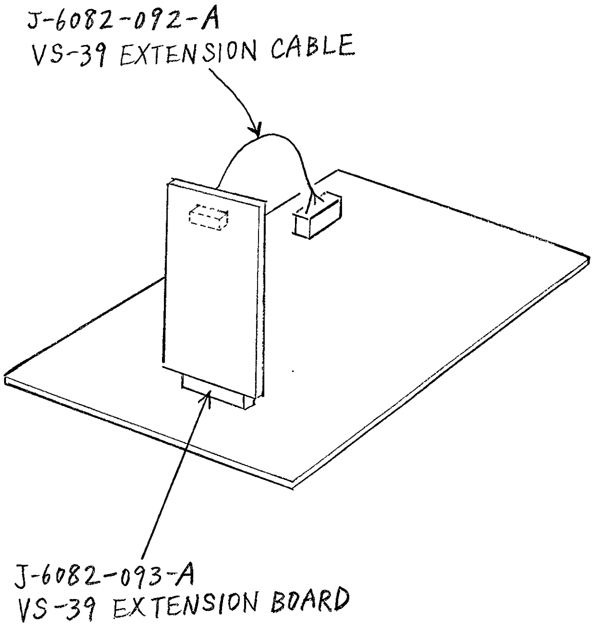
4. Abbreviations

Ref. No.	Description
C□□, CV□□	CAPACITOR
CN□□	CONNECTOR
CP□□	COMBINATION
D□□	PARTS
DL□□	DIODE
F□□	DELAY LINE
FL□□	FUSE
IC□□	FILTER
L□□, LV□□	IC
M□□	INDUCTOR
R□□, RV□□	MOTOR
RB□□	RESISTOR
RY□□	RESISTOR BLOCK
S□□, SW□□	RELAY
SB□□	SWITCH
T□□	SOLAR BATTERY
TH□□	TRANSFORMER
X□□	THERMISTOR

5. Units for Capacitors, Inductors and Resistors.
   The following units are assumed in schematic diagrams and repair parts list unless otherwise specified :
   Capacitors : μF
   Inductors : μH
   Resistors : Ω

2-7. FIXTURES

J-6093-490-A	EXTENSION BOARD ASSEMBLY 基板立て延長基板（SMI-3083Dで使用）
J-6093-570-A	IC EXTRACTION TOOL, 68-PIN PLCC IC引き抜き治具（一般治具）
~~J-~~	~~BOARD STAND KIT, VS-39~~
J-6200-200-A	KEYTOP EXTRACTION TOOL キートップ引き抜き治具（一般治具）
J-6082-092-A	VS-39 EXTENSION CABLE (VS-39延長ケーブル)
J-6082-093-A	VS-39 EXTENSION BOARD (VS-39 L型コネクター)



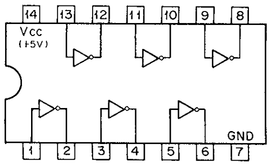
CHAPTER 5
COMPUTER SCHEMATIC DIAGRAM

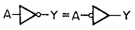
5-1. SEMICONDUCTOR PIN ASSIGNMENTS

TYPE	PAGE
1S2075K	5-21
1SS120	5-21
1SS123	5-21
1SS135E	5-21
1SS168	5-21
1SS223	5-21
1SS226	5-21
1T33C-01	5-21
2SA1162	5-21
2SA812	5-21
2SC1623	5-21
2SC2655	5-21
2SC4237	5-21
2SC458C	5-21
74AC00SJ	5-4
74F04SJ	5-2
74F08SJ	5-2
74F32SJ	5-2
74F373SJ	5-4
Am29827ASC	5-4
AN1431T	5-19
CX23065	5-11
CXD1030M	5-17
CXD1172M	5-17
D10LCA20	5-21
D1NL20	5-21
D3SB60	5-21
DFG1A8	5-21
DS1000M-50	5-5
DS1287	5-5
ERC38-06	5-21
FE3001	5-12
FE3010B	5-13
FE3021	5-14
FE3031	5-14
HZ5A3	5-21
HZ5C3	5-21
HZ6B2	5-21
LA7801	5-11
LM386N	5-11
M5F7805	5-19
M5F79M05	5-20
M5F79M12	5-20
MB3771DIP	5-19
MB81256-10PSZ	5-9
MB81464-10PSZ	5-9
MB81C4256-10PSZ	5-9
MC1488M	5-3
MC1489AM	5-3
MC74HC4053N	5-4
N13T1	5-21
N80286-10	5-16
NJM7805A	5-19
NJM78L05A	5-20
NJM78L09A	5-20
NJM79M12A	5-20
NT108PRO-35VOA99P	5-5
P8742AH	5-6
PC111S	5-21
PVGA1A	5-8
RC7805FA	5-19
RC78L05A	5-20
RC78L09A	5-20
RD4.7ES-B2	5-21
RD5.1ES-B3	5-21
RD5.6ES-B3	5-21
S15SC4M	5-21
SN7406NS	5-2
SN74ALS10NS	5-2
SN74ALS10ANS	5-2
SN74ALS32NS	5-2
SN74F240NS	5-3
SN74F241NS	5-3
SN74LS04NS	5-2
SN74LS06N	5-2
SN74LS125AN	5-2
SN74LS125ANS	5-2
SN74LS126ANS	5-2
SN74LS138NS	5-2
SN74LS244NS	5-3
SN74LS245NS	5-3
SN74LS32NS	5-2
SN74LS74ANS	5-2
STR9012	5-19
TA78L009AP	5-20
TC74HC00F	5-4
TC74HC123F	5-4
TC74HC123P	5-4
TC74HC14F	5-4
TC74HC221F	5-4
TC74HC4053AP	5-4
TC74HC74AP	5-4
TL084CN	5-11
TL601CPS	5-11
TMM2018AP-25	5-9
uPC358C	5-11
uPC358G2	5-11
uPC393C	5-11
uPC79M05H	5-20
uPC79M12H	5-20
uPD27C512C-15	5-10
uPD27C512D-15	5-10
uPD42102G-3	5-11
uPD65005GC-306-3B6	GATE ARRAY
uPD65006GF-325-3B8	GATE ARRAY
uPD65013S-526	GATE ARRAY
uPD6902C	5-17
V19C	5-21
V7020	5-18
VL16C452QC	5-6
WD37C65BJM	5-7

74F04SJ (FSC) FLAT PACKAGE
SN74LS04NS (TI) FLAT PACKAGE

TTL INVERTER
- TOP VIEW -


14
13
12
11
10
9
8
Vcc
(+5V)
GND
1
2
3
4
5
6
7



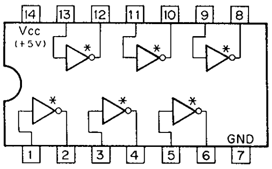
Y = $\overline{A}$

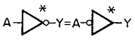
A	Y
0	1
1	0

0; LOW LEVEL
1; HIGH LEVEL

SN7406NS (TI) FLAT PACKAGE
SN74LS06N (TI)

TTL INVERTER BUFFER/DRIVER WITH OPEN-COLLECTOR
- TOP VIEW -


14
13
12
11
10
9
8
Vcc
(+5V)
*
GND
1
2
3
4
5
6
7



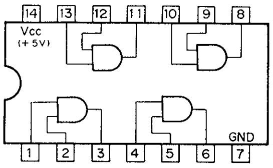
Y = $\overline{A}$

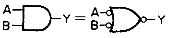
A	Y
0	1
1	0

0; LOW LEVEL
1; HIGH LEVEL
*; OPEN COLLECTOR

74F08SJ (FSC) FLAT PACKAGE

TTL 2-INPUT POSITIVE-AND GATE
- TOP VIEW -


14
13
12
11
10
9
8
Vcc
(+5V)
GND
1
2
3
4
5
6
7



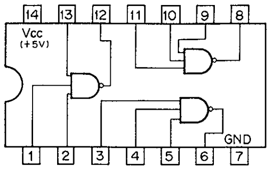
Y = A · B = $\overline{\overline{A}+\overline{B}}$

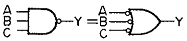
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

0; LOW LEVEL
1; HIGH LEVEL

SN74ALS10ANS (TI) FLAT PACKAGE
SN74ALS10NS (TI) FLAT PACKAGE

TTL 3-INPUT POSITIVE NAND GATE
- TOP VIEW -


14
13
12
11
10
9
8
Vcc
(+5V)
GND
1
2
3
4
5
6
7



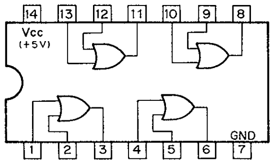
Y = $\overline{ABC}$ = $\overline{A}+\overline{B}+\overline{C}$

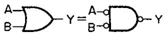
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

0 : LOW LEVEL
1 : HIGH LEVEL

74F32SJ (FSC) FLAT PACKAGE
SN74ALS32NS (TI) FLAT PACKAGE
SN74LS32NS (TI) FLAT PACKAGE

TTL 2-INPUT POSITIVE-OR GATE
- TOP VIEW -


14
13
12
11
10
9
8
Vcc
(+5V)
GND
1
2
3
4
5
6
7



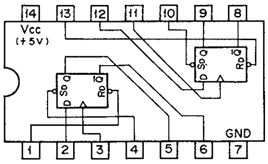
Y = A + B = $\overline{\overline{A}\cdot\overline{B}}$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

0; LOW LEVEL
1; HIGH LEVEL

SN74LS74ANS (TI) FLAT PACKAGE

TTL D-TYPE FLIP FLOP WITH DIRECT SET/RESET
- TOP VIEW -

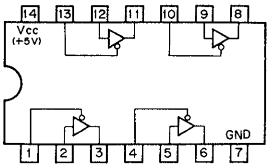

14
13
12
11
10
9
8
Vcc
(+5V)
Sd
Rd
D
Q
GND
1
2
3
4
5
6
7

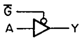
INPUTS				OUTPUTS	
$\overline{S_D}$	$\overline{R_D}$	CK	D	Qn+1	$\overline{Qn+1}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Qn	$\overline{Q}$n

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
1*; NONSTABLE

SN74LS125AN (TI)
SN74LS125ANS (TI) FLAT PACKAGE

TTL BUS BUFFER GATES WITH 3-STATE OUTPUTS
- TOP VIEW -


14
13
12
11
10
9
8
Vcc
(+5V)
GND
1
2
3
4
5
6
7

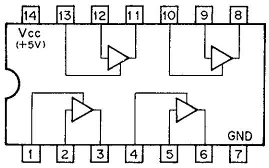


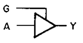
$\overline{G}$	A	Y
0	0	0
0	1	1
1	X	HI - Z

0; LOW LEVEL X; DON'T CARE
1; HIGH LEVEL HI-Z; HIGH IMPEDANCE

SN74LS126ANS (TI) FLAT PACKAGE

TTL BUS BUFFER GATE WITH 3-STATE OUTPUT
- TOP VIEW -


14
13
12
11
10
9
8
Vcc
(+5V)
GND
1
2
3
4
5
6
7

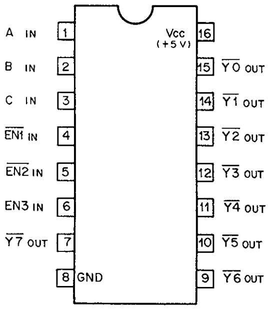


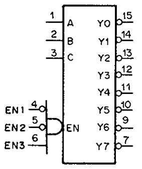
G	A	Y
1	1	1
1	0	0
0	X	HI-Z

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE

SN74LS138NS (TI) FLAT PACKAGE

TTL 3-TO-8-LINE DECODER/DEMULTIPLEXER
- TOP VIEW -


A IN 1
B IN 2
C IN 3
$\overline{EN1}$ IN 4
$\overline{EN2}$ IN 5
EN3 IN 6
$\overline{Y7}$ OUT 7
8 GND
Vcc (+5V) 16
15 $\overline{Y0}$ OUT
14 $\overline{Y1}$ OUT
13 $\overline{Y2}$ OUT
12 $\overline{Y3}$ OUT
11 $\overline{Y4}$ OUT
10 $\overline{Y5}$ OUT
9 $\overline{Y6}$ OUT


1 A
2 B
3 C
EN1 4
EN2 5
EN3 6
EN
Y0 15
Y1 14
Y2 13
Y3 12
Y4 11
Y5 10
Y6 9
Y7 7

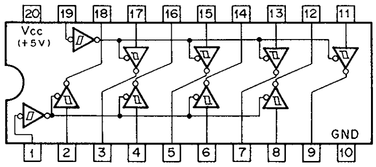
INPUTS				OUTPUTS							
EN	C	B	A	$\overline{Y7}$	$\overline{Y6}$	$\overline{Y5}$	$\overline{Y4}$	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
0	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	0
1	0	0	1	1	1	1	1	1	1	0	1
1	0	1	0	1	1	1	1	1	0	1	1
1	0	1	1	1	1	1	1	0	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1	1
1	1	1	0	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1	1	1

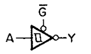
EN = $\overline{EN1}$ · $\overline{EN2}$ · EN3

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

SN74F240NS (TI) FLAT PACKAGE

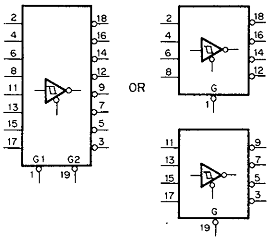
TTL 3-STATE SCHMITT TRIGGER INVERTER/LINE DRIVER
- TOP VIEW -


Vcc
(+5V)
GND
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10


$\overline{G}$
A
Y

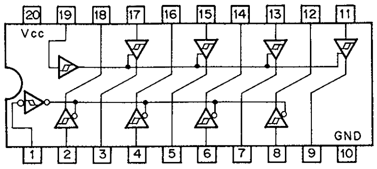
$\overline{G}$	A	Y
0	0	1
0	1	0
1	X	HI-Z

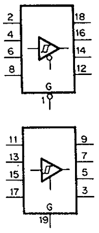
0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE

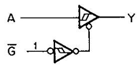

2 4 6 8 11 13 15 17
18 16 14 12 9 7 5 3
G1 G2
1 19
OR
G

SN74F241NS (TI) FLAT PACKAGE

TTL 3-STATE SCHMITT TRIGGER BUFFER/LINE DRIVER
- TOP VIEW -

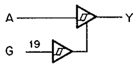

Vcc
GND
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10


2 4 6 8
18 16 14 12
G
1
11 13 15 17
9 7 5 3
G
19


A
Y
$\overline{G}$
1

$\overline{G}$	A	Y
0	0	0
0	1	1
1	0	HI-Z
1	1	HI-Z

HI-Z ;
HIGH IMPEDANCE

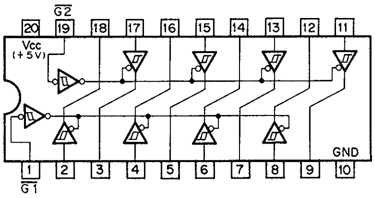


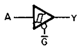
G	A	Y
0	0	HI-Z
0	1	HI-Z
1	0	0
1	1	1

HI-Z ;
HIGH IMPEDANCE

SN74LS244NS (TI) FLAT PACKAGE

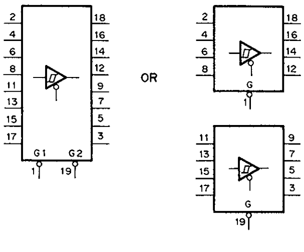
TTL 3-STATE SCHMITT TRIGGER BUFFER/DRIVER
- TOP VIEW -


$\overline{G2}$
Vcc
(+5V)
GND
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
$\overline{G1}$


A
Y
$\overline{G}$

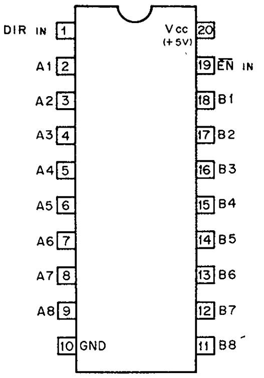
$\overline{G}$	A	Y
0	0	0
0	1	1
1	X	HI-Z

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE


2 4 6 8 11 13 15 17
18 16 14 12 9 7 5 3
G1 G2
1 19
OR
G

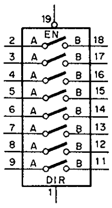
SN74LS245NS (TI) FLAT PACKAGE

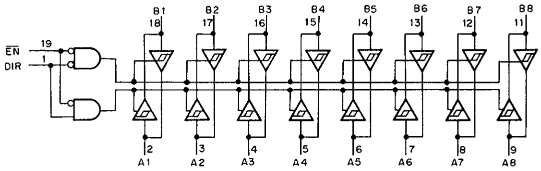
TTL BILATERAL SCHMITT TRIGGER BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
- TOP VIEW -


DIR IN 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
A7 8
A8 9
10 GND
Vcc (+5V) 20
19 $\overline{EN}$ IN
18 B1
17 B2
16 B3
15 B4
14 B5
13 B6
12 B7
11 B8

$\overline{EN}$	DIR	OPERATION
0	0	B to A
0	1	A to B
1	X	HI-Z

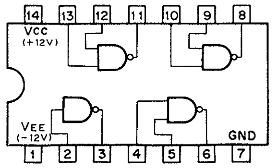
0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE

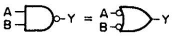

19
EN
2 3 4 5 6 7 8 9
A
B
18 17 16 15 14 13 12 11
DIR
1


B1 B2 B3 B4 B5 B6 B7 B8
18 17 16 15 14 13 12 11
$\overline{EN}$ 19
DIR 1
2 3 4 5 6 7 8 9
A1 A2 A3 A4 A5 A6 A7 A8

MC1488M (MOTOROLA) FLAT PACKAGE

2-INPUT (1-INPUT) POSITIVE-NAND LINE DRIVER
- TOP VIEW -


VCC
(+12V)
VEE
(-12V)
GND
14 13 12 11 10 9 8
1 2 3 4 5 6 7



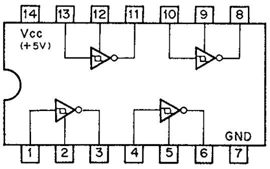
$Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

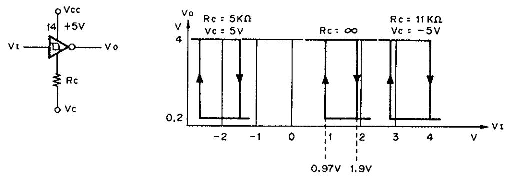
0: LOW LEVEL
1: HIGH LEVEL

MC1489AM (MOTOROLA) FLAT PACKAGE

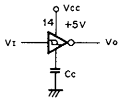
QUADRUPLE LINE RECEIVER
- TOP VIEW -


Vcc
(+5V)
GND
14 13 12 11 10 9 8
1 2 3 4 5 6 7

INPUT THRESHOLD SHIFTING

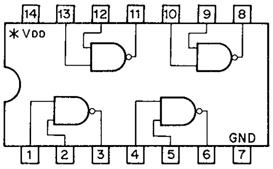


INPUT NOISE FILTERING

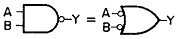

Vcc
14 +5V
Vi
Vo
Cc

74AC00SJ (FSC) FLAT PACKAGE
TC74HC00F (TOSHIBA) FLAT PACKAGE

C-MOS 2-INPUT NAND GATE
– TOP VIEW –


14
13
12
11
10
9
8
∗VDD
GND
1
2
3
4
5
6
7

∗VDD AC, HC; +2 to +6V
HCT; +5V



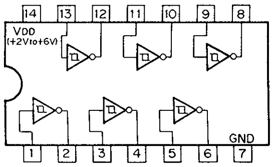
$Y = \overline{A \cdot B} = \overline{A} + \overline{B}$

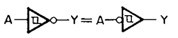
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

0; LOW LEVEL
1; HIGH LEVEL

TC74HC14F (TOSHIBA) FLAT PACKAGE

C-MOS SCHMITT TRIGGER INVERTER
– TOP VIEW –

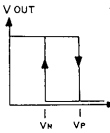

14
13
12
11
10
9
8
VDD (+2V to +6V)
GND
1
2
3
4
5
6
7

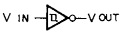


$Y = \overline{A}$

A	Y
0	1
1	0

0; LOW LEVEL
1; HIGH LEVEL

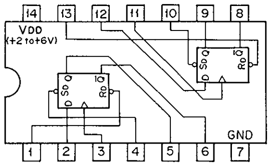




VDD	VN	VP
2.0V	0.75V	1.25V
4.5V	1.9V	2.7V
6.0V	2.6V	3.6V

TC74HC74AP (TOSHIBA)

C-MOS D-TYPE FLIP FLOP WITH DIRECT SET/RESET
– TOP VIEW –

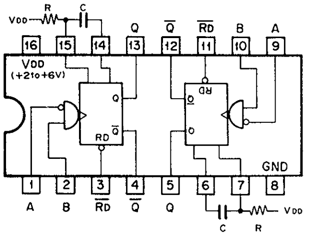

14
13
12
11
10
9
8
VDD (+2 to +6V)
SD
RD
Q
GND
1
2
3
4
5
6
7

INPUTS				OUTPUTS	
$\overline{S_D}$	$\overline{R_D}$	CK	D	Qn+1	$\overline{Qn+1}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1	1
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Qn	$\overline{Qn}$

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE

TC74HC123F (TOSHIBA) FLAT PACKAGE
TC74HC123P (TOSHIBA)

C-MOS DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR
– TOP VIEW –


VDD
R
C
Q
Q̄
R̄D
B
A
16
15
14
13
12
11
10
9
VDD (+2to+6V)
Q
RD
Q̄
GND
1
2
3
4
5
6
7
8
A
B
R̄D
Q̄
Q
C
R
VDD

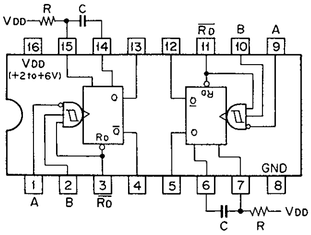
INPUT			OUTPUT	
$\overline{RD}$	A	B	Q	$\overline{Q}$
0	X	X	0	1
1	1	X	0	1
1	X	0	0	1
1	0	↑	⊓	⊔
1	↓	1	⊓	⊔
↑	0	1	⊓	⊔

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

OUTPUT PULSE WIDTH = 0.46CR

TC74HC221F (TOSHIBA) FLAT PACKAGE

C-MOS MONOSTABLE MULTIVIBRATOR WITH SCHMITT TRIGGER INPUT
– TOP VIEW –


VDD
R
C
R̄D
B
A
16
15
14
13
12
11
10
9
VDD (+2to+6V)
RD
Q̄
GND
1
2
3
4
5
6
7
8
A
B
R̄D
C
R
VDD

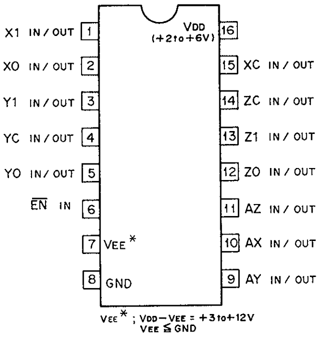
INPUTS			OUTPUTS	
$\overline{R_D}$	A	B	Q	$\overline{Q}$
0	X	X	0	1
X	1	X	0	1
X	X	0	0	1
1	0	↑	⊓	⊔
1	↓	1	⊓	⊔
↑	0	1	⊓	⊔

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE

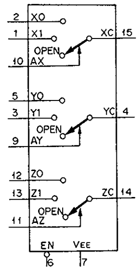
OUTPUT PULSE WIDTH = 0.7CR

MC74HC4053N (MOTOROLA)
TC74HC4053AP (TOSHIBA)

C-MOS 2-CHANNEL MULTIPLEXER/DEMULTIPLEXER
– TOP VIEW –


X1 IN/OUT 1
X0 IN/OUT 2
Y1 IN/OUT 3
YC IN/OUT 4
Y0 IN/OUT 5
E̅N̅ IN 6
7 VEE ∗
8 GND
VDD (+2to+6V) 16
15 XC IN/OUT
14 ZC IN/OUT
13 Z1 IN/OUT
12 Z0 IN/OUT
11 AZ IN/OUT
10 AX IN/OUT
9 AY IN/OUT

VEE ∗ ; VDD – VEE = +3 to +12V
VEE ≦ GND

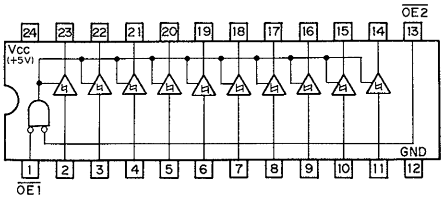

2 X0
1 X1
XC 15
OPEN
10 AX
5 Y0
3 Y1
YC 4
OPEN
9 AY
12 Z0
13 Z1
ZC 14
OPEN
11 AZ
EN
VEE
6
7

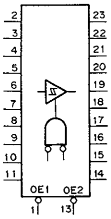
0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE.

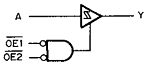
CONT. INPUTS		ON CHANNEL
$\overline{EN}$	A (X,Y,Z,)	
0	0	0
0	1	1
1	X	OPEN

Am29827ASC (AMD) FLAT PACKAGE

3-STATE 10-BIT BUS DRIVERS
– TOP VIEW –


O̅E̅2̅
24
23
22
21
20
19
18
17
16
15
14
13
Vcc (+5V)
GND
1
2
3
4
5
6
7
8
9
10
11
12
O̅E̅1̅


2
3
4
5
6
7
8
9
10
11
23
22
21
20
19
18
17
16
15
14
OE1
OE2
1
13

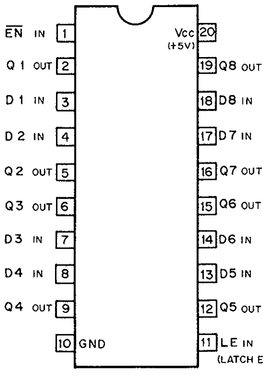


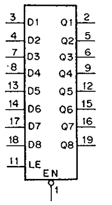
$\overline{OE1}$	$\overline{OE2}$	A	Y
0	0	0	0
0	0	1	1
1	X	X	HI-Z
X	1	X	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE

74F373SJ (FSC) FLAT PACKAGE

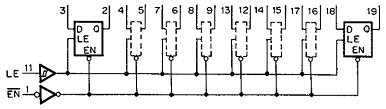
TTL 3-STATE OUTPUTS OCTAL LATCHES
– TOP VIEW –


E̅N̅ IN 1
Q1 OUT 2
D1 IN 3
D2 IN 4
Q2 OUT 5
Q3 OUT 6
D3 IN 7
D4 IN 8
Q4 OUT 9
10 GND
Vcc (+5V) 20
19 Q8 OUT
18 D8 IN
17 D7 IN
16 Q7 OUT
15 Q6 OUT
14 D6 IN
13 D5 IN
12 Q5 OUT
11 LE IN (LATCH ENABLE)


3 D1 Q1 2
4 D2 Q2 5
7 D3 Q3 6
8 D4 Q4 9
13 D5 Q5 12
14 D6 Q6 15
17 D7 Q7 16
18 D8 Q8 19
11 LE
EN
1

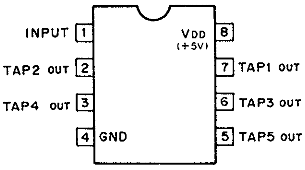
INPUTS			OUT
$\overline{EN}$	D	LE	Q
0	1	1	1
0	0	1	0
0	X	0	Qo
1	X	X	HI-Z

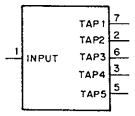
HI-Z;
HIGH IMPEDANCE
0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE

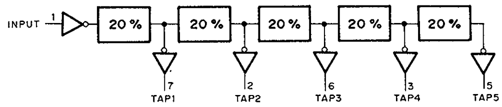

3
2
4
5
7
6
8
9
13
12
14
15
17
16
18
19
D Q
LE
EN
LE 11
E̅N̅ 1

DS1000M-50 (DELAY TIME = 50nS) (DALLAS SEMICONDUCTOR)

5 TAP SILLCON DELAY LINE
- TOP VIEW -


INPUT 1
TAP2 OUT 2
TAP4 OUT 3
4 GND
VDD (+5V) 8
7 TAP1 OUT
6 TAP3 OUT
5 TAP5 OUT

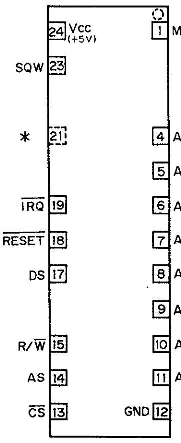

1 INPUT
TAP1 7
TAP2 2
TAP3 6
TAP4 3
TAP5 5

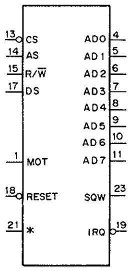

INPUT 1
20 %
20 %
20 %
20 %
20 %
7 TAP1
2 TAP2
6 TAP3
3 TAP4
5 TAP5

TYPE. NO.	DELAY TIME (ns)				
	TAP1	TAP2	TAP3	TAP4	TAP5
DS1000M-50	10	20	30	40	50
DS1000M-60	12	24	36	48	60
DS1000M-75	15	30	45	60	75
DS1000M-100	20	40	60	80	100
DS1000M-125	25	50	75	100	125
DS1000M-150	30	60	90	120	150
DS1000M-175	35	70	105	140	175
DS1000M-200	40	80	120	160	200
DS1000M-250	50	100	150	200	250
DS1000M-500	100	200	300	400	500

DS1287 (DALLAS SEMICONDUCTOR)

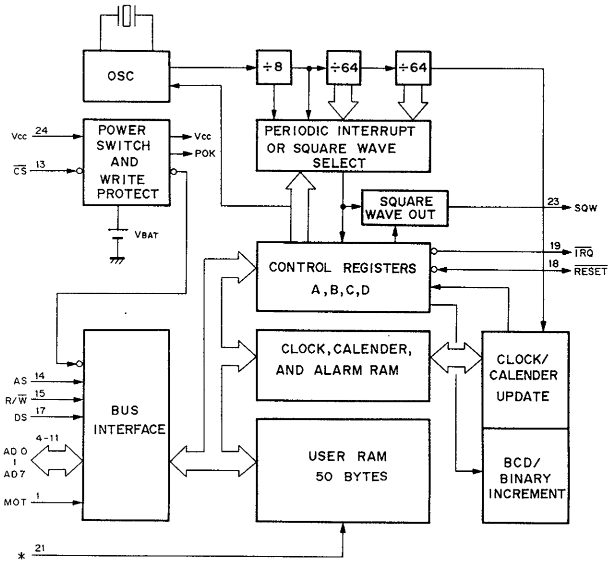
C-MOS REAL-TIME CLOCK PLUS RAM
- BOTTOM VIEW -


24 Vcc (+5V)
1 MOT
SQW 23
* 21
4 AD0
5 AD1
IRQ 19
6 AD2
RESET 18
7 AD3
DS 17
8 AD4
9 AD5
R/W 15
10 AD6
AS 14
11 AD7
CS 13
GND 12


13 CS
14 AS
15 R/W
17 DS
1 MOT
18 RESET
21 *
AD0 4
AD1 5
AD2 6
AD3 7
AD4 8
AD5 9
AD6 10
AD7 11
SQW 23
IRQ 19

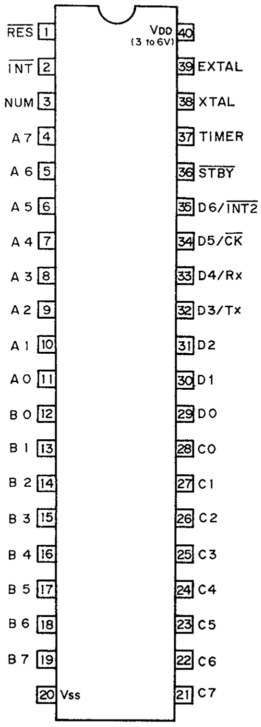
AD0 – AD7 ; MULTIPLEXED ADDRESS/DATA BUS
AS ; MULTIPLEXED ADDRESS STROBE
$\overline{CS}$; CHIP SELECT
DS ; DATA STROBE
$\overline{IRQ}$; INTERRUPT REQUEST (OPEN DRAIN)
MOT ; MOTOROLA/$\overline{INTEL}$ BUS TYPE SELECTION
$\overline{RCLR}$; RAM CLEAR (ONLY DS1287A)
$\overline{RESET}$; RESET INPUT
SQW ; SQUARE WAVE OUTPUT

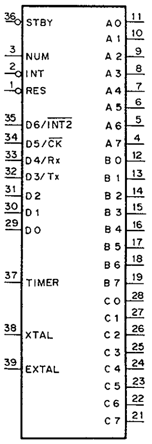
∗ 21PIN DS1287 ; NC(BE MISSING BY DESIGN)
DS1287A ; $\overline{RCLR}$


OSC
÷8
÷64
÷64
POWER SWITCH AND WRITE PROTECT
Vcc 24
CS 13
Vcc
POK
VBAT
PERIODIC INTERRUPT OR SQUARE WAVE SELECT
SQUARE WAVE OUT
23 SQW
CONTROL REGISTERS A,B,C,D
19 IRQ
18 RESET
CLOCK, CALENDER, AND ALARM RAM
CLOCK/ CALENDER UPDATE
BCD/ BINARY INCREMENT
BUS INTERFACE
AS 14
R/W 15
DS 17
4-11
AD 0 I AD 7
MOT 1
USER RAM 50 BYTES
* 21

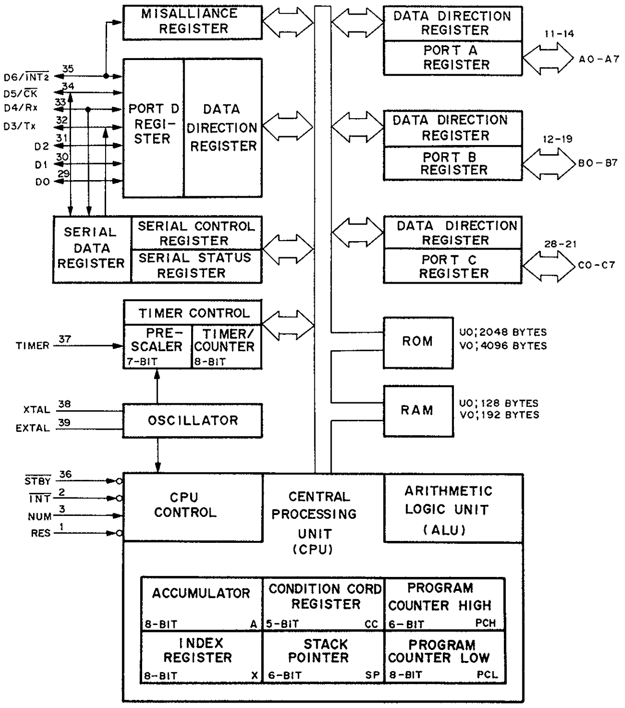
NT108PRO-35V0A99P

C-MOS MICROCOMPUTER UNIT
-TOP VIEW-


RES 1
INT 2
NUM 3
A7 4
A6 5
A5 6
A4 7
A3 8
A2 9
A1 10
A0 11
B0 12
B1 13
B2 14
B3 15
B4 16
B5 17
B6 18
B7 19
20 Vss
VDD (3 to 6V) 40
39 EXTAL
38 XTAL
37 TIMER
36 STBY
35 D6/INT2
34 D5/CK
33 D4/Rx
32 D3/Tx
31 D2
30 D1
29 D0
28 C0
27 C1
26 C2
25 C3
24 C4
23 C5
22 C6
21 C7


36 STBY
3 NUM
2 INT
1 RES
35 D6/INT2
34 D5/CK
33 D4/Rx
32 D3/Tx
31 D2
30 D1
29 D0
37 TIMER
38 XTAL
39 EXTAL
A0 11
A1 10
A2 9
A3 8
A4 7
A5 6
A6 5
A7 4
B0 12
B1 13
B2 14
B3 15
B4 16
B5 17
B6 18
B7 19
C0 28
C1 27
C2 26
C3 25
C4 24
C5 23
C6 22
C7 21

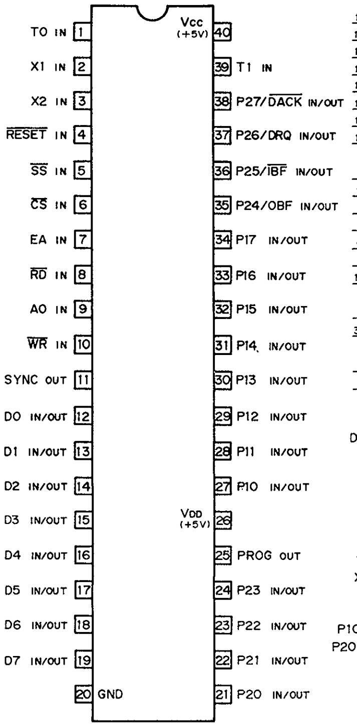
A0 – A7 ; PORT A INPUTS/OUTPUTS
B0 – B7 ; PORT B INPUTS/OUTPUTS
C0 – C7 ; PORT C INPUTS/OUTPUTS
$\overline{CK}$; SERIAL INTERFACE CLOCK INPUT
D0 – D6 ; PORT D INPUTS/OUTPUTS
EXTAL ; EXTERNAL CLOCK INPUT
OR CRYSTAL CONNECTION
$\overline{INT}$; INTERRUPTION 1 INPUT
$\overline{INT2}$; INTERRUPTION 2 INPUT
NUM ; NON-USER MODE (FIXED V_{SS} LEVEL)
$\overline{RES}$; RESET INPUT
Rx ; SERIAL DATA RECEIVE
$\overline{STBY}$; STANDBY SIGNAL INPUT
TIMER ; TIMER CONTROL INPUT
Tx ; SERIAL DATA TRANSFER

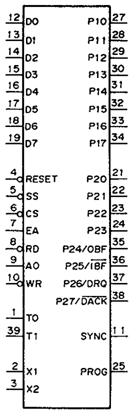

MISALLIANCE REGISTER
DATA DIRECTION REGISTER
PORT A REGISTER
11-14
A0-A7
D6/INT2 35
D5/CK 34
D4/Rx 33
D3/Tx 32
D2 31
D1 30
D0 29
PORT D REGI-STER
DATA DIRECTION REGISTER
DATA DIRECTION REGISTER
PORT B REGISTER
12-19
B0-B7
SERIAL DATA REGISTER
SERIAL CONTROL REGISTER
SERIAL STATUS REGISTER
DATA DIRECTION REGISTER
PORT C REGISTER
28-21
C0-C7
TIMER CONTROL
TIMER 37
PRE-SCALER 7-BIT
TIMER/COUNTER 8-BIT
ROM
U0; 2048 BYTES
V0; 4096 BYTES
XTAL 38
EXTAL 39
OSCILLATOR
RAM
U0; 128 BYTES
V0; 192 BYTES
STBY 36
INT 2
NUM 3
RES 1
CPU CONTROL
CENTRAL PROCESSING UNIT (CPU)
ARITHMETIC LOGIC UNIT (ALU)
ACCUMULATOR 8-BIT A
CONDITION CORD REGISTER 5-BIT CC
PROGRAM COUNTER HIGH 6-BIT PCH
INDEX REGISTER 8-BIT X
STACK POINTER 6-BIT SP
PROGRAM COUNTER LOW 8-BIT PCL

P8742AH (INTEL)

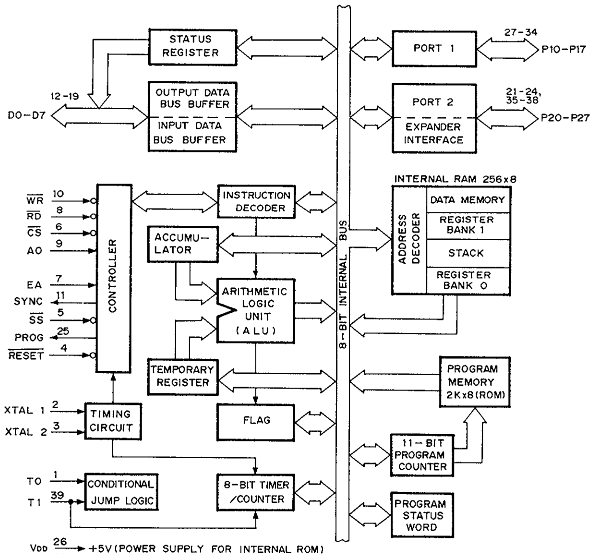
N-MOS SINGLE CHIP 8-BIT MICROCOMPUTER

– TOP VIEW –


Vcc (+5V) 40
T0 IN 1
X1 IN 2
X2 IN 3
RESET IN 4
SS IN 5
CS IN 6
EA IN 7
RD IN 8
A0 IN 9
WR IN 10
SYNC OUT 11
D0 IN/OUT 12
D1 IN/OUT 13
D2 IN/OUT 14
D3 IN/OUT 15
D4 IN/OUT 16
D5 IN/OUT 17
D6 IN/OUT 18
D7 IN/OUT 19
20 GND
39 T1 IN
38 P27/DACK IN/OUT
37 P26/DRQ IN/OUT
36 P25/IBF IN/OUT
35 P24/OBF IN/OUT
34 P17 IN/OUT
33 P16 IN/OUT
32 P15 IN/OUT
31 P14 IN/OUT
30 P13 IN/OUT
29 P12 IN/OUT
28 P11 IN/OUT
27 P10 IN/OUT
VDD (+5V) 26
25 PROG OUT
24 P23 IN/OUT
23 P22 IN/OUT
22 P21 IN/OUT
21 P20 IN/OUT


12 D0
13 D1
14 D2
15 D3
16 D4
17 D5
18 D6
19 D7
4 RESET
5 SS
6 CS
7 EA
8 RD
9 A0
10 WR
1 T0
39 T1
2 X1
3 X2
P10 27
P11 28
P12 29
P13 30
P14 31
P15 32
P16 33
P17 34
P20 21
P21 22
P22 23
P23 24
P24/OBF 35
P25/IBF 36
P26/DRQ 37
P27/DACK 38
SYNC 11
PROG 25

D0-D7; DATA INPUTS/OUTPUTS
$\overline{\text{SS}}$; SINGLE STEP INPUT
$\overline{\text{CS}}$; CHIP SELECT INPUT
EA; EXTERNAL ADDRESS INPUT
$\overline{\text{RD}}$; READ STROBE INPUT
A0; ADDRESS 0 INPUT
$\overline{\text{WR}}$; WRITE STROBE INPUT
T0,T1; TEST INPUTS
X1, X2; CRYSTAL
PROG; STROBE PULSE OUTPUT/PROGRAM PULSE INPUT
P10-P17; INPUT/OUTPUT PORT1
P20-P27; INPUT/OUTPUT PORT2
OBF; OUTPUT BUFFER FULL FLAG OUTPUT
$\overline{\text{IBF}}$; INPUT BUFFER FULL FLAG OUTPUT
DRQ; DIRECT MEMORY ACCESS REQUEST OUTPUT
$\overline{\text{DACK}}$; DIRECT MEMORY ACCESS ACKNOWLEGDE OUTPUT

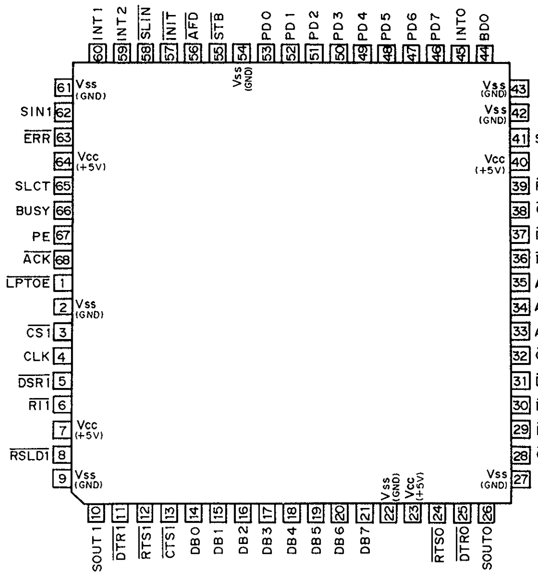

STATUS REGISTER
OUTPUT DATA BUS BUFFER
INPUT DATA BUS BUFFER
12-19
D0-D7
PORT 1
27-34
P10-P17
PORT 2
EXPANDER INTERFACE
21-24, 35-38
P20-P27
INTERNAL RAM 256x8
ADDRESS DECODER
DATA MEMORY
REGISTER BANK 1
STACK
REGISTER BANK 0
WR 10
RD 8
CS 6
A0 9
EA 7
SYNC 11
SS 5
PROG 25
RESET 4
CONTROLLER
INSTRUCTION DECODER
ACCUMU-LATOR
ARITHMETIC LOGIC UNIT (ALU)
TEMPORARY REGISTER
FLAG
8-BIT INTERNAL BUS
PROGRAM MEMORY 2Kx8(ROM)
11-BIT PROGRAM COUNTER
PROGRAM STATUS WORD
XTAL 1 2
XTAL 2 3
TIMING CIRCUIT
T0 1
T1 39
CONDITIONAL JUMP LOGIC
8-BIT TIMER /COUNTER

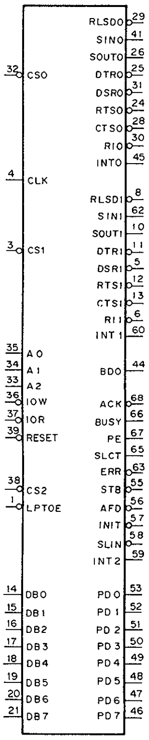
VDD 26 → +5V (POWER SUPPLY FOR INTERNAL ROM)
Vcc 40 → +5V

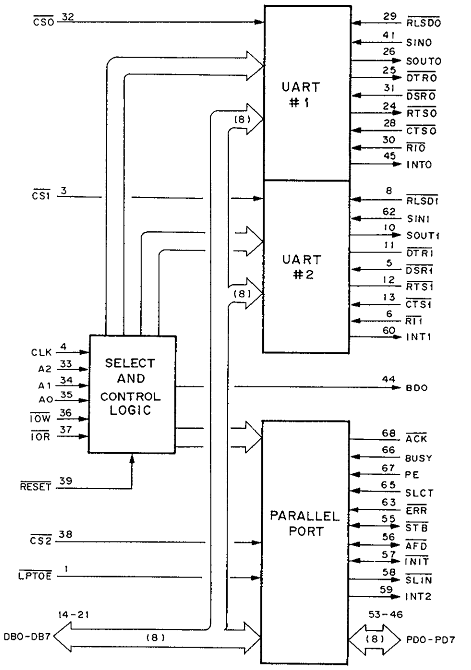
VL16C452QC (VLSI TECHNOLOGY)

C-MOS DUAL HIGH SPEED UART WITH CENTRONICS PRINTER PORT (PLCC PACKAGE)

– TOP VIEW –


60 INT1
59 INT2
58 SLIN
57 INIT
56 AFD
55 STB
54 Vss (GND)
53 PD0
52 PD1
51 PD2
50 PD3
49 PD4
48 PD5
47 PD6
46 PD7
45 INT0
44 BDO
61 Vss (GND)
SIN1 62
ERR 63
64 Vcc (+5V)
SLCT 65
BUSY 66
PE 67
ACK 68
LPTOE 1
2 Vss (GND)
CS1 3
CLK 4
DSR1 5
RI1 6
7 Vcc (+5V)
RSLD1 8
9 Vss (GND)
Vss (GND) 43
Vss (GND) 42
41 SIN0
Vcc (+5V) 40
39 RESET
38 CS2
37 IOR
36 IOW
35 A0
34 A1
33 A2
32 CS0
31 DSR0
30 RI0
29 RSLD0
28 CTS0
Vss (GND) 27
10 SOUT1
11 DTR1
12 RTS1
13 CTS1
14 DB0
15 DB1
16 DB2
17 DB3
18 DB4
19 DB5
20 DB6
21 DB7
22 Vss (GND)
23 Vcc (+5V)
24 RTS0
25 DTR0
26 SOUT0

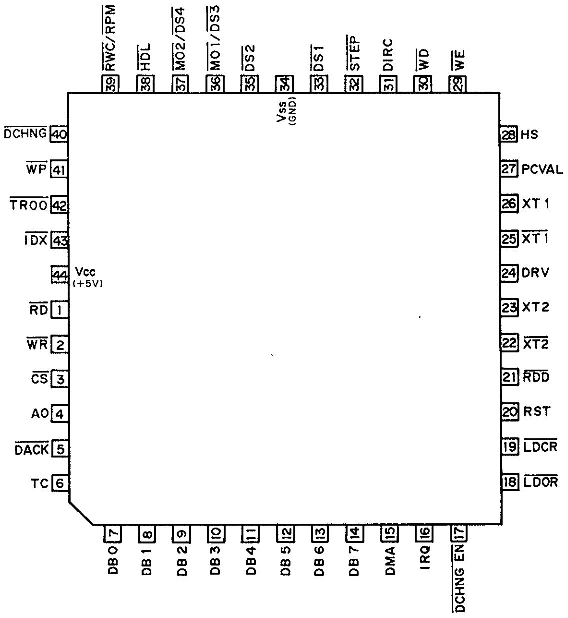

32 CS0
4 CLK
3 CS1
35 A0
34 A1
33 A2
36 IOW
37 IOR
39 RESET
38 CS2
1 LPTOE
14 DB0
15 DB1
16 DB2
17 DB3
18 DB4
19 DB5
20 DB6
21 DB7
RLSD0 29
SIN0 41
SOUT0 26
DTR0 25
DSR0 31
RTS0 24
CTS0 28
RI0 30
INT0 45
RLSD1 8
SIN1 62
SOUT1 10
DTR1 11
DSR1 5
RTS1 12
CTS1 13
RI1 6
INT1 60
BDO 44
ACK 68
BUSY 66
PE 67
SLCT 65
ERR 63
STB 55
AFD 56
INIT 57
SLIN 58
INT2 59
PD0 53
PD1 52
PD2 51
PD3 50
PD4 49
PD5 48
PD6 47
PD7 46

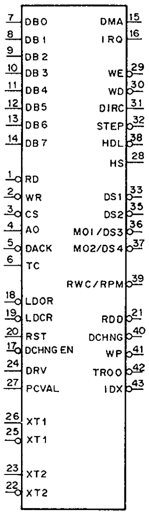

CS0 32
UART #1
(8)
29 RLSD0
41 SIN0
26 SOUT0
25 DTR0
31 DSR0
24 RTS0
28 CTS0
30 RI0
45 INT0
CS1 3
UART #2
8 RLSD1
62 SIN1
10 SOUT1
11 DTR1
5 DSR1
12 RTS1
13 CTS1
6 RI1
60 INT1
CLK 4
A2 33
A1 34
A0 35
IOW 36
IOR 37
SELECT AND CONTROL LOGIC
44 BDO
RESET 39
CS2 38
LPTOE 1
PARALLEL PORT
68 ACK
66 BUSY
67 PE
65 SLCT
63 ERR
55 STB
56 AFD
57 INIT
58 SLIN
59 INT2
14-21
DB0-DB7
(8)
53-46
PD0-PD7

A0 – A2 : ADDRESS LINES 0 TO 2, INPUTS
ACK : LINE PRINTER ACKNOWLEDGE INPUT
AFD : LINE PRINTER AUTOFEED INPUT/OUTPUT
BDO : BUS BUFFER OUTPUT
BUSY : LINE PRINTER BUSY INPUT
CLK : CLOCK INPUT
CS0, CS1 : CHIP SELECT INPUTS 0 AND 1 FOR SERIAL CHANNELS
CS3 : CHIP SELECT INPUT 3 FOR LINE PRINTER PORT
CTS0, CTS1 : CLEAR TO SEND INPUTS 0 AND 1
DB0 – DB7 : DATA BITS 0 TO 7, INPUTS/OUTPUTS
DSR0, DSR1 : DATA SET READY INPUTS 0 AND 1
DTR0, DTR1 : DATA TERMINAL READY LINES 0 AND 1
ERROR : LINE PRINTER ERROR INPUT
INIT : LINE PRINTER INITIALIZE INPUT/OUTPUT
INT0, INT1 : SERIAL CHANNEL INTERRUPT OUTPUTS 0 AND 1
INT2 : PRINTER PORT INTERRUPT OUTPUT
IOR : INPUT/OUTPUT READ STROBE INPUT
IOW : INPUT/OUTPUT WRITE STROBE INPUT
LPTOE : LINE PRINTER OUTPUT ENABLE INPUT
PD0 – PD7 : PARALLEL DATA BITS 0 TO 7, INPUTS/OUTPUTS
PE : LINE PRINTER PAPER EMPTY INPUT
RESET : RESET INPUT
RI0, RI1 : RING INDICATOR INPUTS 0 AND 1
RLSD0, RLSD1 : RECEIVE LINE SIGNAL DETECT INPUTS 0 AND 1
RTS0, RTS1 : REQUEST TO SEND OUTPUTS 0 AND 1
SIN0, SIN1 : SERIAL DATA INPUTS 0 AND 1
SLCT : LINE PRINTER SELECTED INPUT
SLIN : LINE PRINTER SELECT INPUT/OUTPUT
SOUT0, SOUT1 : SERIAL DATA OUTPUTS 0 AND 1
STB : LINE PRINTER STROBE INPUT/OUTPUT

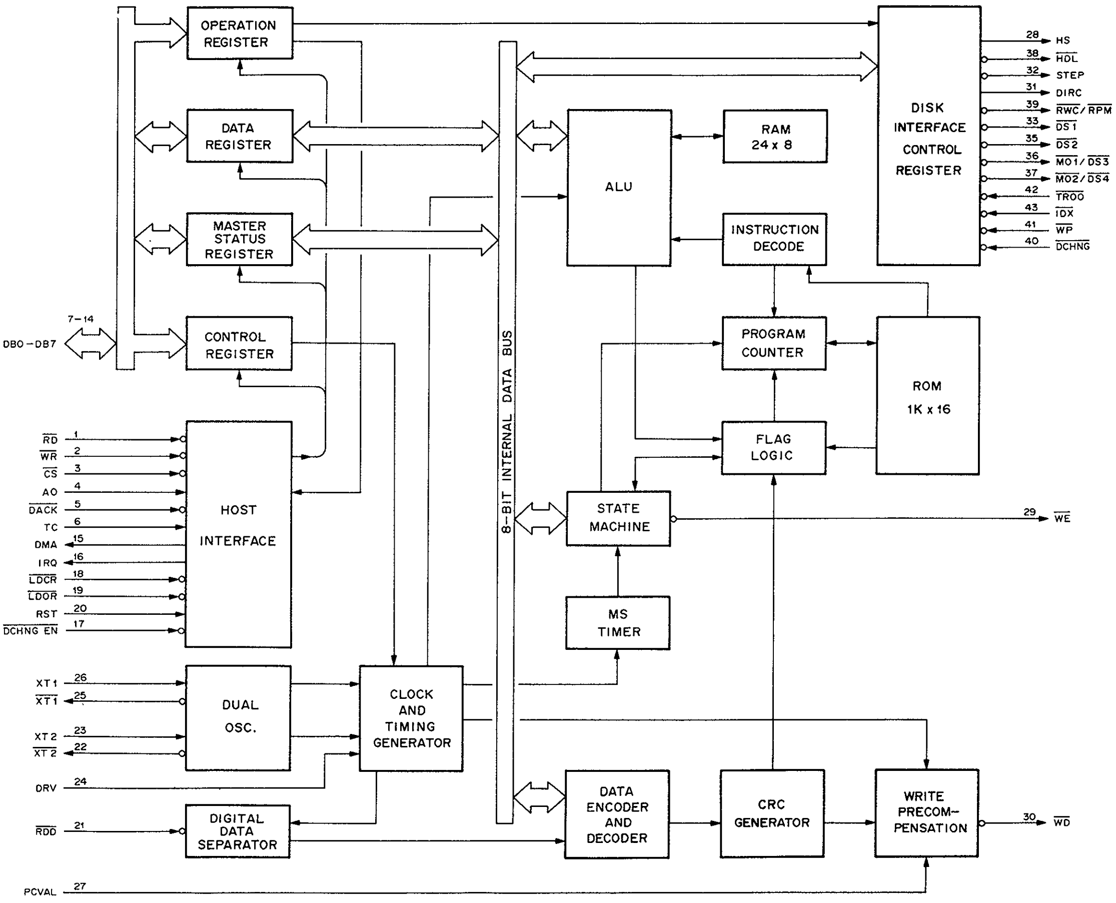
WD37C65BJM (WESTERN DIGITAL)

C-MOS FLOPPY-DISK SUBSYSTEM CONTROLLER (PLCC PACKAGE)
– TOP VIEW –


39 RWC/RPM
38 HDL
37 MO2/DS4
36 MO1/DS3
35 DS2
34 Vss (GND)
33 DS1
32 STEP
31 DIRC
30 WD
29 WE
DCHNG 40
WP 41
TR00 42
IDX 43
44 Vcc (+5V)
RD 1
WR 2
CS 3
A0 4
DACK 5
TC 6
28 HS
27 PCVAL
26 XT1
25 XT1
24 DRV
23 XT2
22 XT2
21 RDD
20 RST
19 LDCR
18 LDOR
7 DB0
8 DB1
9 DB2
10 DB3
11 DB4
12 DB5
13 DB6
14 DB7
15 DMA
16 IRQ
17 DCHNG EN

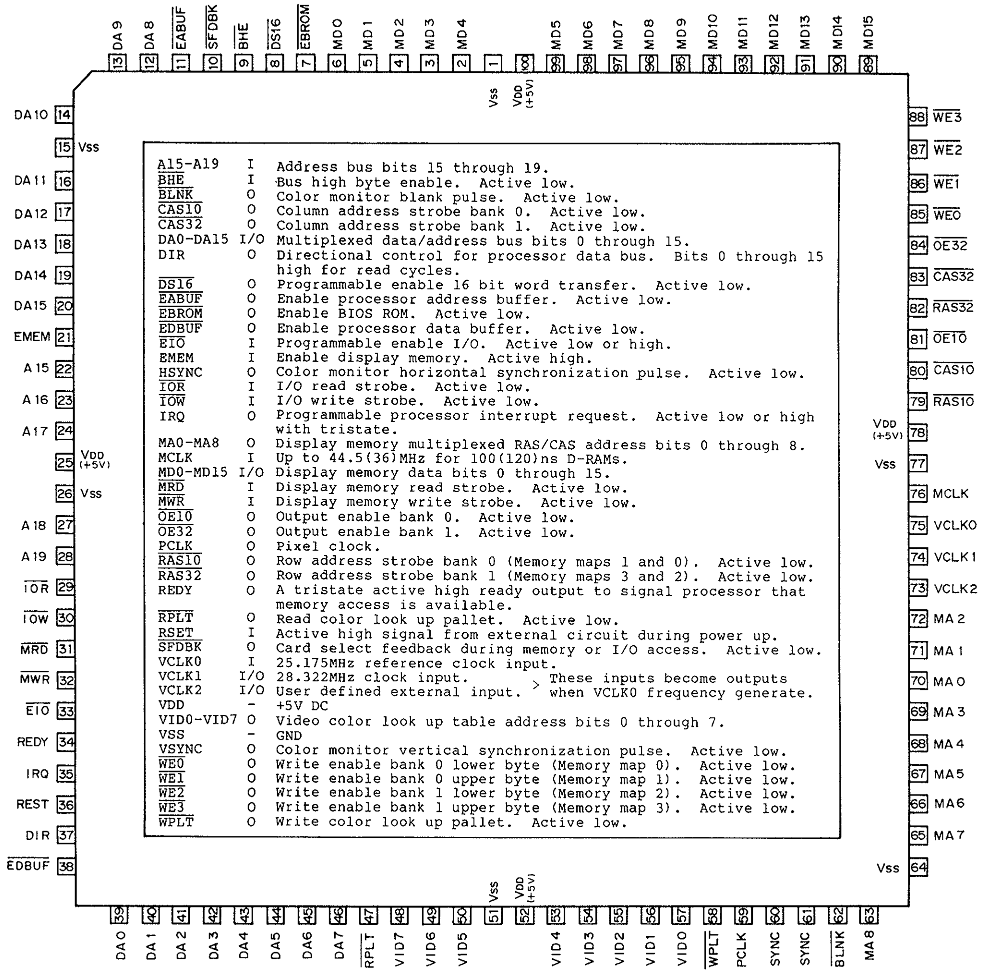

7 DB0
8 DB1
9 DB2
10 DB3
11 DB4
12 DB5
13 DB6
14 DB7
1 RD
2 WR
3 CS
4 A0
5 DACK
6 TC
18 LDOR
19 LDCR
20 RST
17 DCHNG EN
24 DRV
27 PCVAL
26 XT1
25 XT1
23 XT2
22 XT2
DMA 15
IRQ 16
WE 29
WD 30
DIRC 31
STEP 32
HDL 38
HS 28
DS1 33
DS2 35
MO1/DS3 36
MO2/DS4 37
RWC/RPM 39
RDD 21
DCHNG 40
WP 41
TR00 42
IDX 43

A0 ;	ADDRESS LINE, INPUT
CS ;	CHIP SELECT, INPUT
DACK ;	DMA ACKNOWLEDGE, INPUT
DB0-DB7 ;	DATA BUS LINES 0 thru 7, INPUTS/OUTPUTS
DCHNG ;	DISK CHANGE, INPUT
DCHNG EN ;	DISK CHANGE ENABLE, INPUT
DIRC ;	DIRECTION (INWARD/OUTWARD), OUTPUT
DMA ;	DIRECT MEMORY ACCESS, OUTPUT
DRV ;	DRIVE TYPE, INPUT
DS1-DS4 ;	DRIVE SELECTS 1 thru 4, OUTPUTS
HDL ;	HEAD LOADED, OUTPUT
HS ;	HEAD SELECT (SIDE 1/SIDE 0), OUTPUT
IDX ;	INDEX, INPUT
IRQ ;	INTERRUPT, OUTPUT
LDCR ;	LOAD CONTROL REGISTER, INPUT
LDOR ;	LOAD OPERATIONS REGISTER, INPUT
MO1,MO2 ;	MOTOR ON 1 and MOTOR ON 2, OUTPUTS
PCVAL ;	PRECOMPENSATION VALUE SELECT, INPUT
RD ;	READ, INPUT
RDD ;	READ DISK DATA, INPUT
RPM ;	REVOLUTIONS PER MINUTE, OUTPUT
RST ;	RESET, INPUT
RWC ;	REDUCED WRITE CURRENT, OUTPUT
STEP ;	STEP PULSE, OUTPUT
TC ;	TERMINAL COUNT, INPUT
TR00 ;	TRACK 00, INPUT
VCC ;	+5V DC
VSS ;	GROUND
WE ;	WRITE ENABLE, OUTPUT
WD ;	WRITE DATA, OUTPUT
WP ;	WRITE PROTECTED, INPUT
WR ;	WRITE, INPUT
XT1,XT1 ;	XTAL1 INPUT and OUTPUT
XT2,XT2 ;	XTAL2 INPUT and OUTPUT

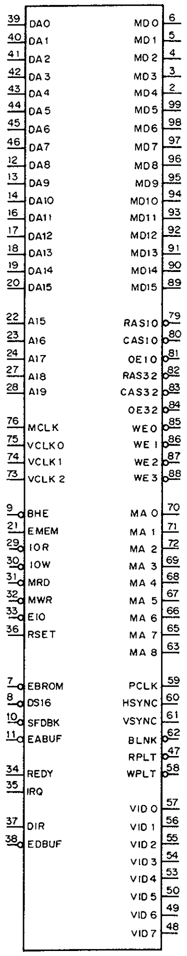

OPERATION REGISTER
DATA REGISTER
MASTER STATUS REGISTER
CONTROL REGISTER
7–14
DB0–DB7
HOST INTERFACE
RD 1
WR 2
CS 3
A0 4
DACK 5
TC 6
DMA 15
IRQ 16
LDCR 18
LDOR 19
RST 20
DCHNG EN 17
XT1 26
XT1 25
XT2 23
XT2 22
DUAL OSC.
CLOCK AND TIMING GENERATOR
DRV 24
RDD 21
DIGITAL DATA SEPARATOR
PCVAL 27
8-BIT INTERNAL DATA BUS
ALU
RAM 24 x 8
INSTRUCTION DECODE
PROGRAM COUNTER
FLAG LOGIC
ROM 1K x 16
STATE MACHINE
MS TIMER
DATA ENCODER AND DECODER
CRC GENERATOR
WRITE PRECOM-PENSATION
DISK INTERFACE CONTROL REGISTER
28 HS
38 HDL
32 STEP
31 DIRC
39 RWC/RPM
33 DS1
35 DS2
36 MO1/DS3
37 MO2/DS4
42 TR00
43 IDX
41 WP
40 DCHNG
29 WE
30 WD

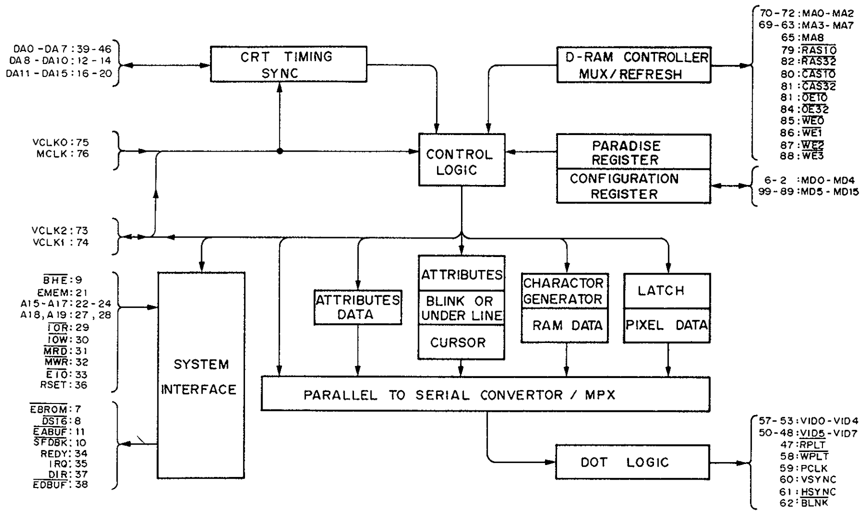
PVGA1A (PARADISE SYSTEMS)

C-MOS VIDEO GRAPHICS ARRAY (PLCC PACKAGE)
– TOP VIEW –


13 DA9
12 DA8
11 EABUF
10 SFDBK
9 BHE
8 DS16
7 EBROM
6 MD0
5 MD1
4 MD2
3 MD3
2 MD4
1 Vss
100 VDD (+5V)
99 MD5
98 MD6
97 MD7
96 MD8
95 MD9
94 MD10
93 MD11
92 MD12
91 MD13
90 MD14
89 MD15
DA10 14
15 Vss
DA11 16
DA12 17
DA13 18
DA14 19
DA15 20
EMEM 21
A15 22
A16 23
A17 24
25 VDD (+5V)
26 Vss
A18 27
A19 28
IOR 29
IOW 30
MRD 31
MWR 32
EIO 33
REDY 34
IRQ 35
REST 36
DIR 37
EDBUF 38
39 DA0
40 DA1
41 DA2
42 DA3
43 DA4
44 DA5
45 DA6
46 DA7
47 RPLT
48 VID7
49 VID6
50 VID5
51 Vss
52 VDD (+5V)
53 VID4
54 VID3
55 VID2
56 VID1
57 VID0
58 WPLT
59 PCLK
60 H SYNC
61 V SYNC
62 BLNK
63 MA8
88 WE3
87 WE2
86 WE1
85 WE0
84 OE32
83 CAS32
82 RAS32
81 OE10
80 CAS10
79 RAS10
VDD (+5V) 78
Vss 77
76 MCLK
75 VCLK0
74 VCLK1
73 VCLK2
72 MA2
71 MA1
70 MA0
69 MA3
68 MA4
67 MA5
66 MA6
65 MA7
Vss 64

A15-A19	I	Address bus bits 15 through 19.
$\overline{\mathrm{BHE}}$	I	Bus high byte enable. Active low.
$\overline{\mathrm{BLNK}}$	O	Color monitor blank pulse. Active low.
$\overline{\mathrm{CAS10}}$	O	Column address strobe bank 0. Active low.
$\overline{\mathrm{CAS32}}$	O	Column address strobe bank 1. Active low.
DA0-DA15	I/O	Multiplexed data/address bus bits 0 through 15.
DIR	O	Directional control for processor data bus. Bits 0 through 15 high for read cycles.
$\overline{\mathrm{DS16}}$	O	Programmable enable 16 bit word transfer. Active low.
$\overline{\mathrm{EABUF}}$	O	Enable processor address buffer. Active low.
$\overline{\mathrm{EBROM}}$	O	Enable BIOS ROM. Active low.
$\overline{\mathrm{EDBUF}}$	O	Enable processor data buffer. Active low.
$\overline{\mathrm{EIO}}$	I	Programmable enable I/O. Active low or high.
EMEM	I	Enable display memory. Active high.
$\overline{\mathrm{HSYNC}}$	O	Color monitor horizontal synchronization pulse. Active low.
$\overline{\mathrm{IOR}}$	I	I/O read strobe. Active low.
$\overline{\mathrm{IOW}}$	I	I/O write strobe. Active low.
IRQ	O	Programmable processor interrupt request. Active low or high with tristate.
MA0-MA8	O	Display memory multiplexed RAS/CAS address bits 0 through 8.
MCLK	I	Up to 44.5(36)MHz for 100(120)ns D-RAMs.
MD0-MD15	I/O	Display memory data bits 0 through 15.
$\overline{\mathrm{MRD}}$	I	Display memory read strobe. Active low.
$\overline{\mathrm{MWR}}$	I	Display memory write strobe. Active low.
$\overline{\mathrm{OE10}}$	O	Output enable bank 0. Active low.
$\overline{\mathrm{OE32}}$	O	Output enable bank 1. Active low.
PCLK	O	Pixel clock.
$\overline{\mathrm{RAS10}}$	O	Row address strobe bank 0 (Memory maps 1 and 0). Active low.
$\overline{\mathrm{RAS32}}$	O	Row address strobe bank 1 (Memory maps 3 and 2). Active low.
REDY	O	A tristate active high ready output to signal processor that memory access is available.
$\overline{\mathrm{RPLT}}$	O	Read color look up pallet. Active low.
RSET	I	Active high signal from external circuit during power up.
$\overline{\mathrm{SFDBK}}$	O	Card select feedback during memory or I/O access. Active low.
VCLK0	I	25.175MHz reference clock input.
VCLK1	I/O	28.322MHz clock input. > These inputs become outputs when VCLK0 frequency generate.
VCLK2	I/O	User defined external input.
VDD	-	+5V DC
VID0-VID7	O	Video color look up table address bits 0 through 7.
VSS	-	GND
$\overline{\mathrm{VSYNC}}$	O	Color monitor vertical synchronization pulse. Active low.
$\overline{\mathrm{WE0}}$	O	Write enable bank 0 lower byte (Memory map 0). Active low.
$\overline{\mathrm{WE1}}$	O	Write enable bank 0 upper byte (Memory map 1). Active low.
$\overline{\mathrm{WE2}}$	O	Write enable bank 1 lower byte (Memory map 2). Active low.
$\overline{\mathrm{WE3}}$	O	Write enable bank 1 upper byte (Memory map 3). Active low.
$\overline{\mathrm{WPLT}}$	O	Write color look up pallet. Active low.

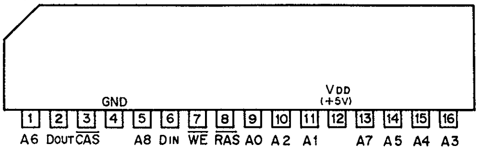

39 DA0
40 DA1
41 DA2
42 DA3
43 DA4
44 DA5
45 DA6
46 DA7
12 DA8
13 DA9
14 DA10
16 DA11
17 DA12
18 DA13
19 DA14
20 DA15
22 A15
23 A16
24 A17
27 A18
28 A19
76 MCLK
75 VCLK0
74 VCLK1
73 VCLK2
9 BHE
21 EMEM
29 IOR
30 IOW
31 MRD
32 MWR
33 EIO
36 RSET
7 EBROM
8 DS16
10 SFDBK
11 EABUF
34 REDY
35 IRQ
37 DIR
38 EDBUF
MD0 6
MD1 5
MD2 4
MD3 3
MD4 2
MD5 99
MD6 98
MD7 97
MD8 96
MD9 95
MD10 94
MD11 93
MD12 92
MD13 91
MD14 90
MD15 89
RAS10 79
CAS10 80
OE10 81
RAS32 82
CAS32 83
OE32 84
WE0 85
WE1 86
WE2 87
WE3 88
MA0 70
MA1 71
MA2 72
MA3 69
MA4 68
MA5 67
MA6 66
MA7 65
MA8 63
PCLK 59
HSYNC 60
VSYNC 61
BLNK 62
RPLT 47
WPLT 58
VID0 57
VID1 56
VID2 55
VID3 54
VID4 53
VID5 50
VID6 49
VID7 48

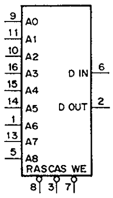

DA0-DA7 : 39-46
DA8-DA10 : 12-14
DA11-DA15 : 16-20
CRT TIMING SYNC
D-RAM CONTROLLER MUX/REFRESH
70-72 : MA0-MA2
69-63 : MA3-MA7
65 : MA8
79 : RAS10
82 : RAS32
80 : CAS10
81 : CAS32
81 : OE10
84 : OE32
85 : WE0
86 : WE1
87 : WE2
88 : WE3
VCLK0 : 75
MCLK : 76
CONTROL LOGIC
PARADISE REGISTER
CONFIGURATION REGISTER
6-2 : MD0-MD4
99-89 : MD5-MD15
VCLK2 : 73
VCLK1 : 74
BHE : 9
EMEM : 21
A15-A17 : 22-24
A18, A19 : 27, 28
IOR : 29
IOW : 30
MRD : 31
MWR : 32
EIO : 33
RSET : 36
EBROM : 7
DS16 : 8
EABUF : 11
SFDBK : 10
REDY : 34
IRQ : 35
DIR : 37
EDBUF : 38
SYSTEM INTERFACE
ATTRIBUTES DATA
ATTRIBUTES
BLINK OR UNDER LINE
CURSOR
CHARACTOR GENERATOR
RAM DATA
LATCH
PIXEL DATA
PARALLEL TO SERIAL CONVERTOR / MPX
DOT LOGIC
57-53 : VID0-VID4
50-48 : VID5-VID7
47 : RPLT
58 : WPLT
59 : PCLK
60 : VSYNC
61 : HSYNC
62 : BLNK

MB81256-10PSZ (FUJITSU) (ACCESS TIME = 100nS)

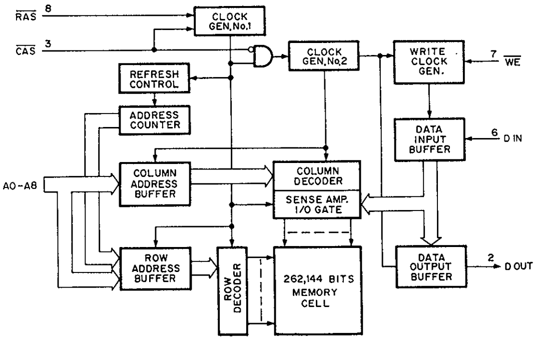
N-MOS 262,144-WORD BY 1-BIT DYNAMIC RAM

– SIDE VIEW –


GND
VDD (+5V)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
A6 DOUT CAS A8 DIN WE RAS A0 A2 A1 A7 A5 A4 A3


9 A0
11 A1
10 A2
16 A3
15 A4
14 A5
1 A6
13 A7
5 A8
D IN 6
D OUT 2
RAS CAS WE
8 3 7

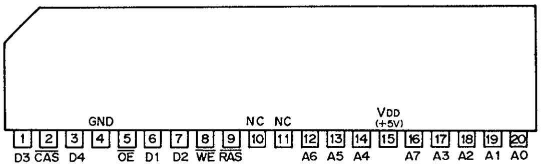
A0–A8 ; ADDRESS INPUT
$\overline{\text{CAS}}$; COLUMN ADDRESS STROBE
D IN ; DATA INPUT
DOUT ; DATA OUTPUT
$\overline{\text{RAS}}$; ROW ADDRESS STROBE
$\overline{\text{WE}}$; WRITE ENABLE

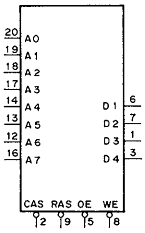

RAS 8
CAS 3
CLOCK GEN.No.1
CLOCK GEN.No.2
WRITE CLOCK GEN.
7 WE
REFRESH CONTROL
ADDRESS COUNTER
DATA INPUT BUFFER
6 D IN
A0–A8
COLUMN ADDRESS BUFFER
COLUMN DECODER
SENSE AMP. I/O GATE
ROW ADDRESS BUFFER
ROW DECODER
262,144 BITS MEMORY CELL
DATA OUTPUT BUFFER
2 D OUT

MB81464-10PSZ (FUJITSU) (ACCESS TIME = 100nS)

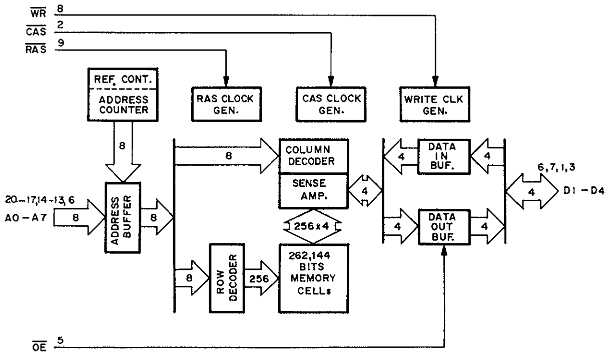
N-MOS 262,144-BIT (65,536x4) DYNAMIC RAM

– SIDE VIEW –


GND
NC NC
VDD (+5V)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
D3 CAS D4 OE D1 D2 WE RAS A6 A5 A4 A7 A3 A2 A1 A0


20 A0
19 A1
18 A2
17 A3
14 A4
13 A5
12 A6
16 A7
D1 6
D2 7
D3 1
D4 3
CAS RAS OE WE
2 9 5 8

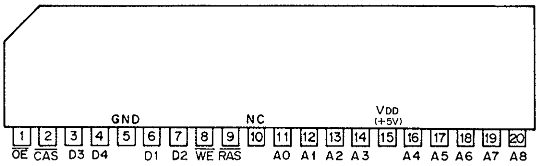
A0–A7 ; ADDRESS INPUT
$\overline{\text{CAS}}$; COLUMN ADDRESS STROBE
D1–D4 ; DATA IN/OUT
$\overline{\text{OE}}$; OUTPUT ENABLE
$\overline{\text{RAS}}$; ROW ADDRESS STROBE
$\overline{\text{WE}}$; WRITE ENABLE

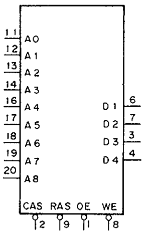

WR 8
CAS 2
RAS 9
REF. CONT.
ADDRESS COUNTER
RAS CLOCK GEN.
CAS CLOCK GEN.
WRITE CLK GEN.
8
20–17,14–13,6
A0–A7
ADDRESS BUFFER
COLUMN DECODER
SENSE AMP.
DATA IN BUF.
DATA OUT BUF.
4
6,7,1,3
D1–D4
256x4
ROW DECODER
256
262,144 BITS MEMORY CELLs
OE 5

MB81C4256-10PSZ (FUJITSU) (ACCESS TIME = 100nS)

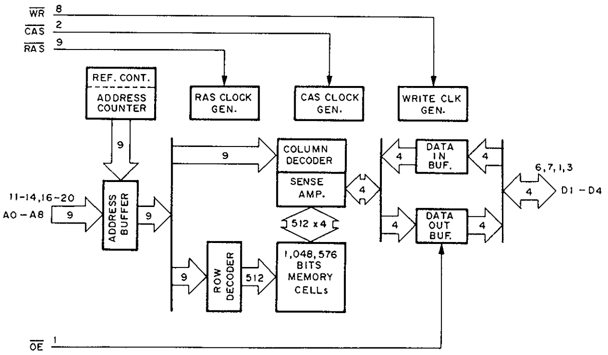
C-MOS 1,048,576-BIT (262,144x4) DYNAMIC RAM

– SIDE VIEW –


GND
NC
VDD (+5V)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
OE CAS D3 D4 D1 D2 WE RAS A0 A1 A2 A3 A4 A5 A6 A7 A8


11 A0
12 A1
13 A2
14 A3
16 A4
17 A5
18 A6
19 A7
20 A8
D1 6
D2 7
D3 3
D4 4
CAS RAS OE WE
2 9 1 8

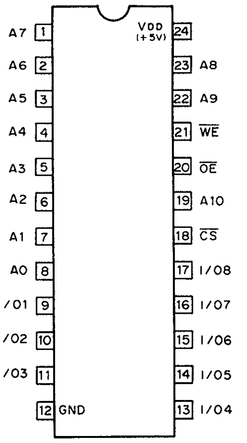
A0–A8 ; ADDRESS INPUT
$\overline{\text{CAS}}$; COLUMN ADDRESS STROBE
D1–D4 ; DATA IN/OUT
$\overline{\text{OE}}$; OUTPUT ENABLE
$\overline{\text{RAS}}$; ROW ADDRESS STROBE
$\overline{\text{WE}}$; WRITE ENABLE

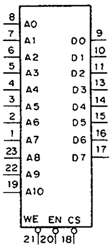

WR 8
CAS 2
RAS 9
REF. CONT.
ADDRESS COUNTER
RAS CLOCK GEN.
CAS CLOCK GEN.
WRITE CLK GEN.
9
11–14,16–20
A0–A8
ADDRESS BUFFER
COLUMN DECODER
SENSE AMP.
DATA IN BUF.
DATA OUT BUF.
4
6,7,1,3
D1–D4
512 x4
ROW DECODER
512
1,048,576 BITS MEMORY CELLs
OE 1

TMM2018AP-25 (TOSHIBA)

N-MOS 16384 (2048x8)-BIT STATIC RAM

– TOP VIEW –

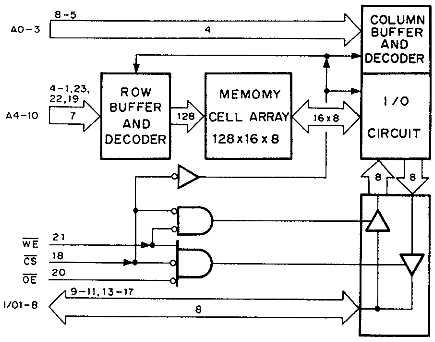

A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
I/O1 9
I/O2 10
I/O3 11
12 GND
VDD (+5V) 24
23 A8
22 A9
21 WE
20 OE
19 A10
18 CS
17 I/O8
16 I/O7
15 I/O6
14 I/O5
13 I/O4


8 A0
7 A1
6 A2
5 A3
4 A4
3 A5
2 A6
1 A7
23 A8
22 A9
19 A10
D0 9
D1 10
D2 11
D3 13
D4 14
D5 15
D6 16
D7 17
WE EN CS
21 20 18

INPUTS			FUNCTION
$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	
0	0	1	WRITE
0	1	0	READ
0	1	1	DISABLE (OUTPUT=HI-Z)
1	X	X	DISABLE (OUTPUT=HI-Z)

0 ;LOW LEVEL
1 ;HIGH LEVEL
X ;DON'T CARE
HI-Z ;HIGH IMPEDANCE

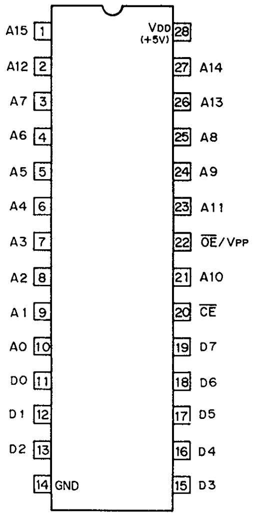
A0-10; ADDRESS INPUTS
I/O1-8; DATA INPUTS/OUTPUTS
$\overline{\text{CS}}$; CHIP SELECT INPUT
$\overline{\text{OE}}$; OUTPUT ENABLE INPUT
$\overline{\text{WE}}$; WRITE ENABLE INPUT

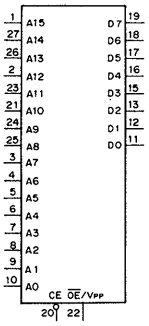

8–5
A0–3
4
COLUMN BUFFER AND DECODER
4–1,23,22,19
A4–10
7
ROW BUFFER AND DECODER
128
MEMOMY CELL ARRAY 128x16x8
16x8
I/O CIRCUIT
8
WE 21
CS 18
OE 20
9–11,13–17
I/O1–8
8

uPD27C512C-15 (NEC) (ACCESS TIME = 150nS)

C-MOS 512K (65,536x8 = 524,288)-BIT ONE TIME PROM

– TOP VIEW –

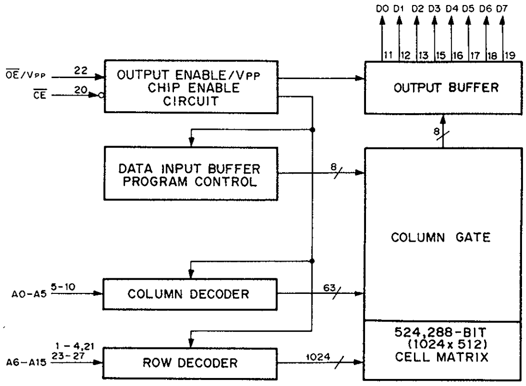

A15 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
D0 11
D1 12
D2 13
14 GND
VDD (+5V) 28
27 A14
26 A13
25 A8
24 A9
23 A11
22 $\overline{OE}$/VPP
21 A10
20 $\overline{CE}$
19 D7
18 D6
17 D5
16 D4
15 D3


1 A15
27 A14
26 A13
2 A12
23 A11
21 A10
24 A9
25 A8
3 A7
4 A6
5 A5
6 A4
7 A3
8 A2
9 A1
10 A0
D7 19
D6 18
D5 17
D4 16
D3 15
D2 13
D1 12
D0 11
CE $\overline{OE}$/VPP
20 22

A0–A15 ; ADDRESS INPUTS
$\overline{CE}$; CHIP ENABLE INPUT
D0–D7 ; DATA OUTPUTS
$\overline{OE}$; OUTPUT ENABLE INPUT
VPP ; PROGRAM POWER SUPPLY

An	$\overline{CE}$	$\overline{OE}$/Vpp	VDD	Dn	FUNCTION
AIN	0	0	+5V	DOUT	READ
AIN	0	1	+5V	HI-Z	OUTPUT DISABLE
X	1	X	+5V	HI-Z	STANDBY
AIN	0	+12.5V	+6V	DIN	PGM
AIN	0	0	+6V	DOUT	PGM VERIFY
X	1	+12.5V	+6V	HI-Z	PGM INH

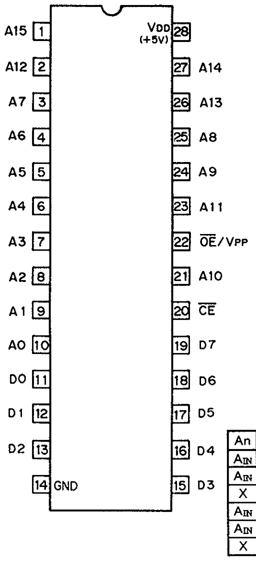
0 ; LOW LEVEL
1 ; HIGH LEVEL
HI–Z ; HIGH IMPEDANCE
X ; DON'T CARE

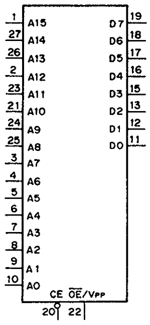

D0 D1 D2 D3 D4 D5 D6 D7
11 12 13 15 16 17 18 19
$\overline{OE}$/VPP 22
$\overline{CE}$ 20
OUTPUT ENABLE/VPP CHIP ENABLE CIRCUIT
OUTPUT BUFFER
8
DATA INPUT BUFFER PROGRAM CONTROL
8
COLUMN GATE
A0–A5 5–10
COLUMN DECODER
63
524,288-BIT (1024x 512) CELL MATRIX
A6–A15 1–4,21 23–27
ROW DECODER
1024

uPD27C512D-15 (NEC) (ACCESS TIME = 150nS)

C-MOS 512K (65,536x8 = 524,288)-BIT ERASABLE PROM

– TOP VIEW –

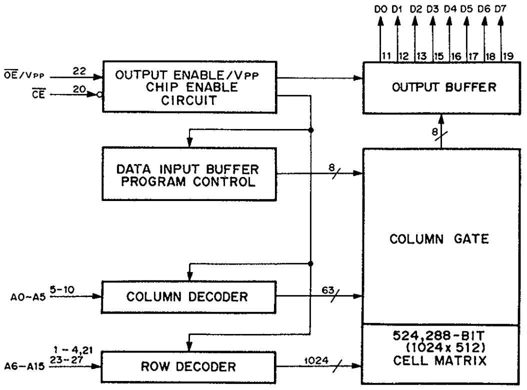

A15 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
D0 11
D1 12
D2 13
14 GND
VDD (+5V) 28
27 A14
26 A13
25 A8
24 A9
23 A11
22 $\overline{OE}$/VPP
21 A10
20 $\overline{CE}$
19 D7
18 D6
17 D5
16 D4
15 D3


1 A15
27 A14
26 A13
2 A12
23 A11
21 A10
24 A9
25 A8
3 A7
4 A6
5 A5
6 A4
7 A3
8 A2
9 A1
10 A0
D7 19
D6 18
D5 17
D4 16
D3 15
D2 13
D1 12
D0 11
CE $\overline{OE}$/VPP
20 22

A0 – A15 : ADDRESS INPUTS
$\overline{CE}$: CHIP ENABLE INPUT
D0 – D7 : DATA OUTPUTS
$\overline{OE}$: OUTPUT ENABLE INPUT
VPP : PROGRAM POWER SUPPLY

An	$\overline{CE}$	$\overline{OE}$/VPP	VDD	Dn	FUNCTION
AIN	0	0	+5V	DOUT	READ
AIN	0	1	+5V	HI-Z	OUTPUT DISABLE
X	1	X	+5V	HI-Z	STANDBY
AIN	0	+12.5V	+6V	DIN	PGM
AIN	0	0	+6V	DOUT	PGM VERIFY
X	1	+12.5V	+6V	HI-Z	PGM INH

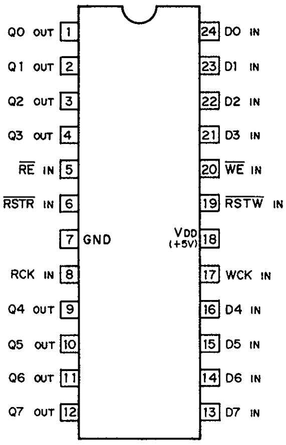
0 : LOW LEVEL
1 : HIGH LEVEL
X : DON'T CARE
HI-Z : HIGH IMPEDANCE

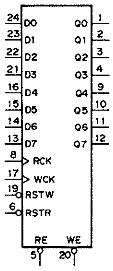

D0 D1 D2 D3 D4 D5 D6 D7
11 12 13 15 16 17 18 19
$\overline{OE}$/VPP 22
$\overline{CE}$ 20
OUTPUT ENABLE/VPP CHIP ENABLE CIRCUIT
OUTPUT BUFFER
8
DATA INPUT BUFFER PROGRAM CONTROL
8
COLUMN GATE
A0–A5 5–10
COLUMN DECODER
63
524,288-BIT (1024x 512) CELL MATRIX
A6–A15 1 – 4,21 23–27
ROW DECODER
1024

uPD42102G-3 (NEC) (ACCESS TIME = 21nS) FLAT PACKAGE

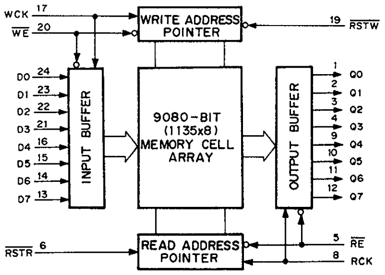
C-MOS 9080-BIT (1135x8) FIFO MEMORY

- TOP VIEW -


Q0 OUT 1
Q1 OUT 2
Q2 OUT 3
Q3 OUT 4
RE IN 5
RSTR IN 6
7 GND
RCK IN 8
Q4 OUT 9
Q5 OUT 10
Q6 OUT 11
Q7 OUT 12
24 D0 IN
23 D1 IN
22 D2 IN
21 D3 IN
20 WE IN
19 RSTW IN
VDD (+5V) 18
17 WCK IN
16 D4 IN
15 D5 IN
14 D6 IN
13 D7 IN


24 D0
23 D1
22 D2
21 D3
16 D4
15 D5
14 D6
13 D7
8 RCK
17 WCK
19 RSTW
6 RSTR
Q0 1
Q1 2
Q2 3
Q3 4
Q4 9
Q5 10
Q6 11
Q7 12
RE 5
WE 20

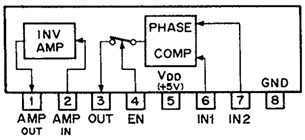
D0-7; DATA INPUTS
Q0-7; DATA OUTPUTS
WCK; WRITE CLOCK INPUT
RCK; READ CLOCK INPUT
$\overline{\text{WE}}$; WRITE ENABLE INPUT
$\overline{\text{RE}}$; READ ENABLE INPUT
$\overline{\text{RSTW}}$; RESET WRITE INPUT
$\overline{\text{RSTR}}$; RESET READ INPUT


WCK 17
WE 20
WRITE ADDRESS POINTER
19 RSTW
D0 24
D1 23
D2 22
D3 21
D4 16
D5 15
D6 14
D7 13
INPUT BUFFER
9080-BIT (1135x8) MEMORY CELL ARRAY
OUTPUT BUFFER
1 Q0
2 Q1
3 Q2
4 Q3
9 Q4
10 Q5
11 Q6
12 Q7
RSTR 6
READ ADDRESS POINTER
5 RE
8 RCK

CX23065 (SONY)

N-MOS PHASE COMPARATOR WITH INVERSION AMPLIFIER

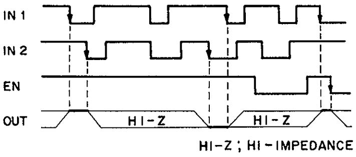
- PRINTED SIDE VIEW -


INV AMP
PHASE COMP
VDD (+5V)
GND
1 AMP OUT
2 AMP IN
3 OUT
4 EN
5
6 IN1
7 IN2
8

EN	OUT
1	ACTIVE
0	HIGH IMPEDANCE

1; HIGH LEVEL
0; LOW LEVEL

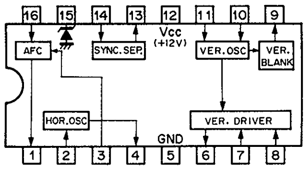
TIMING CHART



LA7801 (SANYO)

SYNCHRO. DEFLECTION CIRCUIT FOR COLOR TV

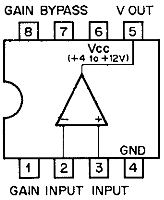
- TOP VIEW -


16 15 14 13 12 11 10 9
AFC
SYNC. SEP.
Vcc (+12V)
VER. OSC
VER. BLANK
HOR. OSC
VER. DRIVER
GND
1 2 3 4 5 6 7 8

LM386N (NS)

LOW VOLTAGE AUDIO POWER AMPLIFIER

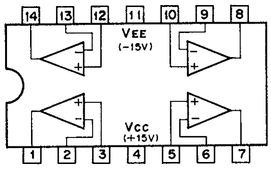
- TOP VIEW -


GAIN BYPASS
V OUT
8 7 6 5
Vcc (+4 to +12V)
GND
1 2 3 4
GAIN INPUT INPUT

TL084CN (TI)

OPERATIONAL AMPLIFIER
(J FET-INPUT)

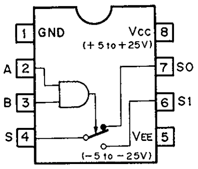
- TOP VIEW -

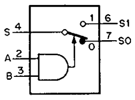

14 13 12 11 10 9 8
VEE (-15V)
Vcc (+15V)
1 2 3 4 5 6 7

TL601CPS (TI) FLAT PACKAGE

P-MOS ANALOG SWITCH

- TOP VIEW -


1 GND
A 2
B 3
S 4
Vcc (+5 to +25V) 8
7 SO
6 S1
VEE 5
(-5 to -25V)


S 4
A 2
B 3
1
0
6 S1
7 SO

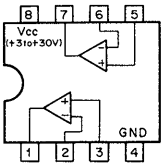
CONT	IN	ON CHANNEL
A	B	
0	0	SO
0	1	SO
1	0	SO
1	1	S1

0; LOW LEVEL
1; HIGH LEVEL

uPC358C (NEC)
uPC358G2 (NEC) FLAT PACKAGE

DUAL OPERATIONAL AMPLIFIERS

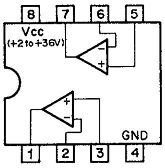
- TOP VIEW -


8 7 6 5
Vcc (+3 to +30V)
GND
1 2 3 4

uPC393C (NEC)

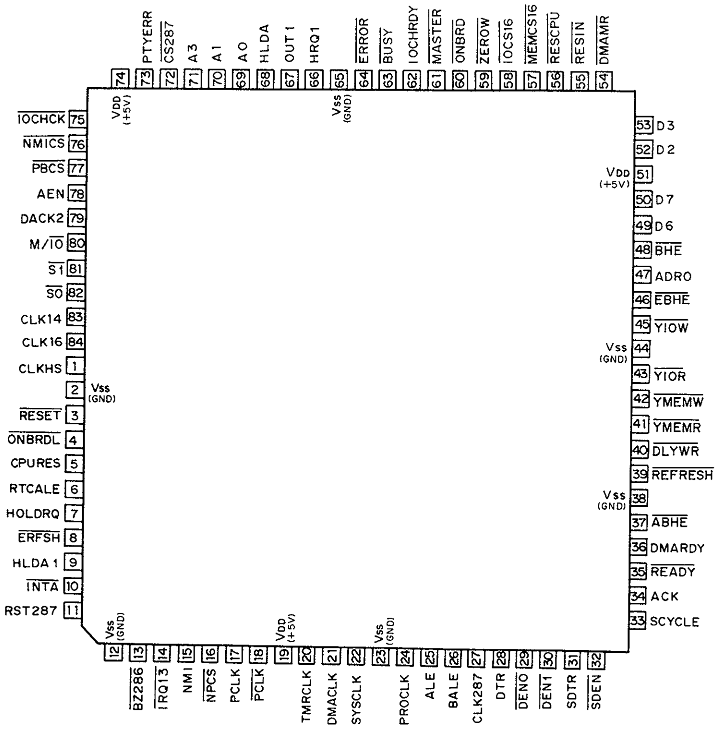
VOLTAGE COMPARATOR

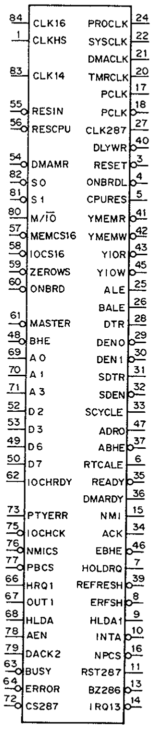
- TOP VIEW -


8 7 6 5
Vcc (+2 to +36V)
GND
1 2 3 4

FE3001 (FARADAY ELECTRONICS)

C-MOS AT CONTROL LOGIC (PLCC PACKAGE)
– TOP VIEW –

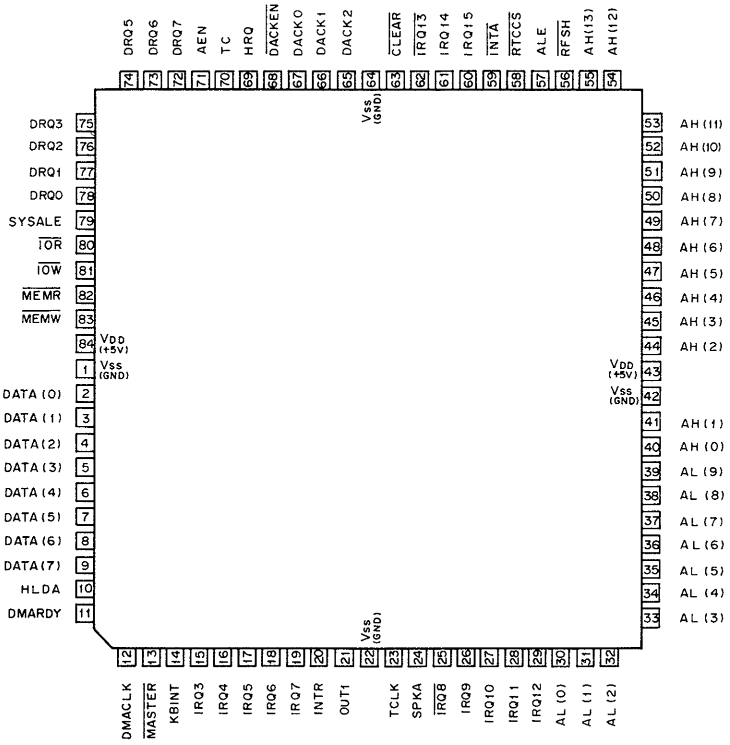

74 VDD (+5V)
73 PTYERR
72 CS287
71 A3
70 A1
69 A0
68 HLDA
67 OUT1
66 HRQ1
65 Vss (GND)
64 ERROR
63 BUSY
62 IOCHRDY
61 MASTER
60 ONBRD
59 ZEROW
58 IOCS16
57 MEMCS16
56 RESCPU
55 RESIN
54 DMAMR
75 IOCHCK
76 NMICS
77 PBCS
78 AEN
79 DACK2
80 M/IO
81 S1
82 S0
83 CLK14
84 CLK16
1 CLKHS
2 Vss (GND)
3 RESET
4 ONBRDL
5 CPURES
6 RTCALE
7 HOLDRQ
8 ERFSH
9 HLDA 1
10 INTA
11 RST287
12 Vss (GND)
13 BZ286
14 IRQ13
15 NMI
16 NPCS
17 PCLK
18 PCLK
19 VDD (+5V)
20 TMRCLK
21 DMACLK
22 SYSCLK
23 Vss (GND)
24 PROCLK
25 ALE
26 BALE
27 CLK287
28 DTR
29 DEN0
30 DEN1
31 SDTR
32 SDEN
53 D3
52 D2
51 VDD (+5V)
50 D7
49 D6
48 BHE
47 ADR0
46 EBHE
45 YIOW
44 Vss (GND)
43 YIOR
42 YMEMW
41 YMEMR
40 DLYWR
39 REFRESH
38 Vss (GND)
37 ABHE
36 DMARDY
35 READY
34 ACK
33 SCYCLE

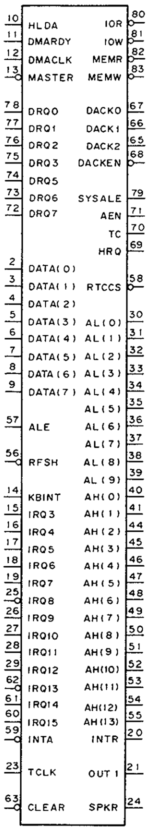

84 CLK16
1 CLKHS
83 CLK14
55 RESIN
56 RESCPU
54 DMAMR
82 S0
81 S1
80 M/IO
57 MEMCS16
58 IOCS16
59 ZEROWS
60 ONBRD
61 MASTER
48 BHE
69 A0
70 A1
71 A3
52 D2
53 D3
49 D6
50 D7
62 IOCHRDY
73 PTYERR
75 IOCHCK
76 NMICS
77 PBCS
66 HRQ1
67 OUT1
68 HLDA
78 AEN
79 DACK2
63 BUSY
64 ERROR
72 CS287
PROCLK 24
SYSCLK 22
DMACLK 21
TMRCLK 20
PCLK 17
PCLK 18
CLK287 27
DLYWR 40
RESET 3
ONBRDL 4
CPURES 5
YMEMR 41
YMEMW 42
YIOR 43
YIOW 45
ALE 25
BALE 26
DTR 28
DEN0 29
DEN1 30
SDTR 31
SDEN 32
SCYCLE 33
ADR0 47
ABHE 37
RTCALE 6
READY 35
DMARDY 36
NMI 15
ACK 34
EBHE 46
HOLDRQ 7
REFRESH 39
ERFSH 8
HLDA1 9
INTA 10
NPCS 16
RST287 11
BZ286 13
IRQ13 14

A0,A1,A3	I	Local 80286 address bus lines 0, 1 and 3.
ABHE	O	High byte enable for devices on local bus.
ACK	O	DMA acknowledge signal to the PC/AT bus.
ADR0	IO	Low byte enable. During a CPU cycle, A0 (pin 69) is latched with ALE (pin 25).
AEN	I	DMA cycle enable from FE3010B.
ALE	O	Local address latch enable.
BALE	O	Bus address latch enable (Programmable).
BHE	IO	High byte enable from 80286. Output during master and DMA cycle for memory control use.
BUSY	I	80287 co-processor busy.
BZ286	O	80287 co-processor busy signal to 80286.
CLK14	I	14.318MHz clock input used to derive TRMCLK, PCLK, PCLK (pins 20, 17, 18).
CLK16	I	16MHz clock input. This provides the low-speed CPU clock for 8MHz operation. When this pin is pulled high, ½CLKHS (pin 1) is used.
CLK287	O	Clock for 80287 co-processor.
CLKHS	I	High-speed clock input (40MHz max). This provides the high-speed clock when selected. When CLK16(pin 84) is pulled high, this input (divided by 2) is used as low-speed clock.
CPURES	O	Reset to 80286.
CS287	I	80287 co-processor select decode (ports 0FxH).
D2, D3	I	Peripheral data bus bits 2 and 3.
D6, D7	IO	Peripheral data bus bits 6 and 7.
DACK2	I	DMA acknowledge bit 2. 16-bit DMA acknowledge from FE3010B.
DEN0	O	Low byte data enable to data buffers.
DEN1	O	High byte data enable to data buffers.
DLYWR	IO	YIOW (pin 45) delayed to FE3010B, active edge delayed one PROCLK (pin 24). Input from FE3010B in during DMA to generate YIOW.
DMACLK	O	Software selectable clock for DMA to FE3010B.
DMAMR	I	DMA memory read from DMA controller.
DMARDY	O	End DMA cycle to FE3010B.
DTR	O	Data direction to data buffers.
EBHE	IO	High byte enable to expansion bus.
ERFSH	O	Enable refresh address signal to FE3010B. Puts refresh address on address bus.
ERROR	I	Error from 80287 co-processor.
HLDA	I	Hold acknowledge from 80286 for a request for the bus from DMA controller.
HLDA1	O	DMA hold acknowledge signal to FE3010B.
HOLDRQ	O	Hold request to 80286 for DMA or refresh.
HRQ1	I	Hold request from DMA controller in FE3010B.
INTA	O	Interrupt acknowledge to FE3010B.
IOCHCK	I	Error from PC/AT bus.
IOCHRDY	I	Current us cycle may complete. May be used to extend CPU, DMA, or refresh cycles.
IOCS16	I	16-bit I/O transfer on PC/AT bus.
IRQ13	O	Interrupt request 13 for 80287 error to FE3010B.
MASTER	I	Master on expansion bus has bus control.
MEMCS16	I	16-bit memory transfer on PC/AT bus.
M/IO	I	80286 memory or I/O select. High indicates memory cycle, low indicates I/O cycle.
NMI	O	Non-maskable interrupt to 80286. Generated in response to parity error or bus IOCHCK.
NMICS	I	NMI port enable decode (ports 7xH). Also used for programming bus control registers.
NPCS	O	80287 co-processor chip select (port 0F8H).
ONBRD	I	16-bit on board D-RAM memory or I/O device. Implies local memory on memory cycles and fast I/O bus timing for I/O cycles.
ONBRDL	O	ONBRD (pin 60) is latched with ALE (pin 25).
OUT1	I	Refresh timer input from FE3010B.
PBCS	I	Port B chip select decode (ports 61H, 63H).
PCLK	O	7.16MHz clock for keyboard controller.
PCLK	O	Inverted PCLK (pin 17).
PROCLK	O	Software selectable 80286 clock.
PTYERR	I	On board RAM parity error.
READY	O	Ready to 80286.
REFRESH	IO	Refresh cycle. Generated from timer channel 1 or externally from the bus.
RESCPU	I	80286 reset input from keyboard controller.
RESET	O	Rest to the system.
RESIN	I	System reset input.
RST287	O	Reset to 80287 co-processor (Write to I/O address 0F1H or system reset).
RTCALE	O	Real time clock address latch enable (port 70H).
S0, S1	I	80286 status lines 0 and 1.
SCYCLE	O	Latch low byte during byte swap read.
SDEN	O	Byte swap data enable to data buffers.
SDTR	O	Byte swap data direction to data buffers.
SYSCLK	O	System clock needed for bus timing.
TMRCLK	O	1.19MHz timer clock to FE3010B.
VDD1-3	-	Terminals of +5V supply.
VSS1-6	-	Terminals of ground.
YIOR	IO	I/O read. Input during HLDA cycle.
YIOW	IO	I/O write. Input during MASTER cycle.
YMEMR	IO	Memory read. Input during MASTER cycle.
YMEMW	IO	Memory write. Input during HLDA cycle.
ZEROWS	I	Zero wait state bus cycle.

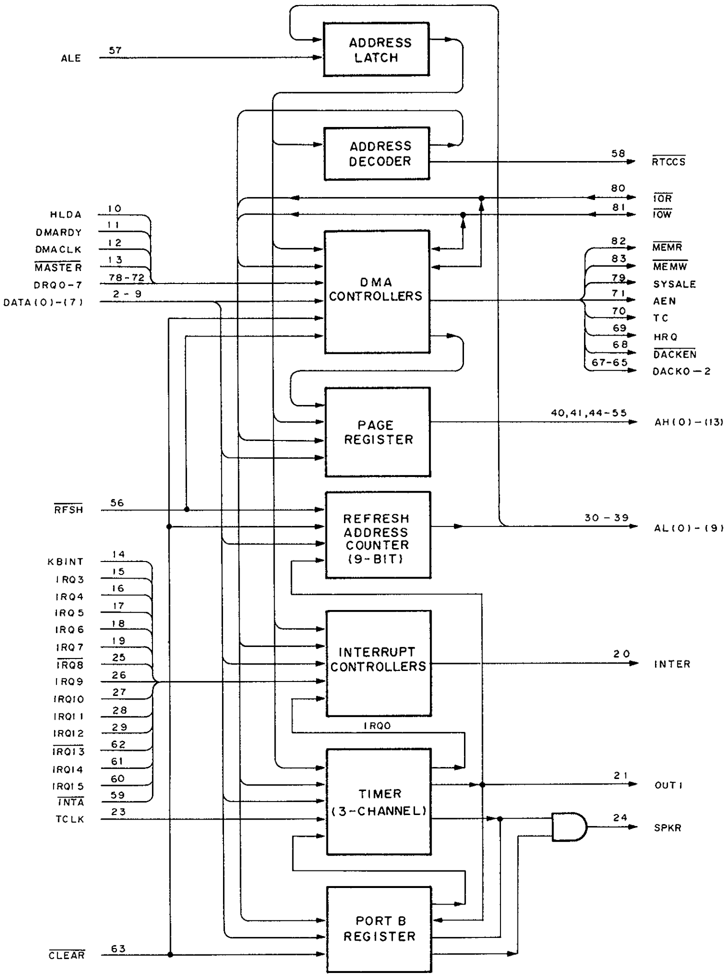
FE3010B (FARADAY ELECTRONICS)

C-MOS AT PERIPHERAL CONTROL LOGIC (PLCC PACKAGE)
– TOP VIEW –


DRQ5 74
DRQ6 73
DRQ7 72
AEN 71
TC 70
HRQ 69
DACKEN 68
DACK0 67
DACK1 66
DACK2 65
64 Vss (GND)
CLEAR 63
IRQ13 62
IRQ14 61
IRQ15 60
INTA 59
RTCCS 58
ALE 57
RFSH 56
AH(13) 55
AH(12) 54
DRQ3 75
DRQ2 76
DRQ1 77
DRQ0 78
SYSALE 79
IOR 80
IOW 81
MEMR 82
MEMW 83
84 VDD (+5V)
1 Vss (GND)
DATA (0) 2
DATA (1) 3
DATA (2) 4
DATA (3) 5
DATA (4) 6
DATA (5) 7
DATA (6) 8
DATA (7) 9
HLDA 10
DMARDY 11
12 DMACLK
13 MASTER
14 KBINT
15 IRQ3
16 IRQ4
17 IRQ5
18 IRQ6
19 IRQ7
20 INTR
21 OUT1
22 Vss (GND)
23 TCLK
24 SPKA
25 IRQ8
26 IRQ9
27 IRQ10
28 IRQ11
29 IRQ12
30 AL (0)
31 AL (1)
32 AL (2)
53 AH (11)
52 AH (10)
51 AH (9)
50 AH (8)
49 AH (7)
48 AH (6)
47 AH (5)
46 AH (4)
45 AH (3)
44 AH (2)
43 VDD (+5V)
42 Vss (GND)
41 AH (1)
40 AH (0)
39 AL (9)
38 AL (8)
37 AL (7)
36 AL (6)
35 AL (5)
34 AL (4)
33 AL (3)


10 HLDA
11 DMARDY
12 DMACLK
13 MASTER
78 DRQ0
77 DRQ1
76 DRQ2
75 DRQ3
74 DRQ5
73 DRQ6
72 DRQ7
2 DATA(0)
3 DATA(1)
4 DATA(2)
5 DATA(3)
6 DATA(4)
7 DATA(5)
8 DATA(6)
9 DATA(7)
57 ALE
56 RFSH
14 KBINT
15 IRQ3
16 IRQ4
17 IRQ5
18 IRQ6
19 IRQ7
25 IRQ8
26 IRQ9
27 IRQ10
28 IRQ11
29 IRQ12
62 IRQ13
61 IRQ14
60 IRQ15
59 INTA
23 TCLK
63 CLEAR
IOR 80
IOW 81
MEMR 82
MEMW 83
DACK0 67
DACK1 66
DACK2 65
DACKEN 68
SYSALE 79
AEN 71
TC 70
HRQ 69
RTCCS 58
AL(0) 30
AL(1) 31
AL(2) 32
AL(3) 33
AL(4) 34
AL(5) 35
AL(6) 36
AL(7) 37
AL(8) 38
AL(9) 39
AH(0) 40
AH(1) 41
AH(2) 44
AH(3) 45
AH(4) 46
AH(5) 47
AH(6) 48
AH(7) 49
AH(8) 50
AH(9) 51
AH(10) 52
AH(11) 53
AH(12) 54
AH(13) 55
INTR 20
OUT1 21
SPKR 24

AEN	O	DMA Address Enable. Signal to indicate that current bus is a DMA cycle.
AH(n)	O	Address lines 10 to 23 or Address High lines 0 to 13.
AL(n)	IO	Address lines 0 to 9 or Address Low lines 0 to 9.
ALE	I	Address Latch Enable.
CLEAR	I	CLEAR of the FE3010B.
DACK n	O	DMA ACKnowledge bits 0 to 2.
DACKEN	O	DMA ACKnowledge ENable. Signal to enable DACK bits 0 to 2 decodes.
DATA(n)	IO	DATA bits 0 to 7.
DMARDY	I	DMA ReaDY. Signal to indicate that DMA may complete its current cycle.
DMACLK	I	DMA CLocK.
DRQ n	I	DMA ReQuests of channels 0 to 3 and 5 to 7.
HLDA	I	HoLD Acknowledge. Acknowledge from CPU for a request for bus from DMA controller.
HRQ	O	DMA Hold ReQuest to CPU.
INTA	I	INTerrupt Acknowledge from CPU.
INTR	O	INTerrupt Request to CPU.
IOR	IO	I/O Read command.
IOW	IO	I/O Write command.
IRQ n	I	Interrupt ReQuests 3 to 7, 9 to 13, 14, and 15.
IRQ n	I	Interrupt ReQuests 8 and 13.
KBINT	I	KeyBoard INTerrupt.
MASTER	I	MASTER of bus. Signal to indicate that a master on expansion bus has control of bus.
MEMR	O	MEMory Read command.
MEMW	O	MEMory Write command.
OUT1	O	OUTput of timer channel 1.
RFSH	I	ReFreSH address. Signal to enable refresh address to address bus during a RAM refresh cycle.
RTCCS	O	Real Time Clock Chip Select.
SPKR	O	SPeaKeR.
SYSALE	O	SYStem Address Latch Enable. Signal to latch address in address latch.
TC	O	Terminal Count, DMA end of operation. Signal to indicate DMA contrller has finished its cycle.
TCLK	I	Timer CLocK. Approx. 1.19MHz clock for timer.
VDD	-	+5V Supply.
VSS	-	Ground.


ADDRESS LATCH
ADDRESS DECODER
DMA CONTROLLERS
PAGE REGISTER
REFRESH ADDRESS COUNTER (9-BIT)
INTERRUPT CONTROLLERS
TIMER (3-CHANNEL)
PORT B REGISTER
ALE 57
HLDA 10
DMARDY 11
DMACLK 12
MASTER 13
DRQ0-7 78-72
DATA(0)-(7) 2-9
RFSH 56
KBINT 14
IRQ3 15
IRQ4 16
IRQ5 17
IRQ6 18
IRQ7 19
IRQ8 25
IRQ9 26
IRQ10 27
IRQ11 28
IRQ12 29
IRQ13 62
IRQ14 61
IRQ15 60
INTA 59
TCLK 23
CLEAR 63
58 RTCCS
80 IOR
81 IOW
82 MEMR
83 MEMW
79 SYSALE
71 AEN
70 TC
69 HRQ
68 DACKEN
67-65 DACK0-2
40,41,44-55 AH(0)-(13)
30-39 AL(0)-(9)
20 INTER
IRQ0
21 OUT1
24 SPKR

FE3010B FUNCTION TABLES

ADDRESS DECODER FUNCTION (0; Low, 1; High, X; Don't care)

Address lines										Decodes	Hex Addresses
9	8	7	6	5	4	3	2	1	0		
0	0	0	0	0	X	X	X	X	X	DMA Controller #1 (CH0-3)	000H-01FH
0	0	0	0	1	X	X	X	X	X	Interrupt Controller Master	020H-03FH
0	0	0	1	0	X	X	X	X	X	Timer	040H-05FH
0	0	0	1	1	0	X	X	X	1	Port B	060H-06FH,odd
0	0	0	1	1	1	X	X	X	1	Real Time Clock (NRTCCS)	070H-07FH,odd
0	0	1	0	0	X	X	X	X	X	Pade register	080H-09FH
0	0	1	0	1	X	X	X	X	X	Interrupt Controller Slave	0A0H-0BFH
0	0	1	1	0	X	X	X	X	X	DMA Controller #2 (CH4-7)	0C0H-0DFH

DMA CONTROLLERs FUNCTION

AT Bus DMA Channel	DMA Controller	Transfer Type
#0	#1 Channel 0	8 bits
#1	#1 Channel 1	8 bits
#2	#1 Channel 2	8 bits
#3	#1 Channel 3	8 bits
#4	#2 Channel 0	Cascade #1
#5	#2 Channel 1	16 bits
#6	#2 Channel 2	16 bits
#7	#2 Channel 3	16 bits

PAGE REGISTER FUNCTION

I/O Address	Decode
087H	DMA Channel 0
083H	DMA Channel 1
081H	DMA Channel 2
082H	DMA Channel 3
08BH	DMA Channel 5
089H	DMA Channel 6
08AH	DMA Channel 7
08FH	Refresh

INTERRUPT CONTROLLERs FUNCTION

System interrupt	Interrupt Controller	Use
0	Master Level 0	Timer
1	Master Level 1	Keyboard
2	Master Level 2	Cascade Slave
3- 7	Master Levels 3 to 7	AT Bus
8	Slave Level 8	Real Time Clock
9-12	Slave Levels 9 to 12	AT Bus
13	Slave Level 13	Co-Processor
14,15	Slave Levels 14 and 15	AT Bus

TIMER FUNCTION

Timer Channel	Use
0	Time of Day(Interrupt)
1	Refresh Request
2	Speaker

DMA ACKNOWLEDGE FUNCTION

DACK Bits			DMA Channel Acknowledge
2	1	0	
0	0	0	#0
0	0	1	#1
0	1	0	#2
0	1	1	#3
1	0	0	Illegal
1	0	1	#5
1	1	0	#6
1	1	1	#7

0; Low, 1; High

DMA CLOCK FUNCTION

System Clock	DMA Clock
6MHz	3 or 6MHz
8MHz	4 or 8MHz
10MHz	5MHz

PORT B FUNCTION

Bit	Function
0	Gate for Timer Channel 2
1	Enable Speaker
2	reserved
3	reserved
4	Toggles on each Refresh (R)
5	OUT2 from Timer Channel 2 (R)

(R); Read only

Notes:

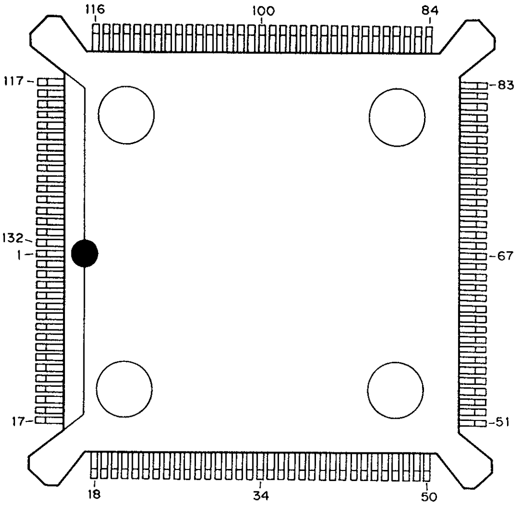
DMA Controller;
Refer to 8237.

Interrupt Controller;
Refer to 8259.

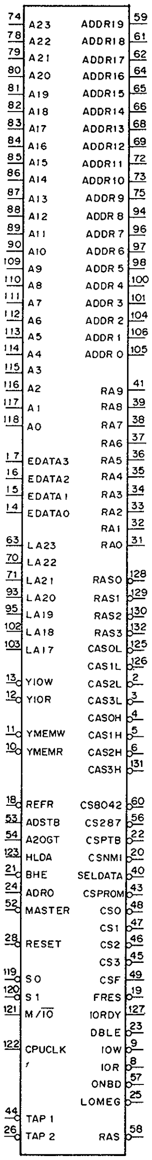
Timer; Refer to 8254.

FE3021 (FARADAY ELECTRONICS)

ADDRESS BUFFER AND MEMORY CONTROLLER
- TOP VIEW -


116
100
84
117
83
132
1
67
17
51
18
34
50

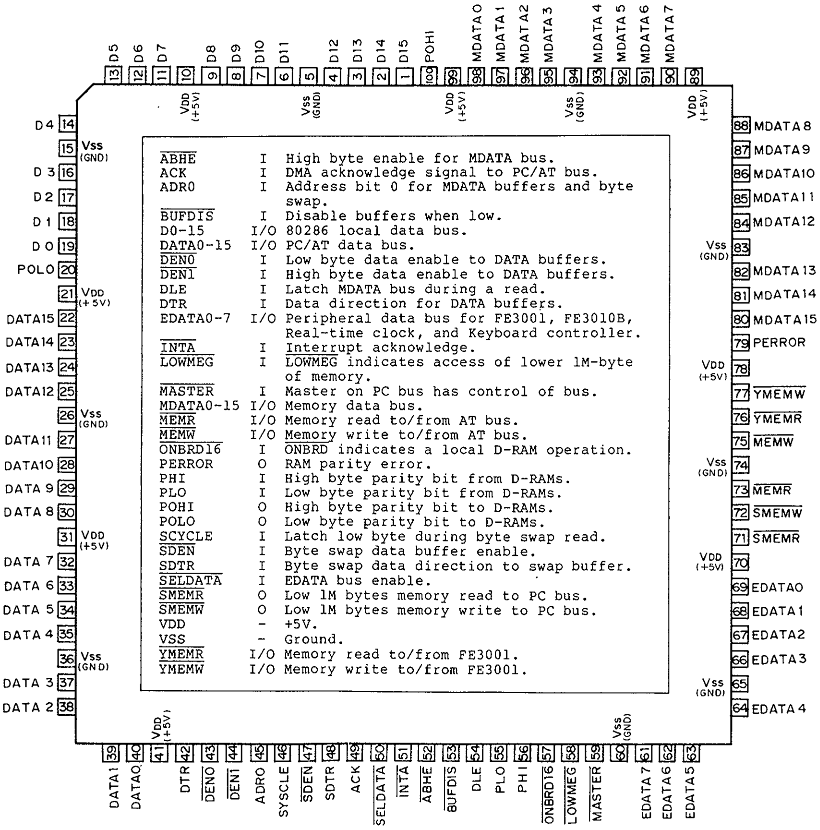
No.	SYMBOL	IO
1	VSS1	--
2	-CAS2L	O
3	-CAS3L	O
4	-CAS0H	O
5	-CAS1H	O
6	-CAS2H	O
7	VDD1	--
8	-IOR	IO
9	-IOW	IO
10	-YMEMR	I
11	-YMEMW	I
12	-YIOR	IO
13	-YIOW	IO
14	EDATA0	IO
15	EDATA1	IO
16	EDATA2	IO
17	EDATA3	IO
18	-REFR	I
19	-FRES	O
20	-CSNMI	O
21	-BHE	I
22	-CSPTB	O
23	-DBLE	O
24	ADR0	I
25	-LOMEG	O
26	-TAP2	I
27	VSS2	--
28	-RESET	I
29	VSS3	--
30	VDD2	--
31	RA0	O
32	RA1	O
33	RA2	O
34	RA3	O
35	RA4	O
36	RA5	O
37	RA6	O
38	RA7	O
39	RA8	O
40	-SELDATA	O
41	RA9	O
42	VSS4	--
43	-CSPROM	O
44	-TAP1	I
45	-CS3	O
46	-CS2	O
47	-CS1	O
48	-CS0	O
49	CSF	O
50	VDD2	--
51	VSS5	--
52	-MASTER	I
53	ADSTB	I
54	A20GT	I
55	VDD3	--
56	-CS287	O
57	-ONBD	O
58	-RAS	O
59	ADDR19	IO
60	-CS8042	O
61	ADDR18	IO
62	ADDR17	IO
63	LA23	IO
64	ADDR16	IO
65	ADDR15	IO
66	ADDR14	IO
67	VSS6	--
68	ADDR13	IO
69	ADDR12	IO
70	LA22	IO
71	LA21	IO
72	ADDR11	IO
73	ADDR10	IO
74	A23	IO
75	ADDR9	IO
76	VSS7	--
77	VDD4	IO
78	A22	IO
79	A21	IO
80	A20	IO
81	A19	IO
82	A18	IO
83	A17	IO
84	A16	IO
85	A15	IO
86	A14	IO
87	A13	IO
88	A12	IO
89	A11	IO
90	A10	IO
91	VSS8	--
92	VDD5	--
93	LA20	IO
94	ADDR8	IO
95	LA19	IO
96	ADDR7	IO
97	ADDR6	IO
98	ADDR5	IO
99	VSS9	--
100	ADDR4	IO
101	ADDR3	IO
102	LA18	IO
103	LA17	IO
104	ADDR2	IO
105	ADDR0	IO
106	ADDR1	IO
107	VDD6	--
108	VSS10	--
109	A9	IO
110	A8	IO
111	A7	IO
112	A6	IO
113	A5	IO
114	A4	IO
115	A3	IO
116	A2	IO
117	A1	IO
118	A0	IO
119	-S0	I
120	-S1	I
121	M/-IO	I
122	CPUCLK	I
123	HLDA	I
124	VSS11	--
125	-CAS0L	O
126	-CAS1L	O
127	IORDY	O
128	-RAS0	O
129	-RAS1	O
130	-RAS2	O
131	-CAS3H	O
132	-RAS3	O


74 A23
78 A22
79 A21
80 A20
81 A19
82 A18
83 A17
84 A16
85 A15
86 A14
87 A13
88 A12
89 A11
90 A10
109 A9
110 A8
111 A7
112 A6
113 A5
114 A4
115 A3
116 A2
117 A1
118 A0
17 EDATA3
16 EDATA2
15 EDATA1
14 EDATA0
63 LA23
70 LA22
71 LA21
93 LA20
95 LA19
102 LA18
103 LA17
13 YIOW
12 YIOR
11 YMEMW
10 YMEMR
18 REFR
53 ADSTB
54 A20GT
123 HLDA
21 BHE
24 ADRO
52 MASTER
28 RESET
119 SO
120 S1
121 M/$\overline{IO}$
122 CPUCLK
44 TAP 1
26 TAP 2
ADDR19 59
ADDR18 61
ADDR17 62
ADDR16 64
ADDR15 65
ADDR14 66
ADDR13 68
ADDR12 69
ADDR11 72
ADDR10 73
ADDR 9 75
ADDR 8 94
ADDR 7 96
ADDR 6 97
ADDR 5 98
ADDR 4 100
ADDR 3 101
ADDR 2 104
ADDR 1 106
ADDR 0 105
RA9 41
RA8 39
RA7 38
RA6 37
RA5 36
RA4 35
RA3 34
RA2 33
RA1 32
RA0 31
RAS0 128
RAS1 129
RAS2 130
RAS3 132
CAS0L 125
CAS1L 126
CAS2L 2
CAS3L 3
CAS0H 4
CAS1H 5
CAS2H 6
CAS3H 131
CS8042 60
CS287 56
CSPTB 22
CSNMI 20
SELDATA 40
CSPROM 43
CS0 48
CS1 47
CS2 46
CS3 45
CSF 49
FRES 19
IORDY 127
DBLE 23
IOW 9
IOR 8
ONBD 57
LOMEG 25
RAS 58

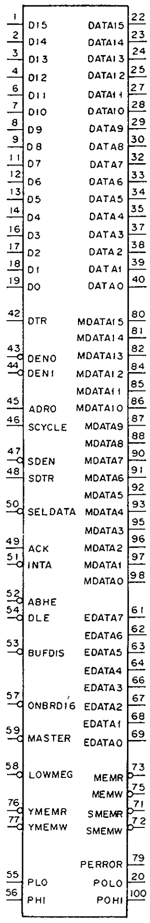
A0-23	;	CPU Address lines 0 to 23.
A20GT	;	Address 20 gate.
ADDR0-19	;	AT bus address lines 0 to 19.
ADR0	;	Low byte enable.
ADSTB	;	Address strobe from FE3001.
-BHE	;	Bus high enable.
-CASnL	;	Column address signal for D-RAM bank n (n=0 to 3), low byte.
-CASnH	;	Column address signal for D-RAM bank n (n=0 to 3), high byte.
CPUCLK	;	CPU clock.
-CS0,1	;	Programmable chip selects 0 and 1.
-CS2	;	Programmable chip select 2 or Real-time clock chip select.
-CS287	;	80287 Co-processor chip select.
-CS3	;	Programmable chip select 3 or Hard disk controller chip select.
-CS8042	;	8042 Keyboard controller chip select.
CSF	;	FDC chip select or Operation or Config. register select.
-CSNMI	;	NMI logic select.
-CSPROM	;	BIOS P-ROM select.
-CSPTB	;	Port B select.
-DBLE	;	Data bus latch enable.
EDATA0-7	;	Control register data bits 0 to 7.
-FRES	;	Fast reset to CPU.
HLDA	;	CPU hold acknowledge line.
-IOR	;	System I/O read command signal, drives expansion bus. An input in Master mode.
IORDY	;	Ready line, open drain. Directly connected to IOCHRDY bus line.
-IOW	;	System I/O write command signal, drives expansion bus. An input in Master mode.
LA17-23	;	AT bus large address lines 17 to 23.
-LOMEG	;	Lower 1M-byte enable.
-MASTER	;	Master on expansion bus has control of the bus.
M/-IO	;	CPU memory or I/O select (memory cycle = high, I/O cycle = low).
-ONBD	;	16 bits on board D-RAM memory or I/O device.
RA0-9	;	Memory address multiplexer output lines 0 to 9.
-RAS	;	To RAS delay line input.
-RASn	;	Raster address signal for D-RAM bank n (n=0 to 3).
-REFR	;	Memory refresh signal.
-RESET	;	Reset to the system.
-S0, -S1	;	CPU status lines 0 and 1.
-SELDATA	;	Direction of data transceiver data to EDATA bus.
-TAP1,2	;	First and Second tap outputs of RAS delay lines.
VDD1-6	;	+5V supply terminals.
VSS1-11	;	Ground terminals.
-YIOR	;	Ungated I/O read strobe from FE3001. An output in Master mode.
-YIOW	;	Ungated I/O write strobe from FE3001. An output in Master mode.
-YMEMR	;	Ungated system memory read command signal from FE3001.
-YMEMW	;	Ungated system memory write command signal from FE3001.

FE3031 (FARADAY ELECTRONICS)

C-MOS AT DATA BUFFER (PLCC PACKAGE)
- TOP VIEW -


13 D5
12 D6
11 D7
10 VDD (+5V)
9 D8
8 D9
7 D10
6 D11
5 Vss (GND)
4 D12
3 D13
2 D14
1 D15
100 POHI
99 VDD (+5V)
98 MDATA0
97 MDATA1
96 MDATA2
95 MDATA3
94 Vss (GND)
93 MDATA4
92 MDATA5
91 MDATA6
90 MDATA7
89 VDD (+5V)
14 D4
15 Vss (GND)
16 D3
17 D2
18 D1
19 D0
20 POLO
21 VDD (+5V)
22 DATA15
23 DATA14
24 DATA13
25 DATA12
26 Vss (GND)
27 DATA11
28 DATA10
29 DATA 9
30 DATA 8
31 VDD (+5V)
32 DATA 7
33 DATA 6
34 DATA 5
35 DATA 4
36 Vss (GND)
37 DATA 3
38 DATA 2
88 MDATA8
87 MDATA9
86 MDATA10
85 MDATA11
84 MDATA12
83 Vss (GND)
82 MDATA13
81 MDATA14
80 MDATA15
79 PERROR
78 VDD (+5V)
77 YMEMW
76 YMEMR
75 MEMW
74 Vss (GND)
73 MEMR
72 SMEMW
71 SMEMR
70 VDD (+5V)
69 EDATA0
68 EDATA1
67 EDATA2
66 EDATA3
65 Vss (GND)
64 EDATA4
39 DATA1
40 DATA0
41 VDD (+5V)
42 DTR
43 DEN0
44 DEN1
45 ADR0
46 SYSCLE
47 SDEN
48 SDTR
49 ACK
50 SELDATA
51 INTA
52 ABHE
53 BUFDIS
54 DLE
55 PLO
56 PHI
57 ONBRD16
58 LOWMEG
59 MASTER
60 Vss (GND)
61 EDATA7
62 EDATA6
63 EDATA5

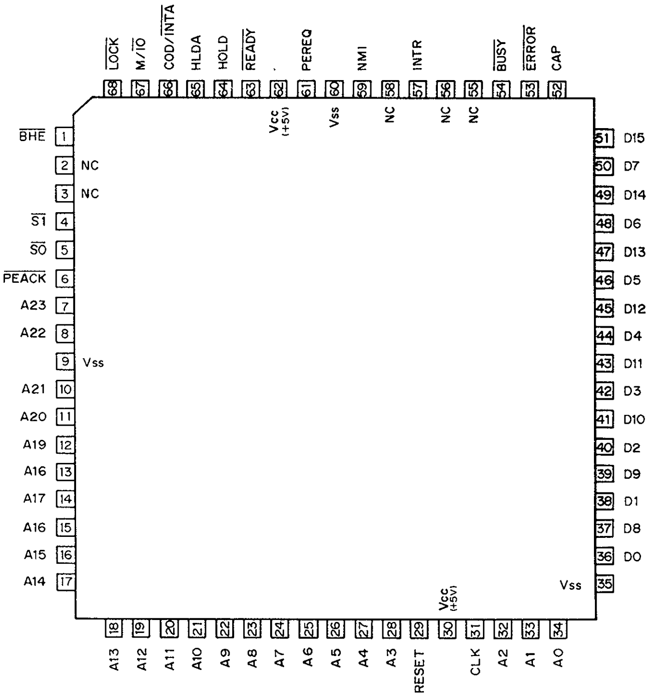
ABHE	I	High byte enable for MDATA bus.
ACK	I	DMA acknowledge signal to PC/AT bus.
ADR0	I	Address bit 0 for MDATA buffers and byte swap.
BUFDIS	I	Disable buffers when low.
D0-15	I/O	80286 local data bus.
DATA0-15	I/O	PC/AT data bus.
DEN0	I	Low byte data enable to DATA buffers.
DEN1	I	High byte data enable to DATA buffers.
DLE	I	Latch MDATA bus during a read.
DTR	I	Data direction for DATA buffers.
EDATA0-7	I/O	Peripheral data bus for FE3001, FE3010B, Real-time clock, and Keyboard controller.
INTA	I	Interrupt acknowledge.
LOWMEG	I	LOWMEG indicates access of lower 1M-byte of memory.
MASTER	I	Master on PC bus has control of bus.
MDATA0-15	I/O	Memory data bus.
MEMR	I/O	Memory read to/from AT bus.
MEMW	I/O	Memory write to/from AT bus.
ONBRD16	I	ONBRD indicates a local D-RAM operation.
PERROR	O	RAM parity error.
PHI	I	High byte parity bit from D-RAMs.
PLO	I	Low byte parity bit from D-RAMs.
POHI	O	High byte parity bit to D-RAMs.
POLO	O	Low byte parity bit to D-RAMs.
SCYCLE	I	Latch low byte during byte swap read.
SDEN	I	Byte swap data buffer enable.
SDTR	I	Byte swap data direction to swap buffer.
SELDATA	I	EDATA bus enable.
SMEMR	O	Low 1M bytes memory read to PC bus.
SMEMW	O	Low 1M bytes memory write to PC bus.
VDD	-	+5V.
VSS	-	Ground.
YMEMR	I/O	Memory read to/from FE3001.
YMEMW	I/O	Memory write to/from FE3001.

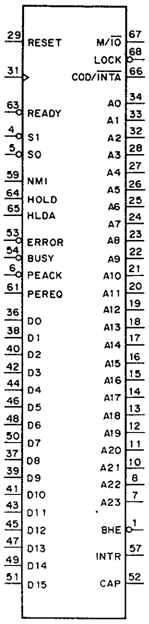

1 D15
2 D14
3 D13
4 D12
6 D11
7 D10
8 D9
9 D8
11 D7
12 D6
13 D5
14 D4
16 D3
17 D2
18 D1
19 D0
42 DTR
43 DEN0
44 DEN1
45 ADR0
46 SCYCLE
47 SDEN
48 SDTR
50 SELDATA
49 ACK
51 INTA
52 ABHE
54 DLE
53 BUFDIS
57 ONBRD16
59 MASTER
58 LOWMEG
76 YMEMR
77 YMEMW
55 PLO
56 PHI
DATA15 22
DATA14 23
DATA13 24
DATA12 25
DATA11 27
DATA10 28
DATA9 29
DATA8 30
DATA7 32
DATA6 33
DATA5 34
DATA4 35
DATA3 37
DATA2 38
DATA1 39
DATA0 40
MDATA15 80
MDATA14 81
MDATA13 82
MDATA12 84
MDATA11 85
MDATA10 86
MDATA9 87
MDATA8 88
MDATA7 90
MDATA6 91
MDATA5 92
MDATA4 93
MDATA3 95
MDATA2 96
MDATA1 97
MDATA0 98
EDATA7 61
EDATA6 62
EDATA5 63
EDATA4 64
EDATA3 66
EDATA2 67
EDATA1 68
EDATA0 69
MEMR 73
MEMW 75
SMEMR 71
SMEMW 72
PERROR 79
POLO 20
POHI 100

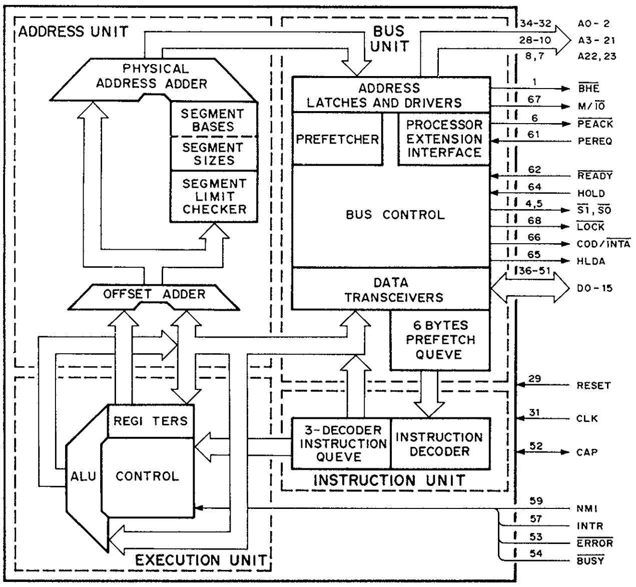
N80286-10 (INTEL) (CLOCK RATE = 10MHz)

16-BIT MICROPROCESSOR

– TOP VIEW –


LOCK 68
M/IO 67
COD/INTA 66
HLDA 65
HOLD 64
READY 63
62 Vcc (+5V)
PEREQ 61
60 Vss
NMI 59
58 NC
INTR 57
56 NC
55 NC
BUSY 54
ERROR 53
CAP 52
BHE 1
2 NC
3 NC
S1 4
S0 5
PEACK 6
A23 7
A22 8
9 Vss
A21 10
A20 11
A19 12
A16 13
A17 14
A16 15
A15 16
A14 17
51 D15
50 D7
49 D14
48 D6
47 D13
46 D5
45 D12
44 D4
43 D11
42 D3
41 D10
40 D2
39 D9
38 D1
37 D8
36 D0
Vss 35
18 A13
19 A12
20 A11
21 A10
22 A9
23 A8
24 A7
25 A6
26 A5
27 A4
28 A3
29 RESET
30 Vcc (+5V)
31 CLK
32 A2
33 A1
34 A0


29 RESET
31
63 READY
4 S1
5 S0
59 NMI
64 HOLD
65 HLDA
53 ERROR
54 BUSY
6 PEACK
61 PEREQ
36 D0
38 D1
40 D2
42 D3
44 D4
46 D5
48 D6
50 D7
37 D8
39 D9
41 D10
43 D11
45 D12
47 D13
49 D14
51 D15
M/IO 67
LOCK 68
COD/INTA 66
A0 34
A1 33
A2 32
A3 28
A4 27
A5 26
A6 25
A7 24
A8 23
A9 22
A10 21
A11 20
A12 19
A13 18
A14 17
A15 16
A16 15
A17 14
A18 13
A19 12
A20 11
A21 10
A22 8
A23 7
BHE 1
INTR 57
CAP 52


ADDRESS UNIT
BUS UNIT
PHYSICAL ADDRESS ADDER
SEGMENT BASES
SEGMENT SIZES
SEGMENT LIMIT CHECKER
OFFSET ADDER
ADDRESS LATCHES AND DRIVERS
PREFETCHER
PROCESSOR EXTENSION INTERFACE
BUS CONTROL
DATA TRANSCEIVERS
6 BYTES PREFETCH QUEVE
REGI TERS
ALU
CONTROL
3-DECODER INSTRUCTION QUEVE
INSTRUCTION DECODER
INSTRUCTION UNIT
EXECUTION UNIT
34-32 A0 - 2
28-10 A3 - 21
8,7 A22, 23
1 BHE
67 M/IO
6 PEACK
61 PEREQ
62 READY
64 HOLD
4,5 S1, S0
68 LOCK
66 COD/INTA
65 HLDA
36-51 D0 - 15
29 RESET
31 CLK
52 CAP
59 NMI
57 INTR
53 ERROR
54 BUSY

A0-A23	(O)	; ADDRESS LINES 0-23
$\overline{BHE}$	(O)	; BUS HIGH ENABLE
$\overline{BUSY}$	(I)	; PROCESSOR EXTENSION BUSY
CAP	(I)	; SUBSTRATE FILTER CAPACITOR
CLK	(I)	; SYSTEM CLOCK
COD/$\overline{INTA}$	(O)	; CODE/INTERRUPT ACKNOWLEDGE
D0-D15	(I/O)	; DATA LINES 0-15
$\overline{ERROR}$	(I)	; PROCESSOR EXTENSION ERROR
HLDA	(O)	; BUS HOLD ACKNOWLEDGE
HOLD	(I)	; BUS HOLD REQUEST
INTR	(I)	; INTERRUPT REQUEST
$\overline{LOCK}$	(O)	; BUS LOCK
M/$\overline{IO}$	(O)	; MEMORY or I/O SELECT
NMI	(I)	; NON-MASKABLE INTERRUPT REQUEST
$\overline{PEACK}$	(O)	; PROCESSOR EXTENSION OPERAND ACKNOWLEDGE
PEREQ	(I)	; PROCESSOR EXTENSION OPERAND REQUEST
$\overline{READY}$	(I)	; BUS READY
RESET	(I)	; SYSTEM RESET
$\overline{S0}$,$\overline{S1}$	(O)	; BUS CYCLE STATUS

BHE and A0 ENCODINGS

BHE VALUE	A0 VALUE	FUNCTION
0	0	WORD TRANSFER
0	1	BYTE TRANSFER ON UPPER HALF OF DATA BUS(D8-D15)
1	0	BYTE TRANSFER ON UPPER HALF OF DATA BUS(D0-D7)
1	1	WILL NEVER OCCUR

80286 BUS CYCLE STATUS DEFINITION

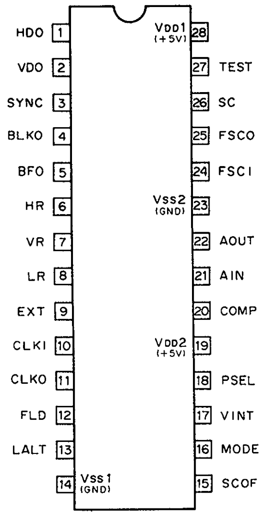
COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	BUS CYCLE INITISTED
0	0	0	0	INTERRUPT ACKNOWLEDGE
0	0	0	1	WILL NOT OCCUR
0	0	1	0	WILL NOT OCCUR
0	0	1	1	NONE ; NOT A STATUS CYCLE
0	1	0	0	IF A1="1" THEN HALF ; ELSE SHUTDOWN
0	1	0	1	MEMORY DATA READ
0	1	1	0	MEMORY DATA WRITE
0	1	1	1	NONE ; NOT A STATUS CYCLE
1	0	0	0	WILL NOT OCCUR
1	0	0	1	I/O READ
1	0	1	0	I/O WRITE
1	0	1	1	NONE ; NOT A STATUS CYCLE
1	1	0	0	WILL NOT OCCUR
1	1	0	1	MEMORY INSTRUCTION READ
1	1	1	0	WILL NOT OCCUR
1	1	1	1	NONE ; NOT A STATUS CYCLE

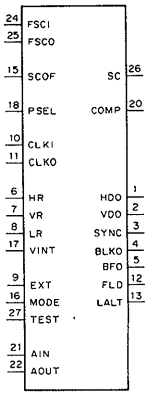
0 ; LOW LEVEL
1 ; HIGH LEVEL

CXD1030M (SONY) FLAT PACKAGE

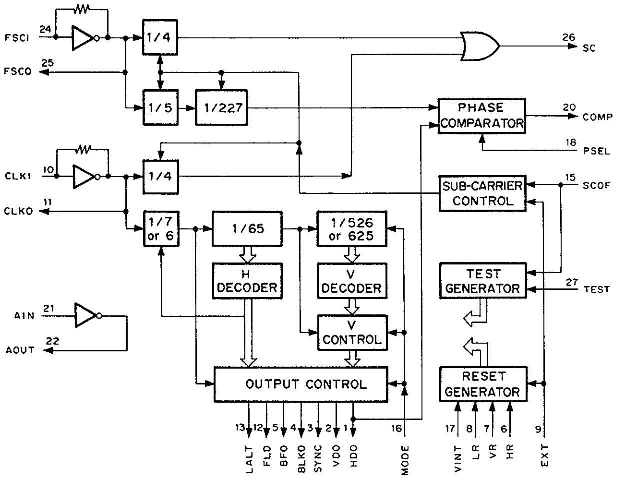
C-MOS SYNCHRONOUS SIGNAL GENERATOR

– TOP VIEW –


HDO 1
VDO 2
SYNC 3
BLKO 4
BFO 5
HR 6
VR 7
LR 8
EXT 9
CLKI 10
CLKO 11
FLD 12
LALT 13
14 Vss1 (GND)
28 Vdd1 (+5V)
27 TEST
26 SC
25 FSCO
24 FSCI
23 Vss2 (GND)
22 AOUT
21 AIN
20 COMP
19 Vdd2 (+5V)
18 PSEL
17 VINT
16 MODE
15 SCOF


24 FSCI
25 FSCO
15 SCOF
18 PSEL
10 CLKI
11 CLKO
6 HR
7 VR
8 LR
17 VINT
9 EXT
16 MODE
27 TEST
21 AIN
22 AOUT
SC 26
COMP 20
HDO 1
VDO 2
SYNC 3
BLKO 4
BFO 5
FLD 12
LALT 13

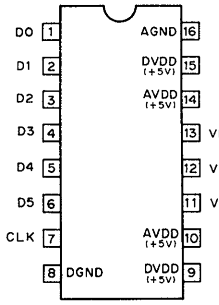
PIN No.	SYMBOL NAME	ABBREVATION
1	HDO	HORIZONTAL DRIVE PULSE OUTPUT
2	VDO	VARTICAL DRIVE PULSE OUTPUT
3	SYNC	COMPOSITE SYNCHRONOUS PULSE OUTPUT
4	BLKO	COMPOSITE BLANKING PULSE OUTPUT
5	BFO	BURST FLAG PULSE OUTPUT
6	HR	H RESET INPUT
7	VR	V RESET INPUT
8	LR	LINE ALTERNATE RESET INPUT
9	EXT	INTERNAL/EXTERNAL MODE SELECT
10	CLKI	CLOCK INPUT (NTSC:14.31818MHz, PAL:14.1875MHz)
11	CLKO	CLOCK OUTPUT
12	FLD	FIELD PULSE OUTPUT
13	VSS1	GND
14	LALT	LINE ALTERNATE PULSE OUTPUT
15	SCOF	SUB-CARRIER OFF INPUT (ON/OFF)
16	MODE	NTSC/PAL MODE SELECT
17	VINT	INITIALRISE INPUT
18	PSEL	PHASE COMPARATE POLARITY SELECT
19	VDD2	+5V of INVERTER for FILTER
20	COMP	OUTPUT of PHASE COMPARATOR
21	AIN	INPUT of INVERTER for FILTER
22	AOUT	OUTPUT of INVERTER for FILTER
23	VSS2	GND of INVERTER for FILTER
24	FSCI	4fsc CLOCK INPUT
25	FSCO	4fsc CLOCK OUTPUT
26	SC	SUB-CRRIER OUTPUT
27	TEST	TEST INPUT (NORMALLY LOW LEVEL)
28	VDD1	+5V

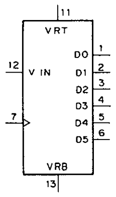

FSCI 24
FSCO 25
1/4
1/5
1/227
26 SC
PHASE COMPARATOR
20 COMP
18 PSEL
CLKI 10
CLKO 11
1/4
SUB-CARRIER CONTROL
15 SCOF
1/7 or 6
1/65
1/526 or 625
H DECODER
V DECODER
V CONTROL
TEST GENERATOR
27 TEST
AIN 21
AOUT 22
OUTPUT CONTROL
RESET GENERATOR
13 12 5 4 3 2 1
LALT FLD BFO BLKO SYNC VDO HDO
16 MODE
17 8 7 6
VINT LR VR HR
9 EXT

CXD1172M (SONY) FLAT PACKAGE

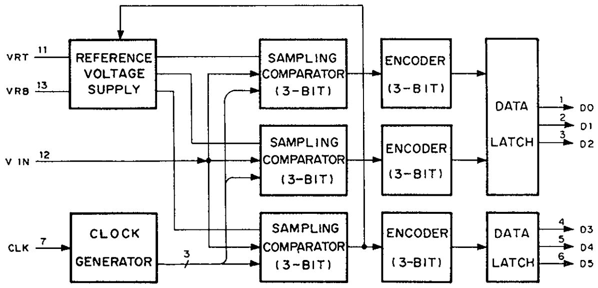
6 BITS 20 MSPS VIDEO A/D CONVERTER

– TOP VIEW –


D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
CLK 7
8 DGND
AGND 16
DVDD (+5V) 15
AVDD (+5V) 14
13 VRB
12 V IN
11 VRT
AVDD (+5V) 10
DVDD (+5V) 9


11 VRT
12 V IN
7
D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
VRB 13

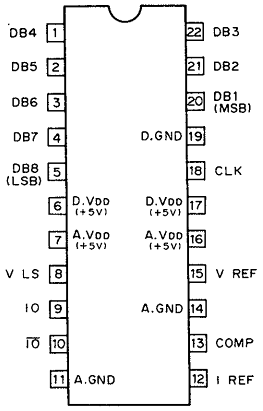
AGND; ANALOG GROUND
AVDD; ANALOG POWER SUPPLY
CLK; CLOCK INPUT
D0-5; DIGITAL DATA OUTPUTS (LSB to MSB)
DGND; DIGITAL GROUND
DVDD; DIGITAL POWER SUPPLY
V IN; ANALOG VOLTAGE INPUT
VRB; BOTTOM REFERENCE VOLTAGE INPUT
VRT; TOP REFERENCE VOLTAGE INPUT

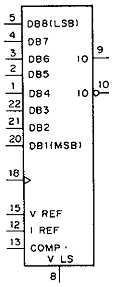

VRT 11
VRB 13
REFERENCE VOLTAGE SUPPLY
SAMPLING COMPARATOR (3-BIT)
ENCODER (3-BIT)
DATA LATCH
V IN 12
CLK 7
CLOCK GENERATOR
3
1 D0
2 D1
3 D2
4 D3
5 D4
6 D5

uPD6902C (NEC)

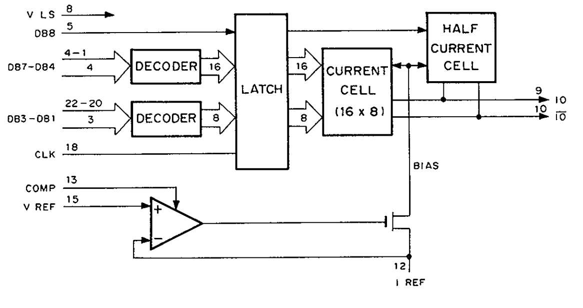
C-MOS 8-BIT D/A CONVERTER

– TOP VIEW –


DB4 1
DB5 2
DB6 3
DB7 4
DB8 (LSB) 5
6 D.Vdd (+5V)
7 A.Vdd (+5V)
V LS 8
IO 9
IO̅ 10
11 A.GND
22 DB3
21 DB2
20 DB1 (MSB)
D.GND 19
18 CLK
D.Vdd (+5V) 17
A.Vdd (+5V) 16
15 V REF
A.GND 14
13 COMP
12 I REF


5 DB8(LSB)
4 DB7
3 DB6
2 DB5
1 DB4
22 DB3
21 DB2
20 DB1(MSB)
18
15 V REF
12 I REF
13 COMP
V LS 8
IO 9
IO 10

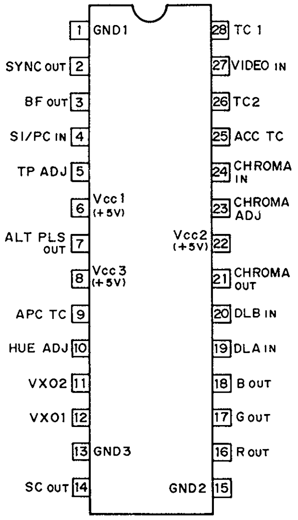
A.GND; ANALOG GROUND
A.VDD; ANALOG POWER SUPPLY
COMP; PHASE COMPENSATION
CLK; CLOCK INPUT
DB1-8; DIGITAL DATA INPUTS (MSB to LSB)
D.GND; DIGITAL GROUND
D.VDD; DIGITAL POWER SUPPLY
IO; ANALOG CURRENT OUTPUT
I REF; FULL SCALE CURRENT
V LS; VOLTAGE LEVEL SELECT (C̅-̅M̅O̅S̅/TTL)
V REF; REFERENCE VOLTAGE

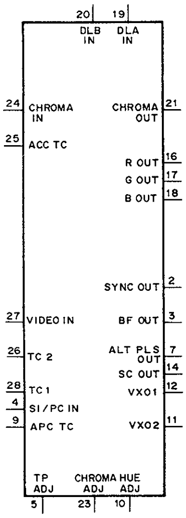

V LS 8
DB8 5
DB7-DB4 4-1
4
DECODER
16
DB3-DB1 22-20
3
DECODER
8
CLK 18
LATCH
16
8
CURRENT CELL (16 x 8)
HALF CURRENT CELL
9 IO
10 IO̅
BIAS
COMP 13
V REF 15
12 I REF

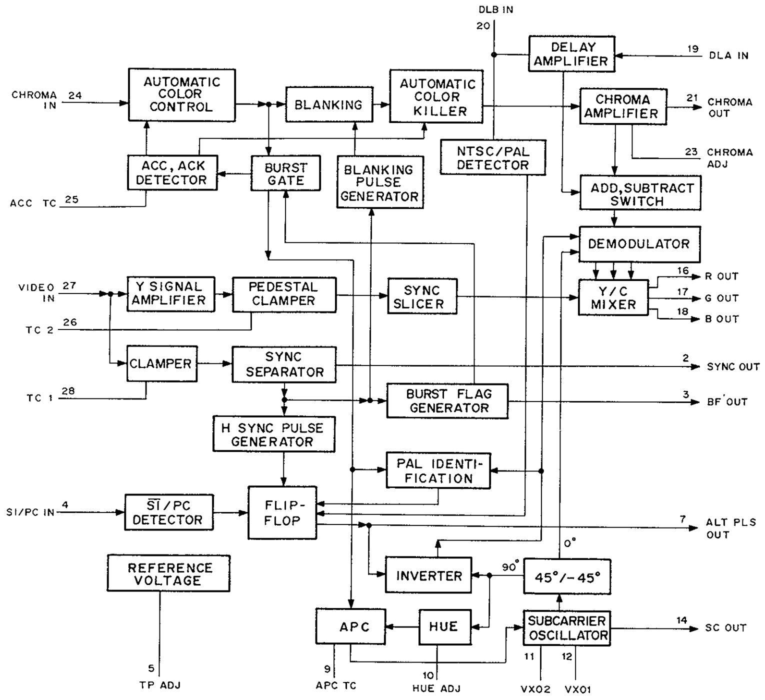
V7020 (SONY)

NTSC/PAL DECODER

– TOP VIEW –


1 GND1
SYNC OUT 2
BF OUT 3
SI/PC IN 4
TP ADJ 5
6 Vcc1 (+5V)
ALT PLS OUT 7
8 Vcc3 (+5V)
APC TC 9
HUE ADJ 10
VXO2 11
VXO1 12
13 GND3
SC OUT 14
28 TC 1
27 VIDEO IN
26 TC2
25 ACC TC
24 CHROMA IN
23 CHROMA ADJ
Vcc2 (+5V) 22
21 CHROMA OUT
20 DLB IN
19 DLA IN
18 B OUT
17 G OUT
16 R OUT
GND2 15


20 DLB IN
19 DLA IN
24 CHROMA IN
25 ACC TC
CHROMA OUT 21
R OUT 16
G OUT 17
B OUT 18
SYNC OUT 2
27 VIDEO IN
BF OUT 3
26 TC 2
ALT PLS OUT 7
SC OUT 14
28 TC1
VXO1 12
4 SI/PC IN
9 APC TC
VXO2 11
TP ADJ 5
CHROMA ADJ 23
HUE ADJ 10

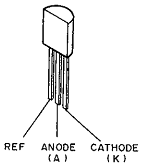

DLB IN 20
DELAY AMPLIFIER
19 DLA IN
CHROMA IN 24
AUTOMATIC COLOR CONTROL
BLANKING
AUTOMATIC COLOR KILLER
CHROMA AMPLIFIER
21 CHROMA OUT
23 CHROMA ADJ
ACC, ACK DETECTOR
BURST GATE
BLANKING PULSE GENERATOR
NTSC/PAL DETECTOR
ADD, SUBTRACT SWITCH
ACC TC 25
DEMODULATOR
VIDEO IN 27
Y SIGNAL AMPLIFIER
PEDESTAL CLAMPER
SYNC SLICER
Y/C MIXER
16 R OUT
17 G OUT
18 B OUT
TC 2 26
CLAMPER
SYNC SEPARATOR
2 SYNC OUT
TC 1 28
BURST FLAG GENERATOR
3 BF OUT
H SYNC PULSE GENERATOR
PAL IDENTI-FICATION
SI/PC IN 4
S̄Ī/PC DETECTOR
FLIP-FLOP
7 ALT PLS OUT
0°
REFERENCE VOLTAGE
INVERTER
90°
45°/-45°
APC
HUE
SUBCARRIER OSCILLATOR
14 SC OUT
5 TP ADJ
9 APC TC
10 HUE ADJ
11 VXO2
12 VXO1

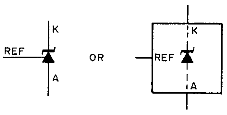
FUNCTION TABLE

PIN No.	SYMBOLIC NAME	DESCRIPTION
1	GND1	GROUND FOR Y SIGNAL AMPLIFIER AND SYNCHRONIZING SIGNAL SEPARATOR
2	SYNC OUT	SYNCHRONIZING SIGNAL OUTPUT (TTL LEVEL)
3	BF OUT	BURST FLAG OUTPUT (TTL LEVEL)
4	SI/PC IN	SUPERIMPOSE OR PERSONAL COMPUTER SELECTION SIGNAL INPUT SI MODE:LOW, PC MODE:HIGH
5	TP ADJ	BURST FLAG POSITION ADJUSTMENT
6	Vcc1	Vcc FOR Y SIGNAL AMPLIFIER AND SYNCHRONIZING SIGNAL SEPARATOR
7	ALT PLS OUT	LINE ALTERNATION PULSE OUTPUT NTSC MODE:LOW PAL MODE:LINE ALTERNATION PULSE
8	Vcc3	Vcc FOR APC, HUE, AND VXO STAGES
9	APC TC	AUTOMATIC PHASE CONTROL TIME CONSTANT
10	HUE ADJ	HUE ADJUSTMENT
11	VXO2	CRYSTAL OSCILLATOR
12	VXO1	
13	GND3	GROUND FOR APC, HUE, AND VXO STAGES
14	SC OUT	SUBCARRIER SIGNAL OUTPUT
15	GND2	GROUND FOR DEMODULATOR AND Y/C MIXER
16	R OUT	RED SIGNAL OUTPUT
17	G OUT	GREEN SIGNAL OUTPUT
18	B OUT	BLUE SIGNAL OUTPUT
19	DLA IN	DELAY AMPLIFIER INPUT
20	DLB IN	MODE SELECTION AND DELAY AMPLIFIER GAIN BIAS NTSC MODE: $V20 \leq 0.8V$ PAL MODE: $2.0V \leq V20 \leq 2.8V$ V20 IS THE VOLTAGE MUST BE APPLIED
21	CHROMA OUT	CHROMA SIGNAL OUTPUT
22	Vcc2	Vcc FOR DEMODULATOR AND Y/C MIXER
23	CHROMA ADJ	MODE SELECTION AND CHROMA AMPLIFIER GAIN ADJUSTMENT BLACK/WHITE MODE: $V23 \leq 0.8V$ COLOR MODE: $2.0V \leq V23 \leq 3.0V$ V23 IS THE VOLTAGE MUST BE APPLIED
24	CHROMA IN	CHROMA SIGNAL INPUT
25	ACC TC	AUTOMATIC COLOR CONTROL TIME CONSTANT
26	TC2	TIME CONSTANT FOR PEDESTAL CLAMPER
27	VIDEO IN	VIDEO SIGNAL INPUT
28	TC1	TIME CONSTANT FOR SYNCHRONIZING SIGNAL SEPARATOR

AN1431T (MATSUSHITA)

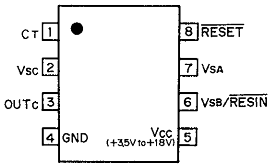
ADJUSTABLE PRECISION SHUNT REGULATOR

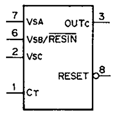

REF
ANODE (A)
CATHODE (K)

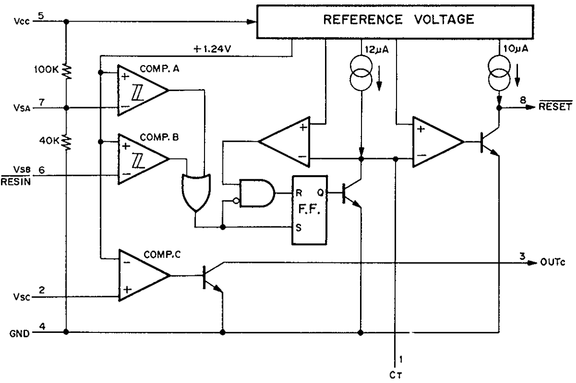

K
REF
A
OR
K
REF
A

MB3771DIP (FUJITSU)

2-WAY SUPPLY VOLTAGE SUPERVISOR
– TOP VIEW –

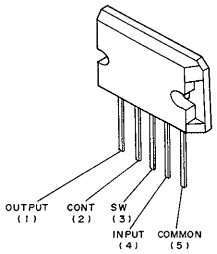

CT 1
Vsc 2
OUTc 3
4 GND
8 RESET
7 VSA
6 VSB/RESIN
Vcc (+3.5V to +18V) 5


7 VSA
6 VSB/RESIN
2 Vsc
1 CT
OUTc 3
RESET 8

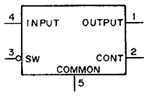

Vcc 5
REFERENCE VOLTAGE
+1.24V
100K
COMP. A
VSA 7
40K
COMP. B
VSB 6 /RESIN
12μA
10μA
8 RESET
R Q
F.F.
S
COMP. C
3 OUTc
Vsc 2
GND 4
1 CT

STR9012 (SANKEN)

POSITIVE VOLTAGE REGULATOR (4A)
– OBLIQUE VIEW –


OUTPUT (1)
CONT (2)
SW (3)
INPUT (4)
COMMON (5)

OUTPUT VOLTAGE	??
5 V	05
12V	12


4 INPUT
OUTPUT 1
3 SW
CONT 2
COMMON
5

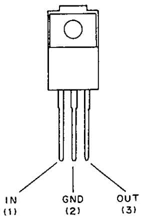
CONT ; OUTPUT CONTROL
SW ; OUTPUT SWITCHING

SW	OUTPUT
0	ON
1	OFF

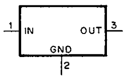
0 ; MAX 0.6V
1 ; MIN 2V

M5F7805 (MITSUBISHI)

POSITIVE VOLTAGE REGULATOR (1A)
– PRINTED SIDE VIEW –

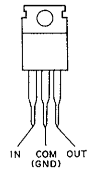

IN (1)
GND (2)
OUT (3)

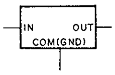
+5V	M5F7805
+6V	M5F7806
+7V	M5F7807
+8V	M5F7808
+9V	M5F7809
+10V	M5F7810
+12V	M5F7812
+15V	M5F7815
+18V	M5F7818
+20V	M5F7820
+24V	M5F7824


1 IN
OUT 3
GND
2

NJM7805A (JRC)

POSITIVE VOLTAGE REGULATOR (1A)
– SIDE VIEW –


IN
COM (GND)
OUT

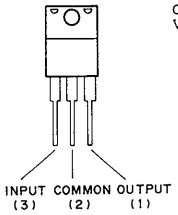

IN
OUT
COM(GND)

OUTPUT VOLTAGE	AN78??	FS78??	HA178??P	L78??	NJM78??B	NJM78??A/K
+5V	AN7805	FS7805	HA17805P	L7805	--------	NJM7805A/K
+6V	AN7806	------	HA17806P	-----	--------	NJM7806A/K
+7V	AN7807	------	HA17807P	L7807	--------	----------
+8V	AN7808	------	HA17808P	-----	--------	NJM7808A/K
+8.5V	------	------	--------	-----	--------	----------
+9V	AN7809	------	--------	-----	--------	NJM7809A/K
+10V	AN7810	------	--------	-----	--------	----------
+12V	AN7812	FS7812	HA17812P	-----	NJM7812B	NJM7812A/K
+15V	AN7815	FS7815	HA17815P	-----	--------	NJM7815A/K
+18V	AN7818	------	HA17818P	-----	--------	NJM7818A/K
+20V	AN7820	------	--------	-----	--------	NJM7820A/K
+24V	AN7824	FS7824	HA17824P	-----	--------	NJM7824A/K

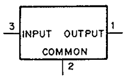
OUTPUT VOLTAGE	uA78??UC	uPC143??H	uPC78??H	TA78???P/AP
+5V	uA7805UC	uPC14305H	uPC7805H	TA78005P/AP
+6V	uA7806UC	---------	--------	TA78006P/AP
+7V	--------	---------	--------	---------
+8V	uA7808UC	uPC14308H	uPC7808H	TA78008P/AP
+8.5V	uA7885UC	---------	--------	---------
+9V	--------	---------	--------	TA78009P/AP
+10V	--------	---------	--------	TA78010P/AP
+12V	uA7812UC	uPC14312H	uPC7812H	TA78012P/AP
+15V	uA7815UC	uPC14315H	uPC7815H	TA78015P/AP
+18V	uA7818UC	uPC14318H	uPC7818H	TA78018P/AP
+20V	--------	---------	--------	TA78020P/AP
+24V	uA7824UC	uPC14324H	uPC7824H	TA78024P/AP

RC7805FA (RAYTHEON)

POSITIVE VOLTAGE REGULATOR
– FRONT VIEW –

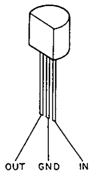

INPUT (3)
COMMON (2)
OUTPUT (1)

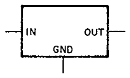
OUTPUT VOLTAGE	NJM78M??FA	NJM78??FA	RC78M??FA	RC78??FA
+5V	NJM78M05FA	NJM7805FA	RC78M05FA	RC7805FA
+6V	NJM78M06FA	NJM7806FA	RC78M06FA	RC7806FA
+8V	NJM78M08FA	NJM7808FA	---------	RC7808FA
+9V	NJM78M09FA	NJM7809FA	RC78M09FA	RC7809FA
+12V	NJM78M12FA	NJM7812FA	RC78M12FA	RC7812FA
+15V	NJM78M15FA	NJM7815FA	RC78M15FA	RC7815FA
+18V	NJM78M18FA	NJM7818FA	---------	RC7818FA
+20V	NJM78M20FA	NJM7820FA	---------	RC7820FA
+24V	NJM78M24FA	NJM7824FA	---------	RC7824FA


3 INPUT
OUTPUT 1
COMMON
2

NJM78L05A (JRC)
NJM78L09A (JRC)
RC78L05A (RAYTHEON)
RC78L09A (RAYTHEON)

POSITIVE VOLTAGE REGULATOR (100mA)

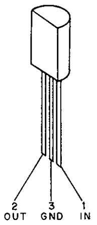


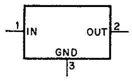


OUTPUT VOLTAGE	NJM78L??A	RC78L??A	uA78L??ACL	uA78L??AWV	uPC78L??J	AN78L??
+2.6V	NJM78L02A	RC78L02A	uA78L02ACL	uA78L26AWV	---------	-------
+4V	---------	--------	----------	----------	---------	AN78L04
+5V	NJM78L05A	RC78L05A	uA78L05ACL	uA78L05AWV	uPC78L05J	AN78L05
+6V	NJM78L06A	RC78L06A	----------	----------	---------	AN78L06
+6.2V	---------	--------	uA78L06ACL	uA78L62AWV	---------	-------
+7V	---------	--------	----------	----------	---------	AN78L07
+8V	NJM78L08A	RC78L08A	uA78L08ACL	----------	uPC78L08J	AN78L08
+8.2V	---------	--------	----------	uA78L82AWV	---------	-------
+9V	NJM78L09A	RC78L09A	uA78L09ACL	uA78L09AWV	---------	AN78L09
+10V	---------	--------	uA78L10ACL	----------	uPC78L10J	AN78L10
+12V	NJM78L12A	RC78L12A	uA78L12ACL	uA78L12AWV	uPC78L12J	AN78L12
+15V	NJM78L15A	RC78L15A	uA78L15ACL	uA78L15AWV	uPC78L15J	AN78L15
+18V	NJM78L18A	RC78L18A	----------	uA78L18AWV	---------	AN78L18
+20V	NJM78L20A	RC78L20A	----------	----------	---------	AN78L20
+24V	NJM78L24A	RC78L24A	----------	uA78L24AWV	---------	AN78L24

TA78L009AP (TOSHIBA)

POSITIVE VOLTAGE REGULATOR (150mA)



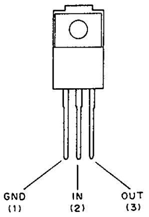


OUTPUT VOLTAGE	???
+5V	005
+6V	006
+7V	007
+7.5V	075
+8V	008
+9V	009
+10V	010
+12V	012
+13.2V	132
+15V	015
+18V	018
+20V	020
+24V	024

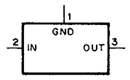
M5F79M05 (MITSUBISHI)
M5F79M12 (MITSUBISHI)

NEGATIVE VOLTAGE REGULATOR (500mA)

– PRINTED SIDE VIEW –



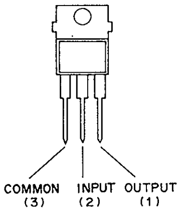
– 5V	M5F79M05
– 6V	M5F79M06
– 7V	M5F79M07
– 8V	M5F79M08
– 9V	M5F79M09
– 10V	M5F79M10
– 12V	M5F79M12
– 15V	M5F79M15
– 18V	M5F79M18
– 20V	M5F79M20
– 24V	M5F79M24



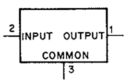
NJM79M12A (JRC)

NEGATIVE VOLTAGE REGULATOR (500mA)

– FRONT VIEW –



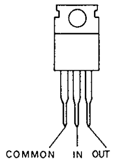
–5V	NJM79M05A
–6V	NJM79M06A
–8V	NJM79M08A
–9V	NJM79M09A
–12V	NJM79M12A
–15V	NJM79M15A
–18V	NJM79M18A
–24V	NJM79M24A



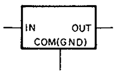
uPC79M05H (NEC)
uPC79M12H (NEC)

NEGATIVE VOLTAGE REGULATOR (0.5A)

– SIDE VIEW –

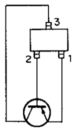


OUTPUT VOLTAGE	uA79M??AUC	FS79??M	AN79M??	uPC79M??H
-5V	uA79M05AUC	FS7905M	AN79M05	uPC79M05H
-6V	uA79M06AUC	-------	AN79M06	---------
-7V	----------	-------	AN79M07	---------
-8V	uA79M08AUC	-------	AN79M08	uPC79M08H
-9V	----------	-------	AN79M09	---------
-10V	----------	-------	AN79M10	---------
-12V	uA79M12AUC	FS7912M	AN79M12	uPC79M12H
-15V	uA79M15AUC	FS7915M	AN79M15	uPC79M15H
-18V	----------	-------	AN79M18	uPC79M18H
-20V	uA79M20AUC	-------	AN79M20	---------
-24V	uA79M24AUC	FS7924M	AN79M24	uPC79M24H



< 2SA >

TOP VIEW (SCALE 4/1)



2SA1162
2SA812

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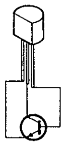
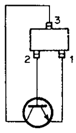


2SC458C

TOP VIEW (SCALE 4/1)



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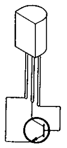

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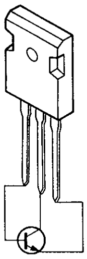
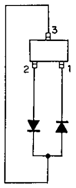


2SC4237

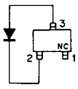
< OTHER >

TOP VIEW (SCALE 4/1)



1SS123
1SS226

TOP VIEW (SCALE 4/1)



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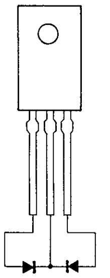

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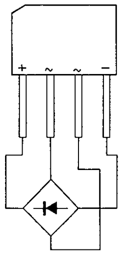

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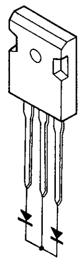

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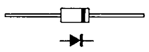

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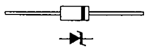
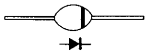
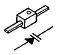
1SS120
1SS135E
1SS168
D1NL20
ERC38- ? ?



HZ ? ?A ?
HZ ? ?B ?
HZ ? ?C ?
RD ? ?ESB ?



DFG1A8
V19 ?



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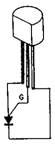
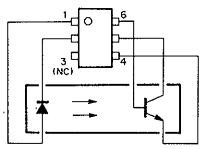


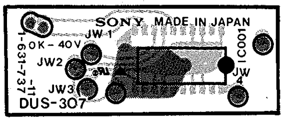
N13T1

TOP VIEW (SCALE 2/1)



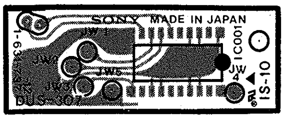
PC111S

5-2. DUS-307 BOARD


SONY MADE IN JAPAN
JW1
OK-40V
JW2
JW3
DUS-307
1-631-737-11
IC001
JW4

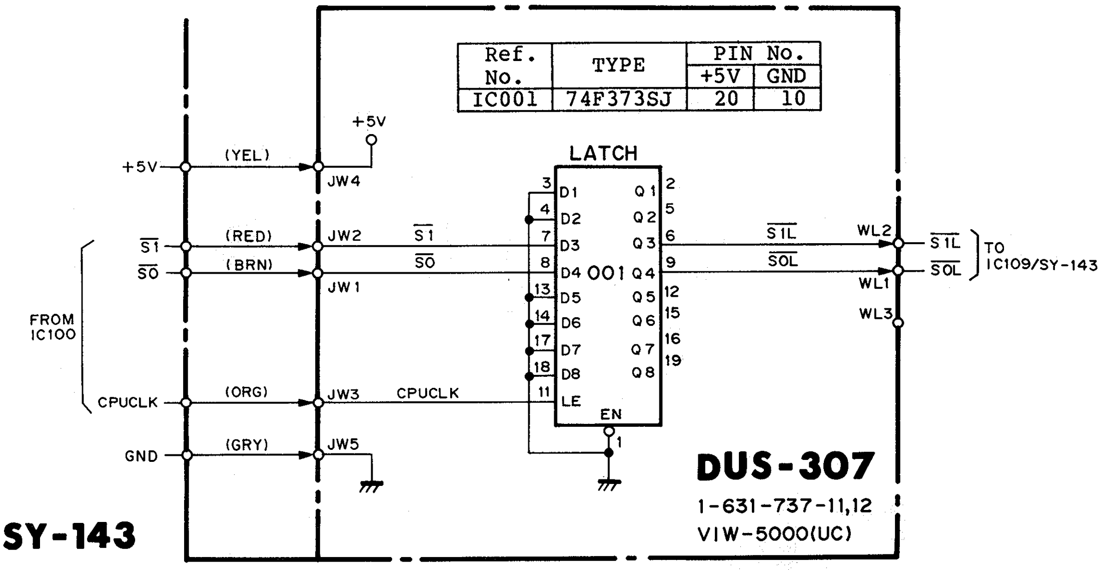
DUS-307 – COMPONENT SIDE –

1-631-737-11
VIW-5000(UC)


SONY MADE IN JAPAN
JW1
JW2
JW3
JW5
DUS-307
IC001
JW4
IS-10

DUS-307 – COMPONENT SIDE –

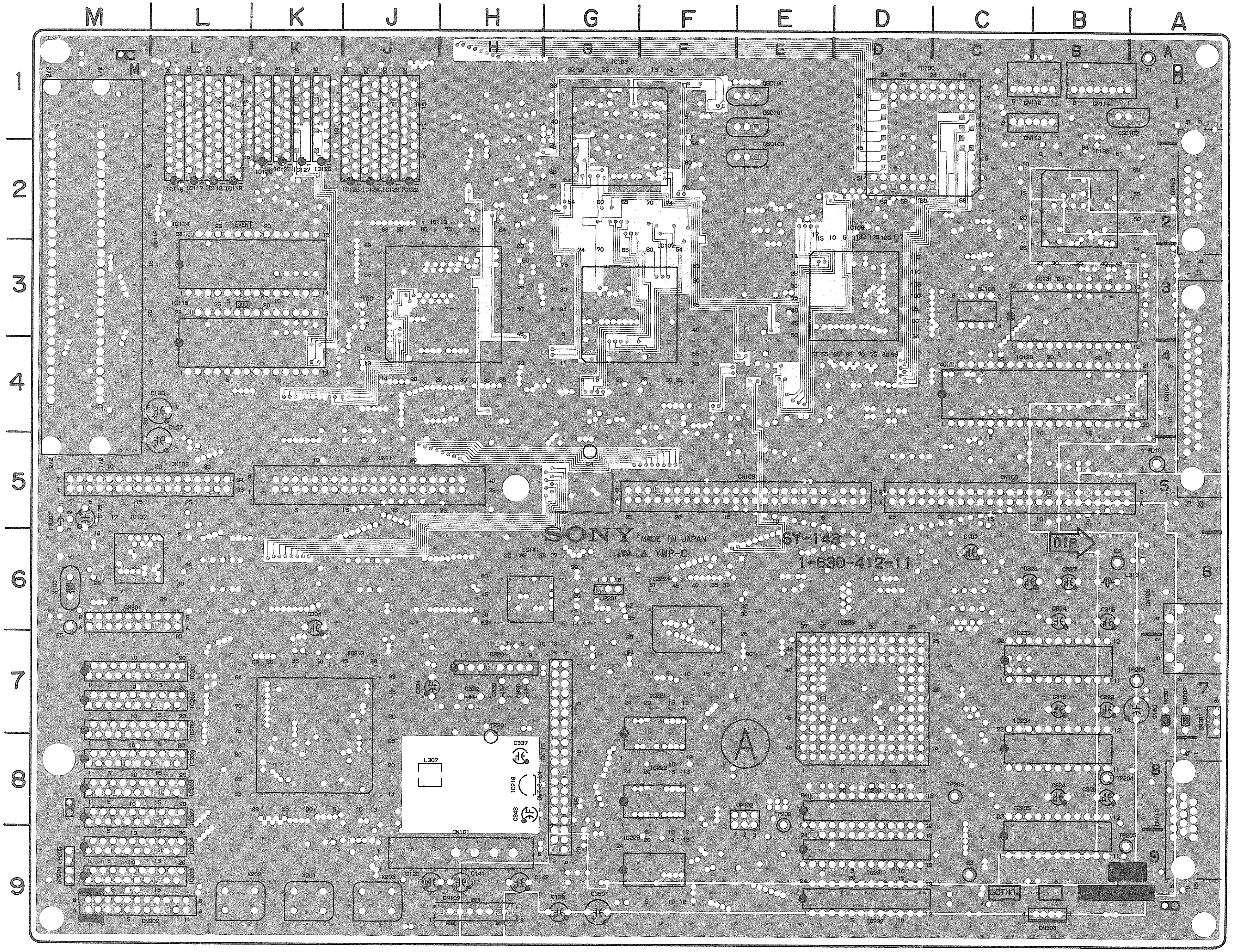
1-631-737-12
VIW-5000(UC)



Ref. No.	TYPE	PIN No.	
		+5V	GND
IC001	74F373SJ	20	10

+5V
(YEL)
JW4
+5V
S1
(RED)
JW2
S1
SO
(BRN)
JW1
SO
FROM IC100
CPUCLK
(ORG)
JW3
CPUCLK
GND
(GRY)
JW5
LATCH
D1
D2
D3
D4
D5
D6
D7
D8
LE
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
EN
001
3
4
7
8
13
14
17
18
11
2
5
6
9
12
15
16
19
1
S1L
SOL
WL2
WL1
WL3
S1L
SOL
TO IC109/SY-143
SY-143
DUS-307
1-631-737-11,12
VIW-5000(UC)

5-3. SY-143 BOARD


M
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K
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D
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1
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3
4
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8
9
SONY
MADE IN JAPAN
YWP-C
SY-143
1-630-412-11
DIP
LOTNO.
CN103
CN111
CN109
CN108
CN104
CN105
CN106
CN110
CN112
CN113
CN114
CN116
CN101
CN102
CN115
CN301
CN302
CN303
IC100
IC102
IC103
IC109
IC113
IC114
IC115
IC116
IC117
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IC123
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IC203
IC204
IC205
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IC207
IC208
IC213
IC218
IC220
IC221
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IC223
IC224
IC228
IC230
IC231
IC232
IC233
IC234
IC235
OSC100
OSC101
OSC102
OSC103
DL100
L307
L313
X100
X201
X202
X203
JP201
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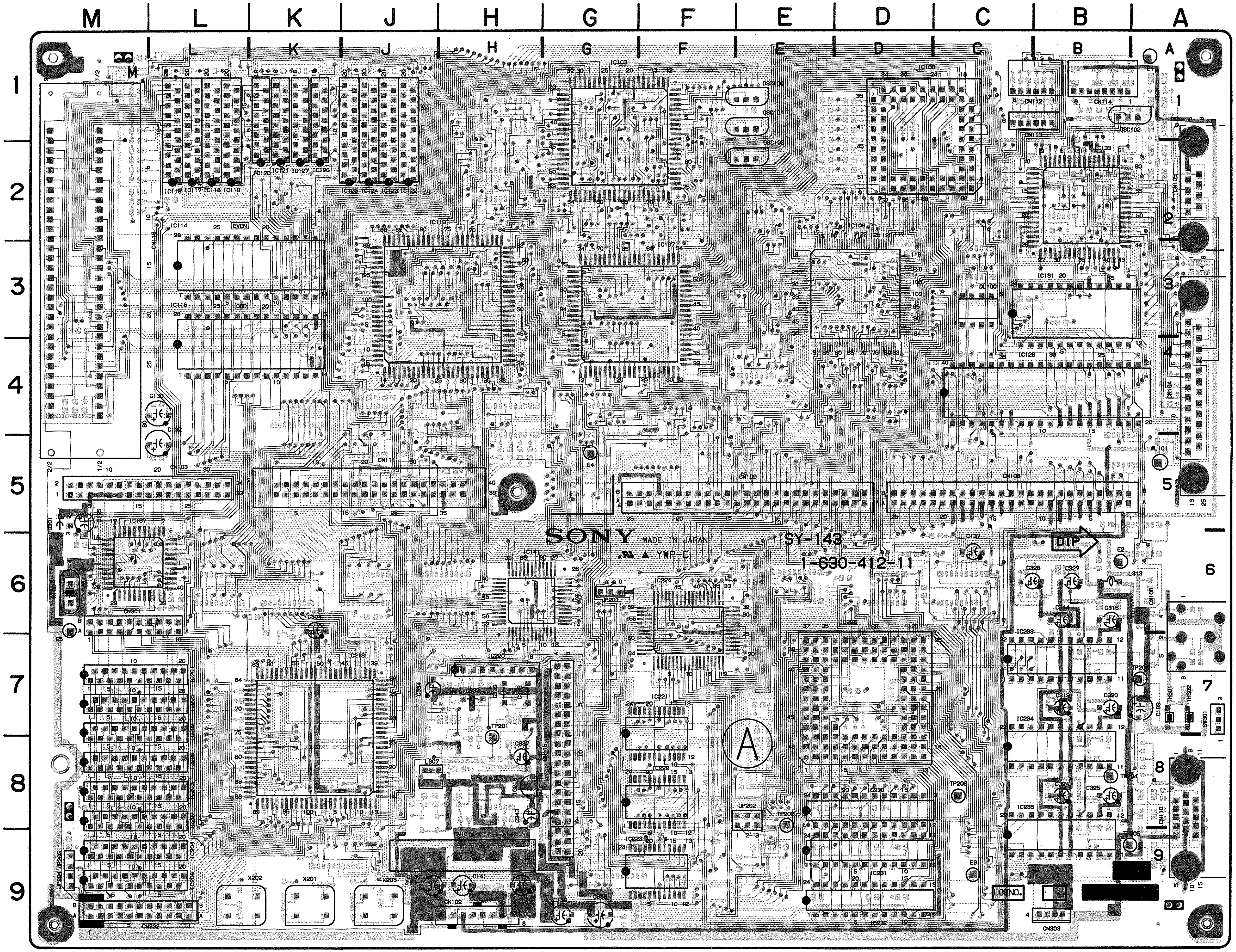
JP204
JP205
TP201
TP202
TP203
TP204
TP205
TP206
SW301
TH301
TH302
E1
E2
E3
E4
E5
WL101
FB301

SY-143 – COMPONENT SIDE –

1-630-412-11
VIW-5000(UC)


M
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8
9
SONY MADE IN JAPAN
YWP-C
SY-143
1-630-412-11
DIP
CN101
CN102
CN103
CN104
CN105
CN106
CN108
CN109
CN110
CN111
CN112
CN113
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CN116
CN301
CN302
CN303
IC100
IC103
IC107
IC109
IC113
IC114
IC115
IC128
IC131
IC133
IC137
IC141
IC213
IC220
IC221
IC222
IC223
IC224
IC225
IC230
IC231
IC232
IC233
IC234
IC235
OSC100
OSC101
OSC102
OSC103
X100
X201
X202
X203
EVEN
ODD
LOT NO.
A

SY-143 – COMPONENT SIDE –

1-630-412-11
VIW-5000(UC)

* C101	D-1	* C211	A-2	CN101	H-9	IC123	J-2	* R017	D-4	* R168	J-2	* R255	D-3	* R340	E-9
* C102	D-2	* C212	A-2	CN102	H-9	IC124	J-2	* R018	C-4	* R169	J-2	* R256	D-3	* R341	F-6
* C103	G-1	* C213	A-2	CN103	L-5	IC125	J-2	* R019	C-3	* R170	M-2	* R257	D-3	* R342	E-6
* C104	G-2	* C214	A-2	CN104	A-4	IC126	K-2	* R020	C-3	* R171	M-2	* R258	D-3	* R343	E-8
* C105	G-2	* C215	A-1	CN105	A-2	IC127	K-2	* R021	D-4	* R172	M-2	* R259	D-3	* R343	L-7
* C106	F-4	* C216	A-1	CN106	A-6	IC128	C-4	* R022	D-4	* R173	M-2	* R260	D-3	* R344	F-9
* C107	G-3	* C217	A-6	CN108	C-5	* IC129	A-5	* R023	D-4	* R174	M-1	* R261	D-4	* R345	D-6
* C108	D-3	* C218	A-7	CN109	E-5	IC131	B-3	* R030	J-7	* R175	M-1	* R262	D-4	* R346	F-8
* C109	E-3	* C219	A-7	CN110	A-8	* IC132	C-3	* R031	J-7	* R176	M-1	* R263	D-3	* R347	D-8
* C110	E-3	* C220	A-8	CN111	J-5	IC133	B-2	* R032	J-6	* R177	M-1	* R264	D-4	* R348	D-9
* C111	E-4	* C221	A-8	CN112	B-1	* IC134	B-2	* R033	J-7	* R178	M-1	* R265	D-3	* R349	D-9
* C112	D-4	* C222	A-9	CN113	B-1	* IC135	B-1	* R034	J-6	* R179	M-2	* R267	D-3	* R350	D-9
* C113	D-4	* C224	A-9	CN114	B-1	* IC136	B-2	* R035	J-7	* R180	M-2	* R268	D-3	* R351	D-9
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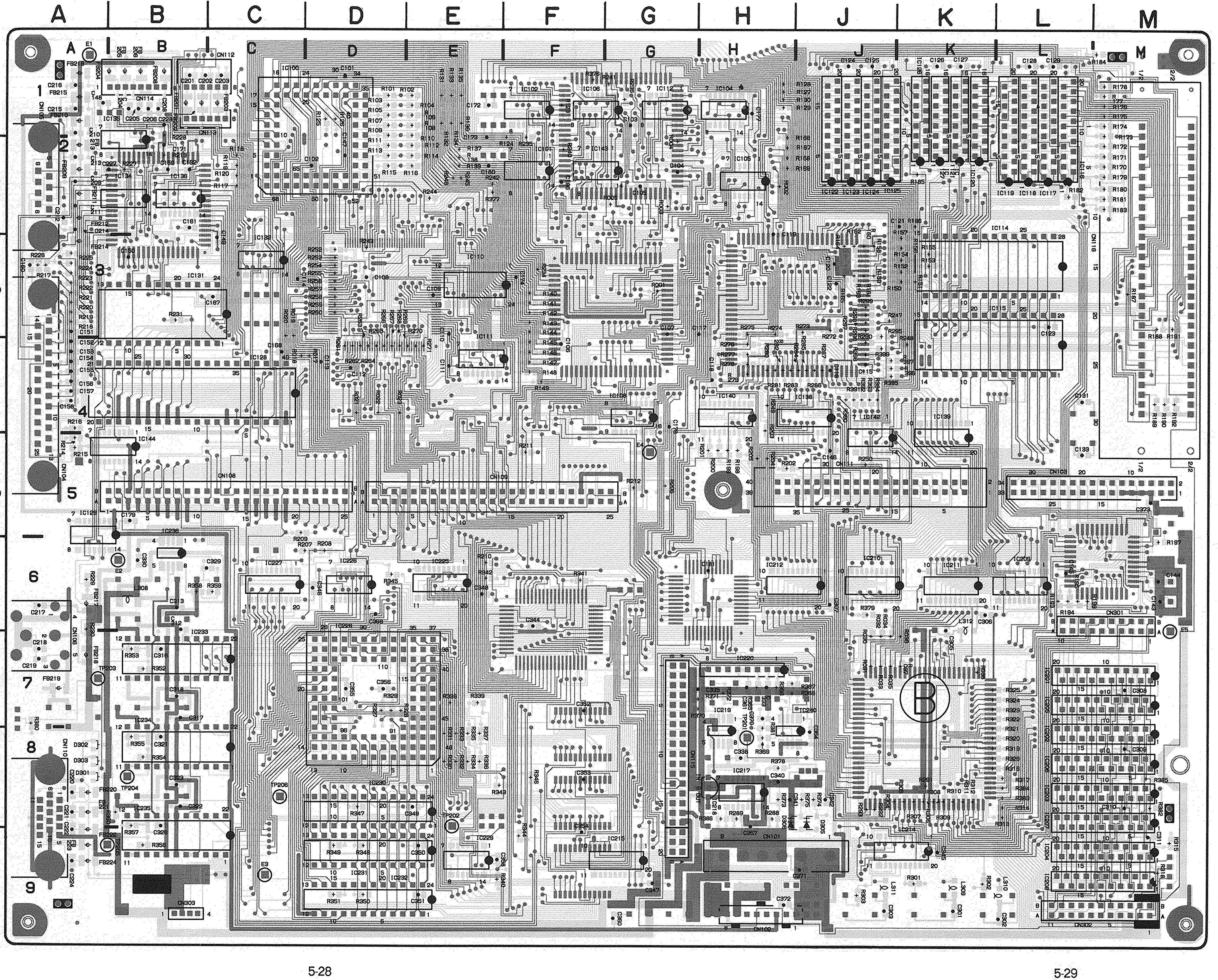
* C115	J-4	* C228	B-1	CN116	M-2	* IC138	J-4	* R037	K-7	* R182	L-2	* R270	E-3	* R353	B-7
* C116	J-4	* C301	K-9	CN301	M-6	* IC139	K-4	* R038	K-7	* R183	M-2	* R271	E-4	* R354	B-8
* C117	H-3	* C302	L-9	CN302	M-9	* IC140	H-4	* R101	D-1	* R184	M-1	* R272	J-3	* R355	B-8
* C118	H-4	* C303	J-9	CN303	B-9	IC141	H-6	* R102	E-1	* R185	K-2	* R273	J-3	* R356	B-9
* C119	H-2	C304	K-6			* IC142	J-4	* R103	D-1	* R186	K-2	* R274	H-3	* R357	B-9
* C120	J-3	* C305	K-7	* D301	A-8	* IC143	F-2	* R104	E-1	* R187	M-3	* R275	H-3	* R358	B-6
* C121	K-2	* C306	K-6	* D302	A-8	* IC144	B-5	* R105	D-1	* R188	M-3	* R276	H-4	* R359	C-6
* C122	J-3	* C307	J-6	* D303	A-8	IC201	L-7	* R106	E-1	* R189	M-4	* R277	H-4	* R360	B-8
* C123	L-3	* C308	M-7	* D305	J-8	IC202	L-7	* R107	D-1	* R190	M-4	* R278	H-4	* R365	H-7
* C124	J-1	* C309	M-8	* D306	H-8	IC203	L-8	* R108	E-1	* R191	M-3	* R279	H-4	* R366	H-7
* C125	J-1	* C310	M-8			IC204	L-9	* R109	D-1	* R192	M-4	* R280	H-4	* R367	J-7
* C126	K-1	* C311	M-9	DL100	C-3	IC205	L-7	* R110	E-2	* R193	L-6	* R281	H-4	* R368	J-7
* C127	K-1	* C312	B-6			IC206	L-8	* R111	D-2	* R194	L-6	* R282	H-4	* R369	H-8
* C128	L-1	* C313	B-6	E1	A-1	IC207	L-8	* R112	E-2	* R195	L-6	* R283	H-4	* R370	H-7
* C129	L-1	C314	B-6	E2	B-6	IC208	L-9	* R113	D-2	* R196	M-6	* R284	J-4	* R371	H-7
C130	L-4	C315	B-6	E3	C-9	* IC209	L-6	* R114	E-2	* R197	M-6	* R285	J-4	* R372	H-7
* C131	L-4	* C316	B-7	E4	G-5	* IC210	J-6	* R115	D-2	* R198	H-5	* R286	J-4	* R373	H-8
C132	L-4	* C317	B-7	E5	M-6	* IC211	K-6	* R116	E-2	* R199	H-5	* R287	J-4	* R374	J-8
* C133	L-5	* C318	B-7			* IC212	H-6	* R117	C-2	* R200	H-5	* R288	H-8	* R375	J-8
C137	C-6	C319	B-7	* FB201	B-1	IC213	J-7	* R118	C-2	* R201	H-5	* R289	H-8	* R376	F-1
C138	G-9	C320	B-7	* FB202	B-1	* IC214	K-9	* R119	C-2	* R202	H-5	* R290	J-4	* R377	E-2
C139	J-9	* C321	B-8	* FB203	C-1	* IC215	G-9	* R120	C-2	* R203	H-4	* R291	K-8	* R378	H-8
C141	H-9	* C322	B-8	* FB204	A-1	* IC217	H-8	* R123	F-1	* R204	H-5	* R292	J-8	* R379	J-6
C142	H-9	* C323	B-8	* FB205	B-1	IC218	H-8	* R124	F-2	* R205	H-5	* R293	J-8	* R380	A-7
* C143	M-6	C324	B-8	* FB206	B-1	* IC219	H-7	* R125	D-1	* R206	G-5	* R295	J-3	* R381	H-7
* C144	M-6	C325	B-8	* FB208	B-1	IC220	H-7	* R126	D-1	* R207	D-6	* R296	J-3	* R382	M-8
* C145	L-6	* C326	B-9	* FB209	A-2	IC221	F-7	* R127	J-1	* R208	D-6	* R297	J-3	* R383	L-8
* C146	J-5	C327	B-6	* FB210	A-1	IC222	F-8	* R128	J-1	* R209	C-5	* R298	J-3	* R384	L-8
* C147	D-2	C328	B-6	* FB211	A-2	IC223	F-9	* R129	J-1	* R210	E-6	* R299	J-3	* R385	M-8
* C148	A-1	* C329	C-6	* FB212	A-2	IC224	F-6	* R130	J-1	* R211	F-5	* R301	K-9	* R386	H-8
* C149	C-3	* C330	B-6	* FB213	A-2	* IC225	E-6	* R131	E-1	* R212	G-5	* R302	K-9	* R390	J-4
* C150	B-3	C332	H-7	* FB214	A-3	* IC226	D-6	* R132	E-2	* R213	B-2	* R303	J-9	* R391	J-4
* C151	A-3	* C333	H-7	* FB215	A-1	* IC227	C-6	* R133	E-1	* R214	A-5	* R304	J-8	* R392	J-4
* C152	A-4	C334	J-7	* FB216	A-1	IC228	D-6	* R134	E-2	* R215	A-5	* R305	K-8	* R393	J-4
* C153	A-4	* C335	H-7	* FB217	A-6	* IC229	E-9	* R135	E-1	* R216	A-4	* R306	K-8	* R394	J-4
* C154	A-4	C336	H-7	* FB218	A-7	IC230	D-8	* R136	E-1	* R217	A-3	* R307	K-8	* R395	J-4
* C155	A-4	C337	H-8	* FB219	A-7	IC231	D-9	* R137	E-2	* R218	A-3	* R308	K-8	* R396	K-4
* C156	A-4	* C338	H-8	* FB220	A-8	IC232	D-9	* R138	E-2	* R219	A-3	* R309	K-8	* R397	K-4
* C157	A-4	C339	H-7	* FB221	A-8	IC233	C-7	* R139	E-2	* R220	A-3	* R310	K-8	* R398	J-4
* C158	A-4	* C340	H-8	* FB222	A-9	IC234	C-7	* R140	F-3	* R221	A-3	* R311	K-8	* R399	J-4
* C159	B-2	* C341	J-8	* FB223	A-9	IC235	C-8	* R141	F-3	* R222	A-3	* R312	K-8		
* C160	A-3	* C342	J-8	* FB224	A-9	* IC236	B-5	* R142	F-3	* R223	A-3	* R313	L-8	SW301	A-7
* C161	B-2	C343	H-8	FB301	M-5	* IC240	J-7	* R143	F-3	* R224	A-3	* R314	L-8		
* C162	B-2	* C344	F-6					* R144	F-3	* R225	A-3	* R315	M-9	TH301	A-7
* C167	C-3	* C345	K-9	IC100	D-1	JP201	G-6	* R145	F-4	* R226	A-3	* R316	L-8	TH302	A-7
* C168	C-4	* C346	D-6	* IC101	F-2	JP202	E-8	* R146	F-4	* R227	B-2	* R317	L-8		
C169	A-7	* C347	G-9	* IC102	F-1	JP204	M-9	* R147	F-4	* R228	B-2	* R318	M-9	TP201	H-7
* C171	B-2	* C348	E-6	IC103	G-1	JP205	M-9	* R148	F-4	* R229	A-6	* R319	L-8	TP202	E-8
* C172	E-1	* C349	E-8	* IC104	H-1			* R149	F-4	* R230	A-6	* R320	L-8	TP203	A-7
* C173	E-2	* C350	E-9	* IC105	H-2	L307	J-8	* R150	J-3	* R231	B-3	* R321	L-7	TP204	B-8
* C174	F-3	* C351	E-9	* IC106	F-1	* L308	B-6	* R151	K-3	* R234	F-3	* R322	L-7	TP205	A-9
C175	M-5	* C352	F-7	IC107	F-3	* L309	K-9	* R152	K-3	* R235	F-2	* R324	L-7	TP206	C-8
* C177	H-1	* C353	F-8	* IC108	G-4	* L310	L-9	* R153	K-3	* R236	G-1	* R325	L-7		
* C178	G-4	* C354	F-8	IC109	D-3	* L311	J-9	* R154	K-3	* R240	F-2	* R326	L-8	WL101	A-5
* C179	B-5	* C355	D-7	* IC110	E-3	* L312	K-6	* R155	K-3	* R241	G-1	* R327	D-7		
* C180	E-2	* C356	D-7	* IC111	E-4	L313	B-6	* R156	K-3	* R242	E-2	* R328	E-7	X100	M-6
* C181	H-6	* C357	H-9	* IC112	G-1			* R157	K-2	* R243	D-3	* R329	D-7	X201	K-9
* C186	F-2	* C358	E-9	IC113	H-2	OSC100	E-1	* R158	J-3	* R244	E-2	* R330	E-8	X202	K-9
* C201	B-1	C359	G-9	IC114	L-2	OSC101	E-1	* R159	J-3	* R245	E-2	* R331	E-8	X203	J-9
* C202	B-1	* C360	G-9	IC115	L-3	OSC102	A-1	* R160	J-2	* R246	E-2	* R332	E-8		
* C203	C-1	* C361	H-7	IC116	L-2	OSC103	E-2	* R161	J-3	* R247	J-3	* R333	E-8		
* C204	B-1	* C364	J-8	IC117	L-2			* R162	J-2	* R248	K-4	* R334	E-8		
* C205	B-1	* C368	D-6	IC118	L-2	* R001	G-3	* R163	J-3	* R249	H-4	* R335	E-8		
* C206	B-1	* C370	H-7	IC119	L-2	* R002	H-2	* R164	J-3	* R250	J-5	* R336	E-8		
* C208	B-1	* C371	J-9	IC120	K-2	* R003	G-2	* R165	J-3	* R252	D-3	* R337	E-8		
* C209	A-2	* C372	H-9	IC121	K-2	* R004	G-2	* R166	J-2	* R253	D-3	* R338	E-7		
* C210	A-1	* C373	M-5	IC122	J-2	* R005	G-2	* R167	J-2	* R254	D-3	* R339	E-7		

* ;
SOLDERING SIDE


A
B
C
D
E
F
G
H
J
K
L
M
1
2
3
4
5
6
7
8
9
B

SY-143 – SOLDERING SIDE –

1-630-412-11
VIW-5000(UC)

AT CONTROL LOGIC
103
CPU
100
AT PERIPHERAL CONTROL LOGIC
107
ADDRESS BUFFER AND MEMORY CONTROLLER
109
DUS-307
IC001
108
DL100
OSC101 14.31818MHz
OSC100 20MHz
OSC103 16MHz
CN108
CN109
TO CN702/MB-232
TO CN701/MB-232
FROM CN701/MB-232
FROM CN702/MB-232
TO/FROM CN702/MB-232
TO/FROM CN701/MB-232
ED2,ED3,ED6,ED7
ED0-ED7
A0,A1,A3
A0-A23
SA0-SA19
RA0-RA9
IOR
IOW
YMEMR
DLYWR
MASTER
CPUCLK
REFRESH
HLDA
BALE
AEN01
D0-D15
NO MOUNTED
2/4
3/4
2/4,3/4,4/4
+5V
+12V
-5V
-12V
GND
N.C.
ERROR

DUS-307

Ref. No.	TYPE	PIN No.	
		+5V	GND
IC001	74F373SJ	20	10

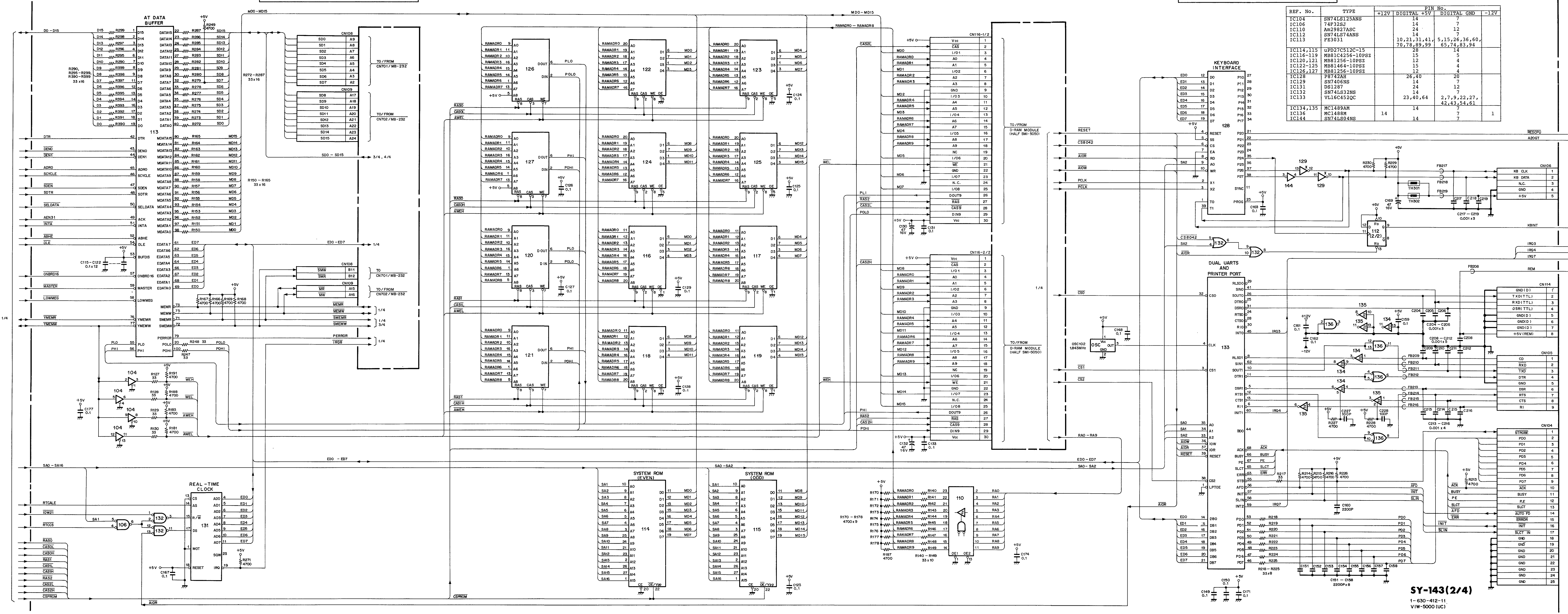
REF. No.	TYPE	PIN No.	
		DIGITAL +5V	DIGITAL GND
IC100	N80286-10	30,62	9,35,60
IC101	74F08SJ	14	7
IC102	SN74LS125ANS	14	7
IC103	FE3001	19,51,74	2,12,23,38,44,65
IC105	74F04SJ	14	7
IC106	74F32SJ	14	7

REF. No.	TYPE	PIN No.	
		DIGITAL +5V	DIGITAL GND
IC107	FE3010B	43,84	1,22,42,64
IC108	SN74LS138NS	16	8
IC109	FE3021	7,30,50,55, 77,92,107	1,27,29,42,51,67, 76,91,99,108,124
IC112	SN74LS74ANS	14	7
IC143	SN74LS04NS	14	7

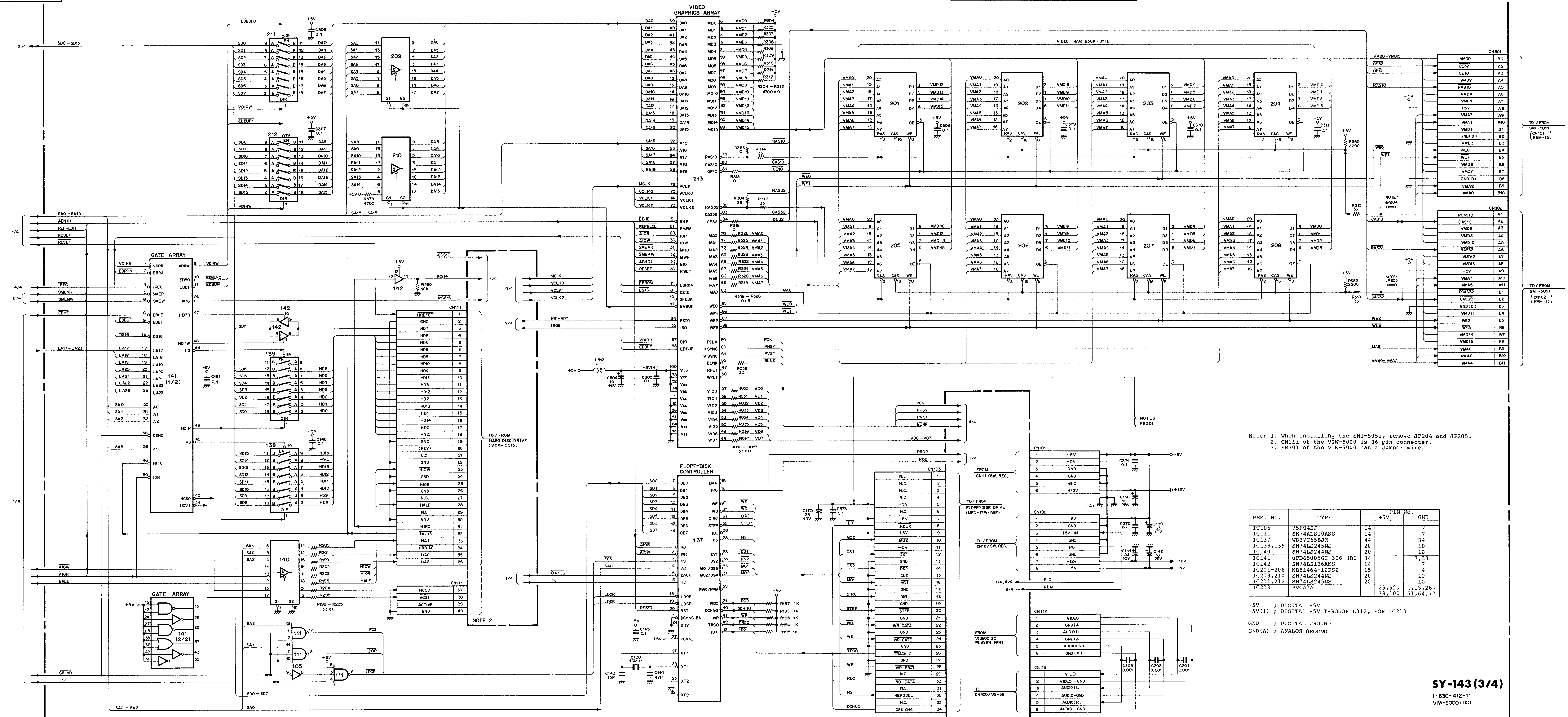
SY-143 (1/4)

1-630-412-11
VIW-5000(UC)

REF. No.	TYPE	PIN No.			
		+12V	DIGITAL +5V	DIGITAL GND	-12V
IC104	SN74LS125ANS		14	7	
IC106	74F32SJ		14	7	
IC110	Am29827ASC		24	12	
IC112	SN74LS74ANS		14	7	
IC113	FE3031		10,21,31,41, 70,78,89,99	5,15,26,36,60, 65,74,83,94	
IC114,115	uPD27C512C-15		28	14	
IC116-119	MB81C4256-10PSZ		15	5	
IC120,121	MB81256-10PSZ		12	4	
IC122-125	MB81464-10PSZ		15	4	
IC126,127	MB81256-10PSZ		12	4	
IC128	P8742AH		26,40	20	
IC129	SN7406NS		14	7	
IC131	DS1287		24	12	
IC132	SN74LS32NS		14	7	
IC133	VL16C452QC		23,40,64	2,7,9,22,27, 42,43,54,61	
IC134,135	MC1489AM		14	7	
IC136	MC1488M	14		7	1
IC144	SN74LS04NS		14	7	


AT DATA BUFFER
113
REAL-TIME CLOCK
131
SYSTEM ROM (EVEN)
114
SYSTEM ROM (ODD)
115
126
127
120
121
122
123
124
125
116
117
118
119
110
KEYBOARD INTERFACE
128
DUAL UARTS AND PRINTER PORT
133
OSC102 1.8432MHz
CN108
CN109
CN116-1/2
CN116-2/2
CN106 KEYBOARD (EXT. VIEW)
CN114 TO / FROM VIDEODISC PLAYER PART
CN105 RS-232C (EXT. VIEW)
CN104 PRINTER (EXT. VIEW)
TO / FROM CN701 / MB-232
TO / FROM CN702 / MB-232
TO / FROM D-RAM MODULE (HALF SMI-5050)
DO - D15
MD0 - MD15
SD0 - SD15
ED0 - ED7
SA0 - SA16
RAMADR0 - RAMADR8
1/4
3/4, 4/4
3/4
+5V
-12V
+12V

SY-143(2/4)
1-630-412-11
VIW-5000(UC)


VIDEO GRAPHICS ARRAY
213
GATE ARRAY
141 (1/2)
141 (2/2)
FLOPPYDISK CONTROLLER
137
VIDEO RAM 256K-BYTE
201
202
203
204
205
206
207
208
209
210
211
212
138
139
140
142
111
105
CN111
TO / FROM HARD DISK DRIVE (SCK-5015)
NOTE 2
CN103
TO / FROM FLOPPYDISK DRIVE (MFD-17W-53E)
CN101
FROM CN11 / SW. REG.
CN102
TO / FROM CN12 / SW. REG.
CN112
FROM VIDEODISC PLAYER PART
CN113
TO CN400 / VS-39
CN301
TO / FROM SMI-5051 (CN101 / RAM-13)
CN302
TO / FROM SMI-5051 (CN102 / RAM-13)
NOTE 1 JP204
NOTE 1 JP205
NOTE 3 FB301
X100 16MHz
L312
1/4
2/4
4/4
1/4, 4/4
+5V
+12V
-12V
-5V

Note: 1. When installing the SMI-5051, remove JP204 and JP205.
2. CN111 of the VIW-5000 is 36-pin connecter.
3. FB301 of the VIW-5000 has a Jumper wire.

REF. No.	TYPE	PIN No.		
		+5V		GND
			1	
IC105	75F04SJ	14		7
IC111	SN74ALS10ANS	14		7
IC137	WD37C65BJM	44		34
IC138,139	SN74LS245NS	20		10
IC140	SN74LS244NS	20		10
IC141	uPD65005GC-306-3B6	34		7,33
IC142	SN74LS126ANS	14		7
IC201-208	MB81464-10PSZ	15		4
IC209,210	SN74LS244NS	20		10
IC211,212	SN74LS245NS	20		10
IC213	PVGA1A		25,52, 78,100	1,15,26, 51,64,77

+5V ; DIGITAL +5V
+5V(1) ; DIGITAL +5V THROUGH L312, FOR IC213

GND ; DIGITAL GROUND
GND(A) ; ANALOG GROUND

SY-143 (3/4)

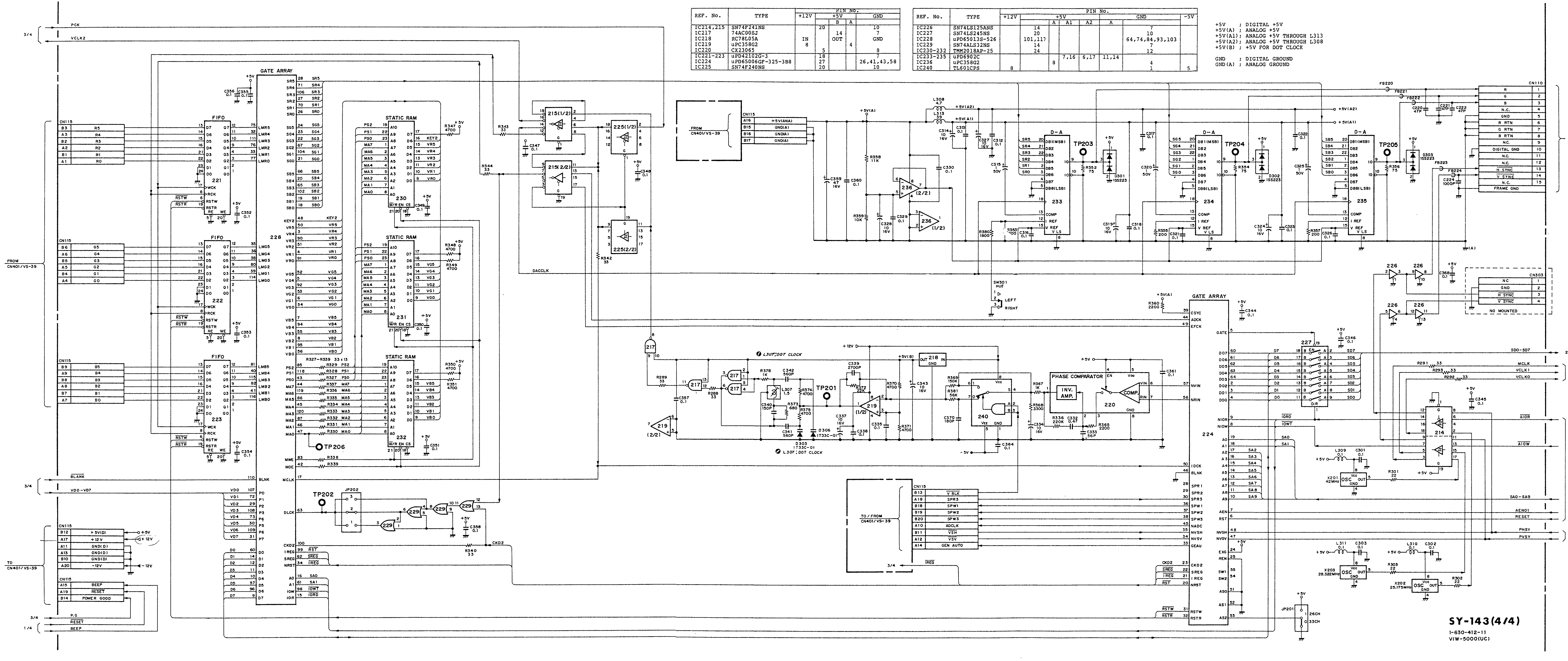
1-630-412-11
VIW-5000 (UC)

REF. No.	TYPE	PIN No.				
		+12V	+5V			GND
				B	A	
IC214,215	SN74F241NS		20			10
IC217	74AC00SJ			14		7
IC218	RC78L05A	IN		OUT		GND
IC219	uPC358G2	8			4	
IC220	CX23065		5			8
IC221-223	uPD42102G-3		18			7
IC224	uPD65006GF-325-3B8		27			26,41,43,58
IC225	SN74F240NS		20			10

REF. No.	TYPE	PIN No.						
		+12V	+5V				GND		-5V
				A	A1	A2	A		
IC226	SN74LS125ANS		14					7	
IC227	SN74LS245NS		20					10	
IC228	uPD65013S-526		101,117					64,74,84,93,103	
IC229	SN74ALS32NS		14					7	
IC230-232	TMM2018AP-25		24					12	
IC233-235	uPD6902C				7,16	6,17	11,14		
IC236	uPC358G2			8				4	
IC240	TL601CPS	8						1	5

+5V ; DIGITAL +5V
+5V(A) ; ANALOG +5V
+5V(A1); ANALOG +5V THROUGH L313
+5V(A2); ANALOG +5V THROUGH L308
+5V(B) ; +5V FOR DOT CLOCK

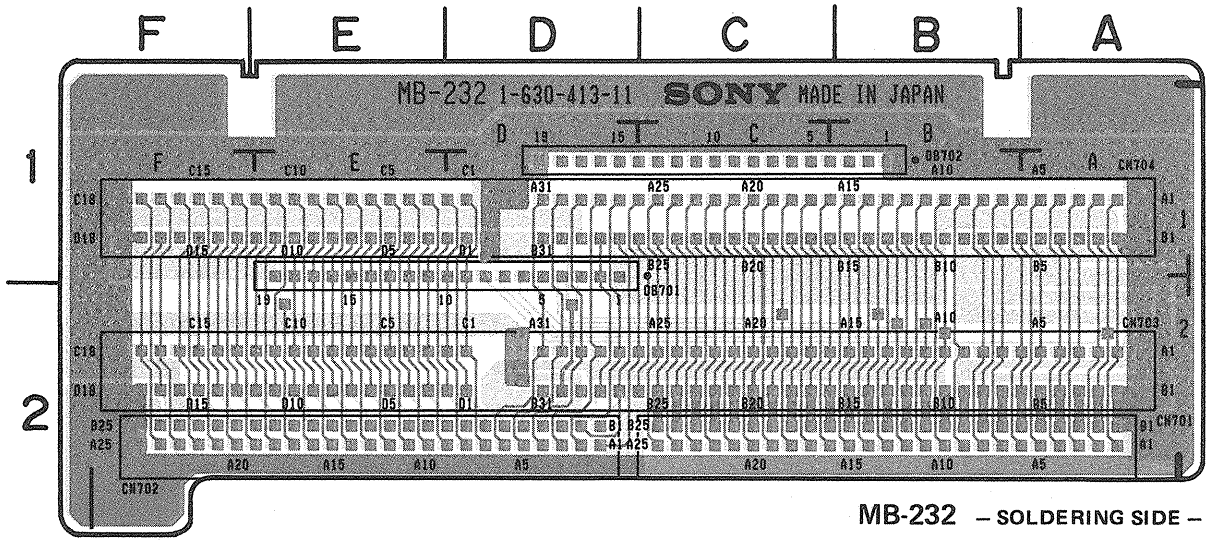
GND ; DIGITAL GROUND
GND(A) ; ANALOG GROUND



PCK
VCLK2
GATE ARRAY
FIFO
221
222
223
228
STATIC RAM
230
231
232
215(1/2)
215(2/2)
225(1/2)
225(2/2)
CN115
FROM CN401/VS-39
TO CN401/VS-39
TO / FROM CN401/VS-39
BLANK
VD0–VD7
+5V(D)
+12V
GND(D)
-12V
BEEP
RESET
POWER GOOD
P.G
DACCLK
TP201
TP202
TP203
TP204
TP205
TP206
JP202
JP201
D-A
233
234
235
236
217
219
220
229
240
218
PHASE COMPARATOR
INV. AMP.
COMP.
L30F,DOT CLOCK
SW301
LEFT
RIGHT
GATE ARRAY
224
226
227
214
CN110
ANALOG RGB OUT
(EXT.VIEW)
CN303
NO MOUNTED
R
G
B
N.C.
GND
R RTN
G RTN
B RTN
DIGITAL GND
H SYNC
V SYNC
FRAME GND
SD0–SD7
MCLK
VCLK1
VCLK0
IOR
IOW
SA0–SA9
AEN01
RESET
PHSY
PVSY
OSC
X201
X202
X203
26CH
33CH
3/4
1/4

SY-143(4/4)
1-630-412-11
VIW-5000(UC)

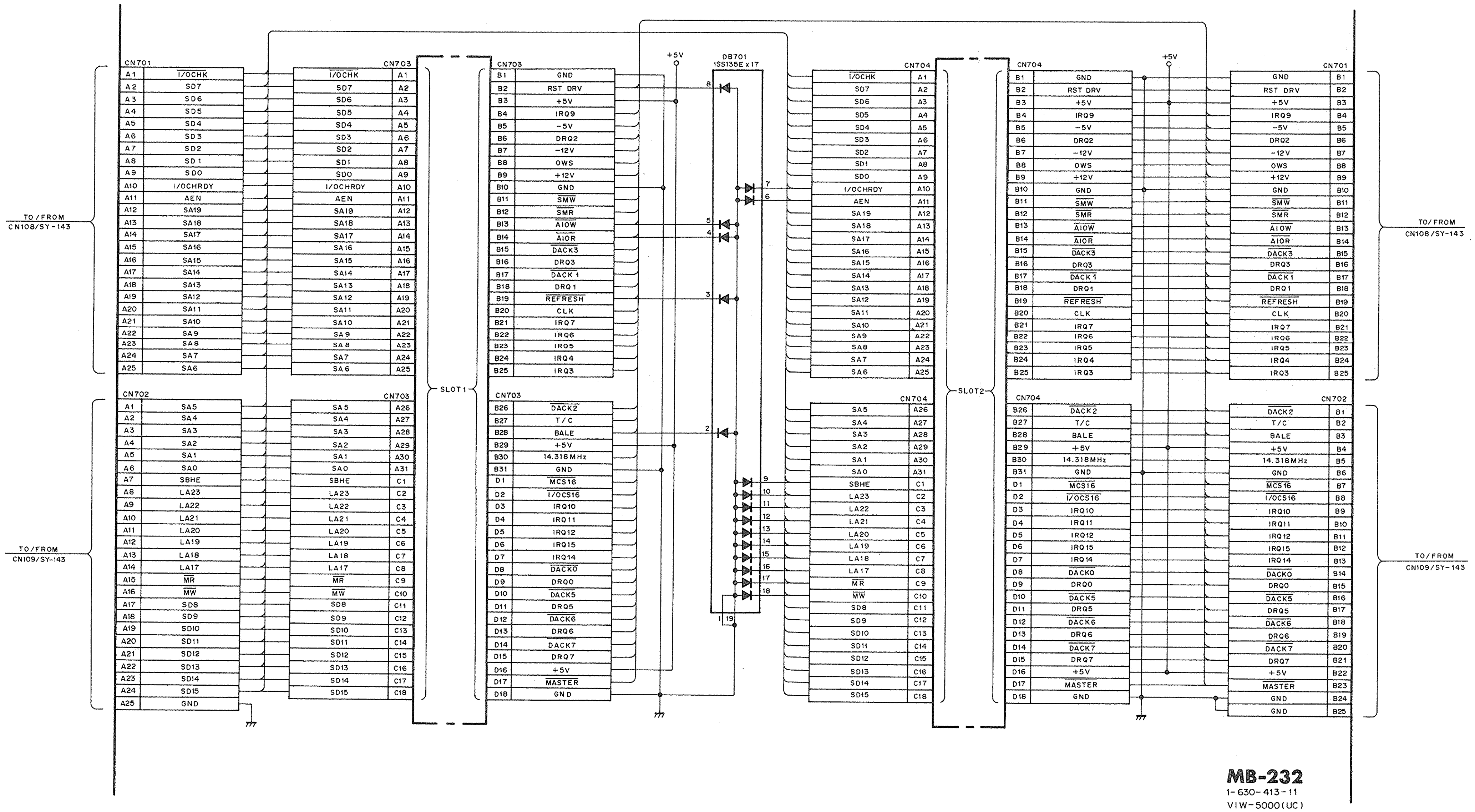
5-4. MB-232 BOARD


F
E
D
C
B
A
1
2
MB-232 1-630-413-11 SONY MADE IN JAPAN
CN701
CN702
CN703
CN704
DB701
DB702

CN701	A-2
CN702	F-2
CN703	A-2
CN704	A-1
DB701	C-2
DB702	B-1

MB-232 – SOLDERING SIDE –

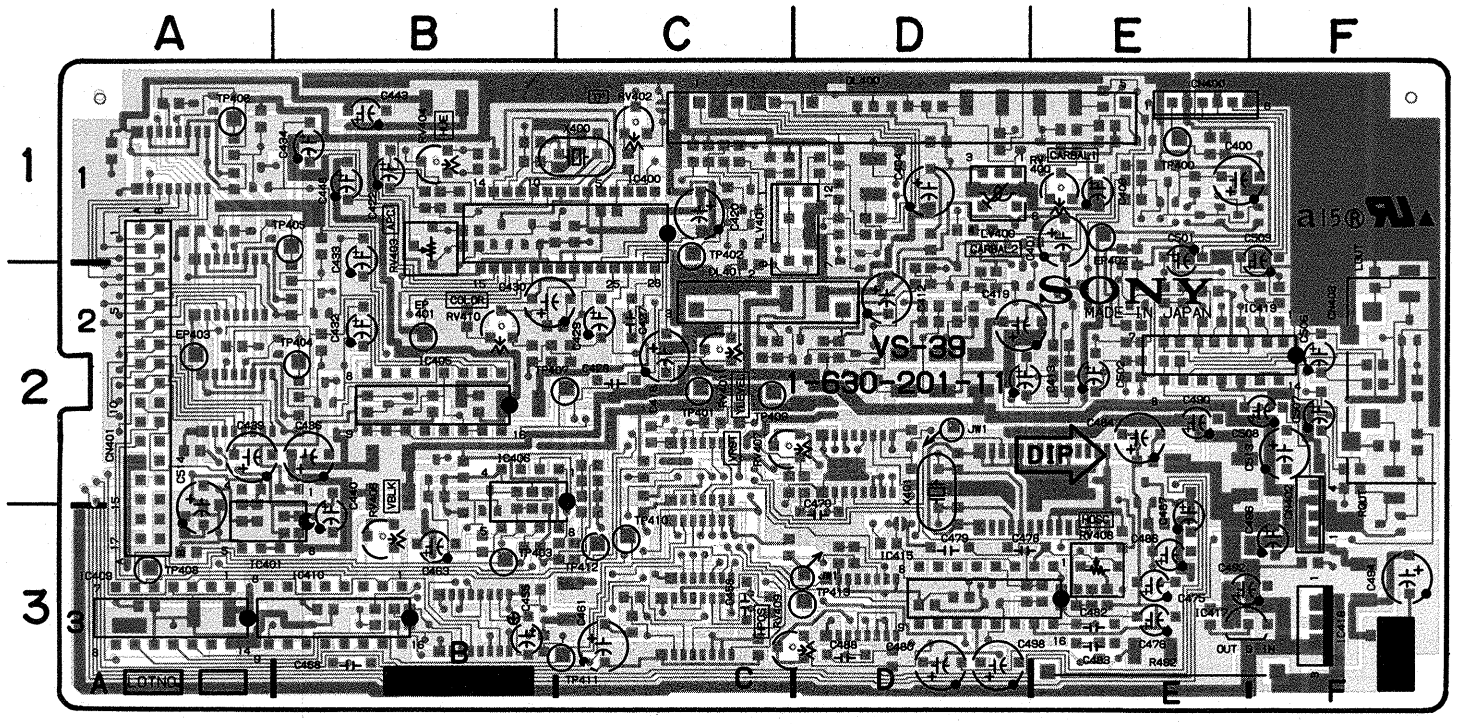
1-630-413-11
VIW-5000(UC)


CN701
CN702
CN703
CN704
SLOT1
SLOT2
DB701
1SS135E x 17
+5V
TO / FROM CN108 / SY-143
TO / FROM CN109 / SY-143
I/OCHK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
I/OCHRDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
SBHE
LA23
LA22
LA21
LA20
LA19
LA18
LA17
MR
MW
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
GND
RST DRV
+5V
IRQ9
-5V
DRQ2
-12V
OWS
+12V
SMW
SMR
AIOW
AIOR
DACK3
DRQ3
DACK1
DRQ1
REFRESH
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
T/C
BALE
14.318MHz
MCS16
I/OCS16
IRQ10
IRQ11
IRQ12
IRQ15
IRQ14
DACK0
DRQ0
DACK5
DRQ5
DACK6
DRQ6
DACK7
DRQ7
MASTER

MB-232
1-630-413-11
VIW-5000(UC)

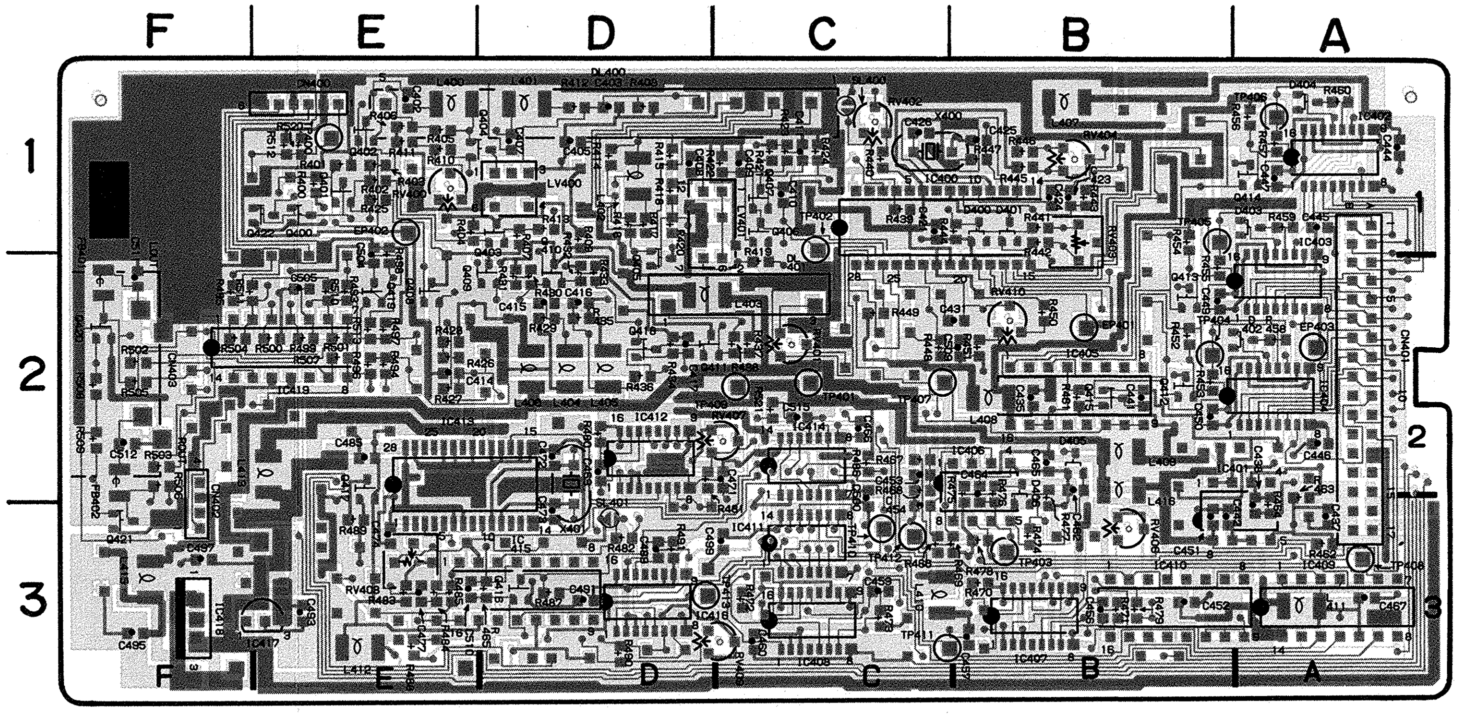
5-5. VS-39 BOARD

C400	E-1	* C460	C-3	* D400	B-1	LV400	D-1	* R433	D-2	* R493	E-2
C401	E-1	C461	C-3	* D401	B-1	LV401	C-1	* R434	D-2	* R494	E-2
* C402	E-1	* C462	B-3	* D402	A-2			* R435	D-2	* R495	F-2
* C403	D-1	C463	B-3	* D403	A-1	* Q400	E-1	* R436	D-2	* R496	E-2
C404	D-1	* C464	B-2	* D404	A-1	* Q401	E-1	* R437	C-2	* R497	E-2
* C405	D-1	* C465	B-2	* D405	B-2	* Q402	E-1	* R438	C-2	* R498	E-1
C406	E-1	* C466	C-2	* D406	B-3	* Q403	D-1	* R439	C-1	* R499	E-2
* C407	D-1	* C467	A-3			* Q404	D-1	* R440	C-1	* R500	E-2
* C408	D-1	C468	B-3	DL400	D-1	* Q405	D-2	* R441	B-1	* R501	E-2
* C409	C-1	* C469	D-2	DL401	C-2	* Q406	C-1	* R442	B-1	* R502	F-2
* C410	C-1	C470	D-3			* Q407	C-1	* R443	B-1	* R503	F-2
* C411	C-1	* C471	C-2	EP401	B-2	* Q408	E-2	* R444	C-1	* R504	F-2
C412	D-2	* C472	D-2	EP402	E-1	* Q409	E-2	* R445	B-1	* R505	F-2
C413	E-2	* C473	D-3	EP403	A-2	* Q410	D-1	* R446	B-1	* R506	F-2
* C414	E-2	* C474	E-3			* Q411	D-2	* R447	B-1	* R507	E-2
* C415	D-2	C475	E-3	* FB401	F-1	* Q412	B-2	* R448	C-2	* R508	F-2
* C416	D-2	C476	E-3	* FB402	F-3	* Q413	B-2	* R449	C-2	* R509	F-2
* C417	D-2	* C477	E-3			* Q414	A-1	* R450	B-2	* R510	E-2
C418	C-2	C478	D-3	IC400	C-1	* Q415	B-2	* R451	B-2	* R511	F-2
C419	D-2	C479	D-3	IC401	A-3	* Q416	D-3	* R452	B-2	* R512	E-1
C420	C-1	C480	D-3	* IC402	A-1	* Q417	E-2	* R453	B-2	* R513	E-2
* C421	C-1	C482	E-3	* IC403	A-1	* Q418	D-2	* R454	B-1	* R520	E-1
C422	B-1	C483	E-3	* IC404	A-2	* Q419	E-2	* R455	B-2	* R521	C-2
* C423	B-1	C484	E-2	IC405	B-2	* Q420	F-2	* R456	A-1		
* C424	B-1	* C485	E-2	IC406	B-2	* Q421	F-3	* R457	A-1	RV400	E-1
* C425	B-1	C486	E-3	* IC407	B-3	* Q422	E-1	* R458	A-2	RV401	C-2
* C426	C-1	C487	E-3	* IC408	C-3			* R459	A-1	RV402	C-1
C427	C-2	C488	D-3	IC409	A-3	* R400	E-1	* R460	A-1	RV403	B-1
C428	C-2	* C489	D-3	IC410	B-3	* R401	E-1	* R461	B-2	RV404	B-1
C429	C-2	C490	E-2	* IC411	C-3	* R402	E-1	* R462	A-3	RV406	B-3
C430	B-2	* C491	D-3	* IC412	D-2	* R403	E-1	* R463	A-2	RV407	C-2
* C431	B-2	C492	E-3	* IC413	E-2	* R404	E-1	* R464	A-3	RV408	E-3
C432	B-2	* C493	E-3	* IC414	C-2	* R405	E-1	* R465	D-3	RV409	C-3
C433	B-1	C494	F-3	IC415	D-3	* R406	E-1	* R466	C-3	RV410	B-2
C434	B-1	* C495	F-3	* IC416	D-3	* R407	D-1	* R467	C-2		
* C435	B-2	C496	F-3	IC417	E-3	* R408	D-1	* R468	C-2	* SL400	C-1
C436	B-2	* C497	F-3	IC418	F-3	* R409	D-1	* R469	B-3	* SL401	D-3
* C437	A-3	C498	D-3	IC419	E-2	* R410	E-1	* R470	B-3		
* C438	A-2	* C499	D-3			* R411	E-1	* R471	B-3	TP400	E-1
C439	A-2	* C500	C-3	JW1	D-2	* R412	D-1	* R472	C-3	TP401	C-2
C440	B-2	C501	E-1	JW1	D-3	* R413	D-2	* R473	C-3	TP402	C-1
* C441	B-2	C502	E-2			* R414	D-1	* R474	B-3	TP403	B-3
* C442	A-3	C503	F-1	* L400	E-1	* R415	D-1	* R475	B-2	TP404	B-2
C443	B-1	* C504	E-1	* L401	D-1	* R416	D-1	* R476	B-3	TP405	B-1
* C444	A-1	* C505	E-2	* L402	D-1	* R417	D-1	* R477	B-3	TP406	A-1
* C445	A-1	C506	F-2	* L403	C-2	* R418	D-1	* R478	B-3	TP407	C-2
* C446	A-2	C507	F-2	* L404	D-2	* R419	C-1	* R479	B-3	TP408	A-3
* C447	A-1	C508	F-2	* L405	D-2	* R420	D-1	* R480	D-2	TP409	C-2
C448	B-1	* C509	C-2	* L406	D-2	* R421	C-1	* R481	C-3	TP410	C-3
* C449	B-2	* C510	E-3	* L407	B-1	* R422	D-1	* R482	D-3	TP411	C-3
* C450	B-2	* C511	F-1	* L408	B-2	* R423	C-1	* R483	E-3	TP412	C-3
* C451	B-3	* C512	F-2	* L409	B-2	* R424	C-1	* R484	E-3	TP413	D-3
* C452	B-3	C513	F-2	* L410	C-3	* R425	E-1	* R485	E-3		
* C453	C-2	C514	A-2	* L411	A-3	* R426	E-2	* R486	C-2	X400	C-1
* C454	C-3	* C515	C-2	* L412	E-3	* R427	E-2	* R487	D-3	X401	D-2
C455	B-3			* L413	F-2	* R428	E-2	* R488	E-3		
* C456	B-3	CN400	E-1	* L415	F-3	* R429	D-2	* R489	E-3		
* C457	B-3	* CN401	A-2	* L416	B-3	* R430	D-2	* R490	D-3	*;	
C458	C-3	CN402	F-2			* R431	D-2	* R491	D-3	SOLDERINGSIDE	
* C459	C-3	CN403	F-2			* R432	D-1	R492	E-3		



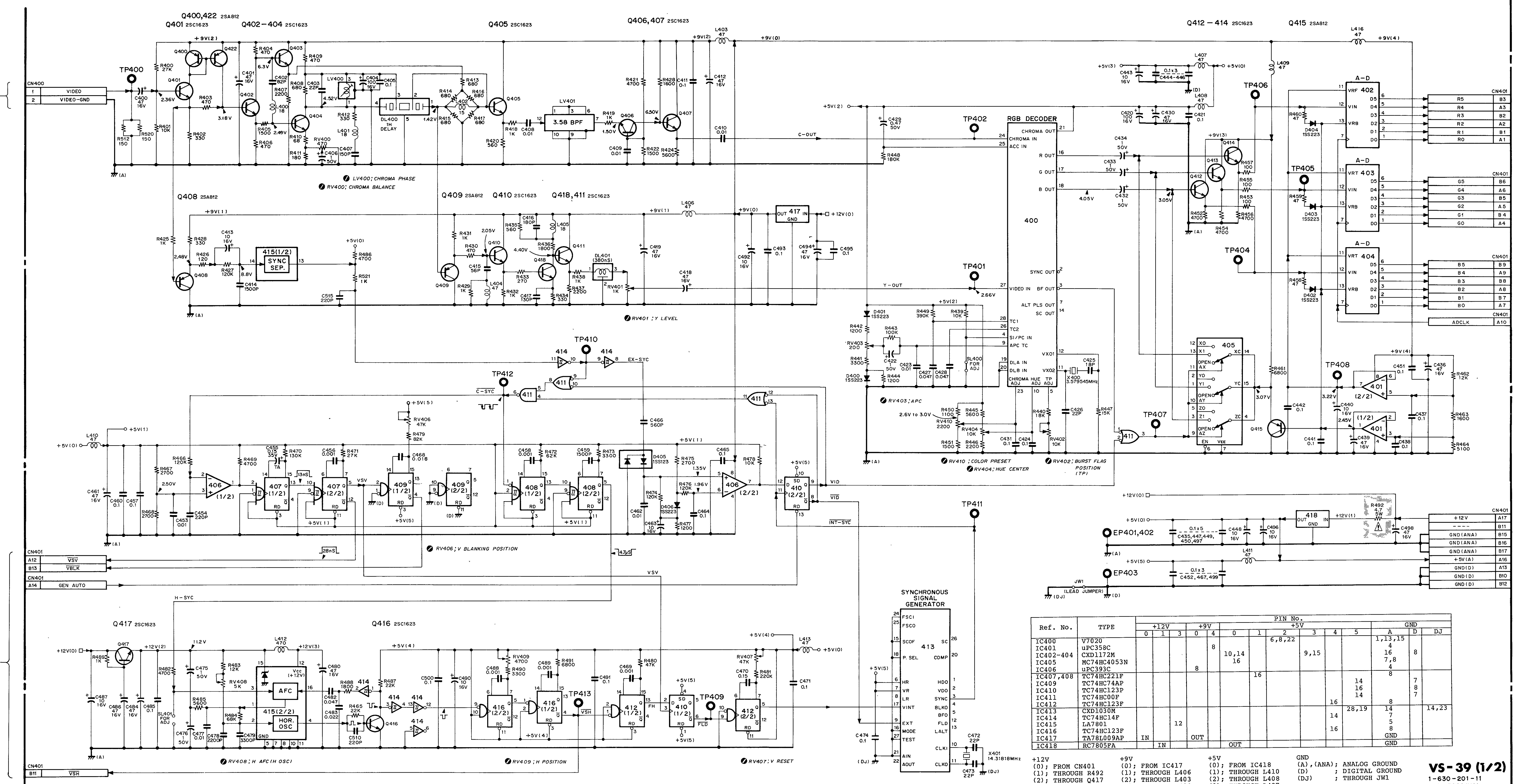
VS-39 – COMPONENT SIDE –

1-630-201-11
VIW-5000(UC)



VS-39 – SOLDERING SIDE –

1-630-201-11
VIW-5000(UC)


FROM CN113/SY-143
CN400
VIDEO
VIDEO-GND
TP400
Q400,422 2SA812
Q401 2SC1623
Q402-404 2SC1623
Q405 2SC1623
Q406,407 2SC1623
LV400
DL400 1H DELAY
LV401 3.58 BPF
C-OUT
LV400; CHROMA PHASE
RV400; CHROMA BALANCE
Q408 2SA812
Q409 2SA812
Q410 2SC1623
Q418,411 2SC1623
415(1/2) SYNC SEP.
DL401 (380nS)
RV401 ; Y LEVEL
417
Y-OUT
TP402
TP401
RGB DECODER
400
CHROMA OUT
CHROMA IN
ACC IN
R OUT
G OUT
B OUT
SYNC OUT
VIDEO IN
BF OUT
ALT PLS OUT
SC OUT
TC1
TC2
SI/PC IN
APC TC
DLA IN
DLB IN
VXO1
VXO2
CHROMA ADJ
HUE ADJ
TP ADJ
X400 3.579545MHz
RV403 ; APC
RV410 ; COLOR PRESET
RV404 ; HUE CENTER
RV402 ; BURST FLAG POSITION (TP)
Q412-414 2SC1623
Q415 2SA812
TP406
TP405
TP404
A-D 402
A-D 403
A-D 404
ADCLK
CN401
TO/FROM CN115/SY-143
405
TP407
TP408
401 (1/2)
401 (2/2)
TP410
TP412
414
411
EX-SYC
C-SYC
406 (1/2)
407 (1/2)
407 (2/2)
409 (1/2)
409 (2/2)
408 (1/2)
408 (2/2)
406 (2/2)
410 (2/2)
VID
INT-SYC
TP411
RV406 ; V BLANKING POSITION
VSV
VBLK
GEN AUTO
H-SYC
Q417 2SC1623
Q416 2SC1623
415(2/2)
AFC
HOR. OSC
416 (2/2)
416 (1/2)
412 (1/2)
410 (1/2)
412 (2/2)
TP413
TP409
VSH
FLD
RV408 ; H AFC(H OSC)
RV409 ; H POSITION
RV407 ; V RESET
SYNCHRONOUS SIGNAL GENERATOR
413
X401 14.31818MHz
418
EP401,402
EP403
JW1 (LEAD JUMPER)

Ref. No.	TYPE	PIN No.													
		+12V			+9V		+5V						GND		
		0	1	3	0	4	0	1	2	3	4	5	A	D	DJ
IC400	V7020								6,8,22				1,13,15		
IC401	uPC358C					8							4		
IC402-404	CXD1172M						10,14			9,15			16	8	
IC405	MC74HC4053N						16						7,8		
IC406	uPC393C				8								4		
IC407,408	TC74HC221F							16					8		
IC409	TC74HC74AP											14		7	
IC410	TC74HC123P											16		8	
IC411	TC74HC00F											14		7	
IC412	TC74HC123F										16		8		
IC413	CXD1030M											28,19	14		14,23
IC414	TC74HC14F										14		7		
IC415	LA7801			12									5		
IC416	TC74HC123F										16		8		
IC417	TA78L009AP	IN			OUT								GND		
IC418	RC7805FA		IN				OUT						GND		

+12V
(0); FROM CN401
(1); THROUGH R492
(2); THROUGH Q417
(3); THROUGH L412
(4); THROUGH L415

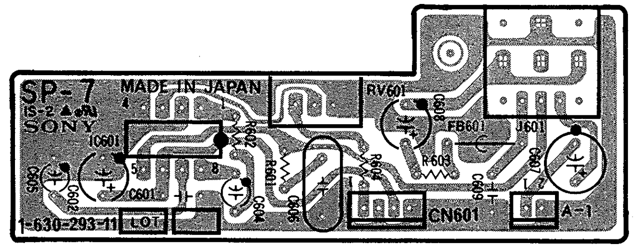
+9V
(0); FROM IC417
(1); THROUGH L406
(2); THROUGH L403
(3); THROUGH L409
(4); THROUGH L416

+5V
(0); FROM IC418
(1); THROUGH L410
(2); THROUGH L408
(3); THROUGH L407
(4); THROUGH L413
(5); THROUGH L411
(A); TO SY-143 BOARD

GND
(A),(ANA); ANALOG GROUND
(D) ; DIGITAL GROUND
(DJ) ; THROUGH JW1

VS-39 (1/2)
1-630-201-11
VIW-5000(UC)

5-6. SP-7 BOARD

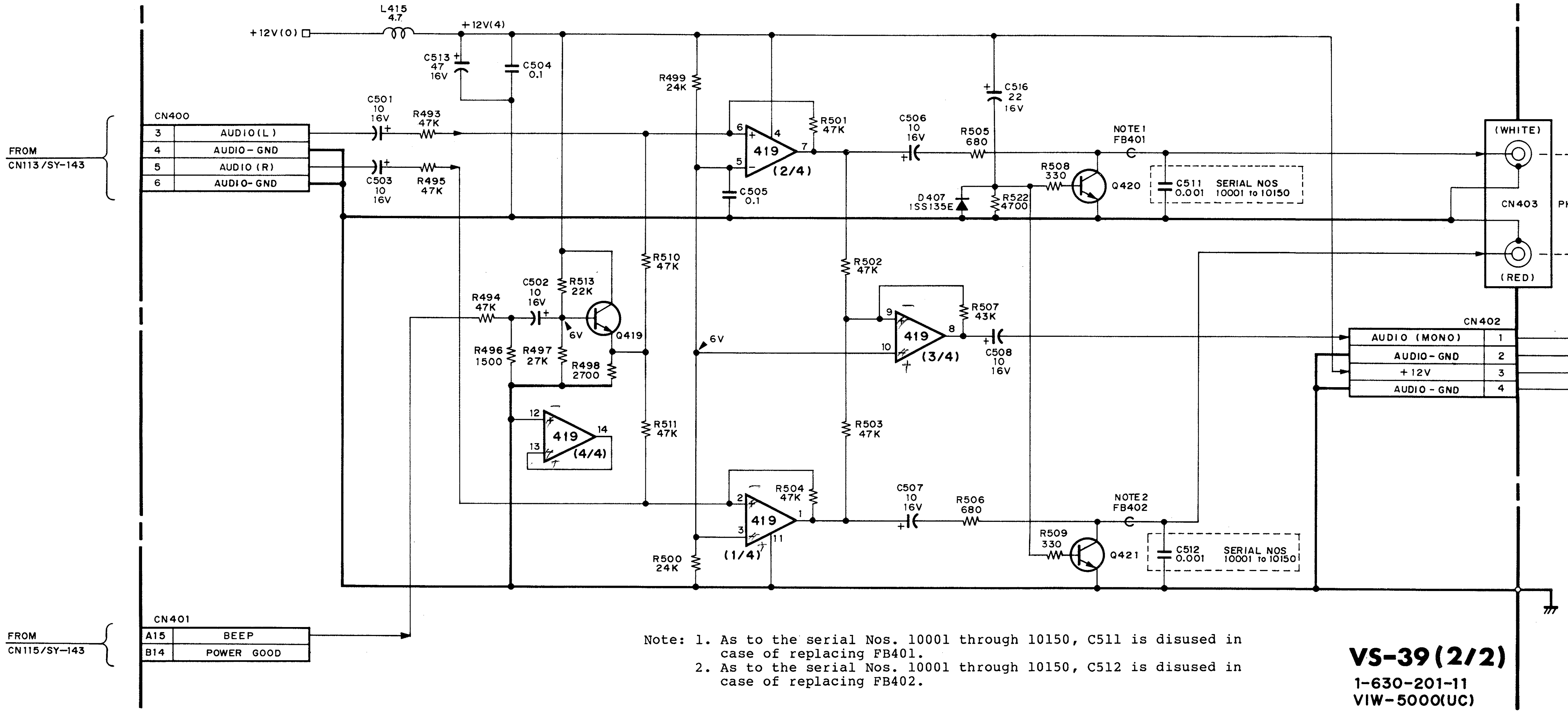

SP-7
SONY
MADE IN JAPAN
RV601
FB601
J601
IC601
CN601
A-1
1-630-293-11

SP-7 – COMPONENT SIDE –

1-630-293-11
VIW-5000(UC)

Ref. No.	TYPE	PIN No. +12V(4)	PIN No. GND
IC419	TL084CNS	4	11

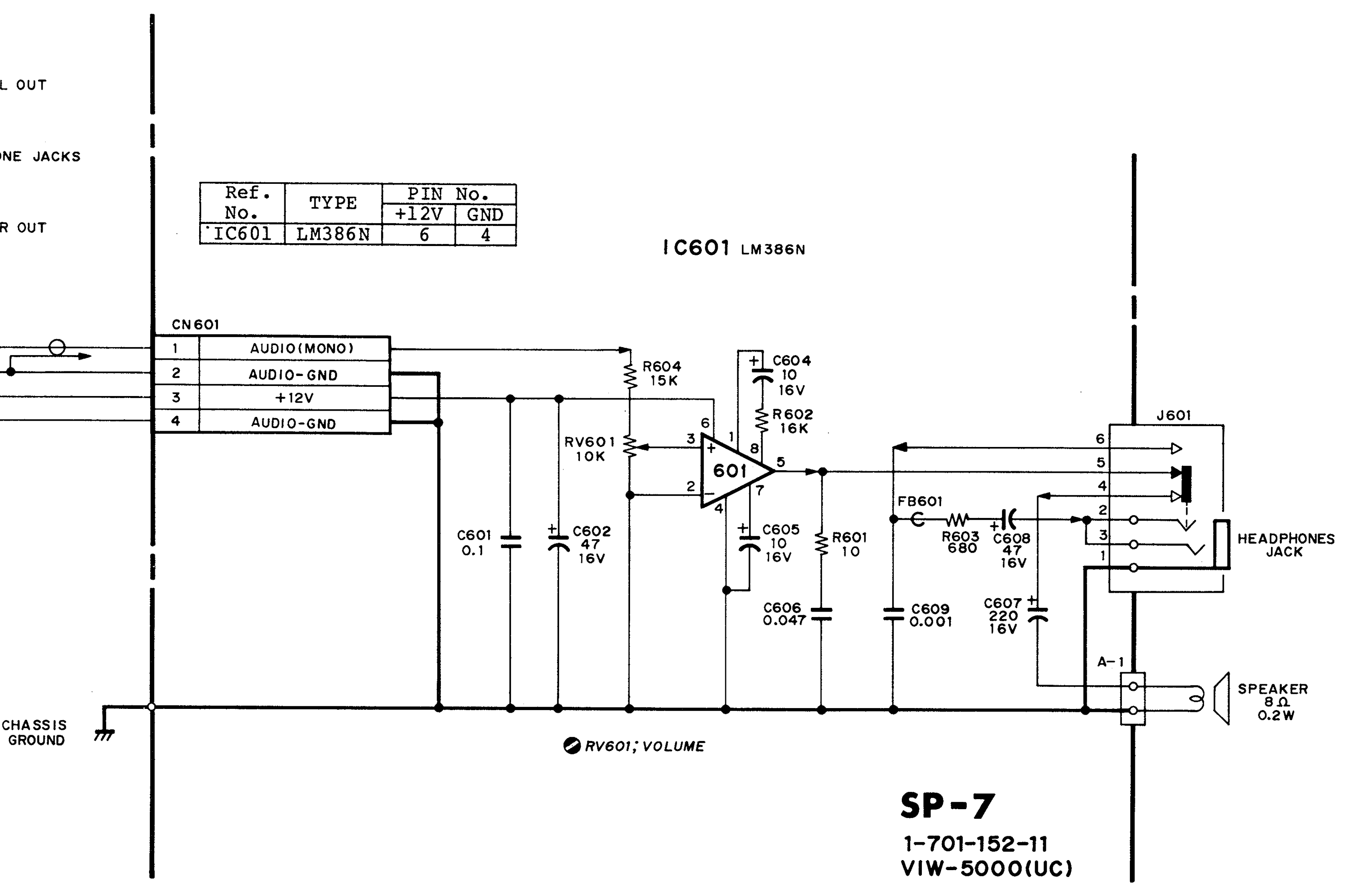
+12V(4); THROUGH L415


Q419 2SC1623
IC419 TL084CNS
Q420,421 2SC1623
+12V(0)
L415 4.7
+12V(4)
C513 47 16V
C504 0.1
R499 24K
C516 22 16V
CN400
FROM CN113/SY-143
3 AUDIO(L)
4 AUDIO-GND
5 AUDIO(R)
6 AUDIO-GND
C501 10 16V
R493 47K
C503 10 16V
R495 47K
419 (2/4)
R501 47K
C505 0.1
C506 10 16V
R505 680
NOTE 1 FB401
R508 330
Q420
D407 1SS135E
R522 4700
C511 0.001 SERIAL NOS 10001 to 10150
(WHITE)
L OUT
CN403 PHONE JACKS
R OUT
(RED)
R510 47K
R502 47K
C502 10 16V
R513 22K
R494 47K
Q419
6V
R496 1500
R497 27K
R498 2700
419 (3/4)
R507 43K
C508 10 16V
419 (4/4)
R511 47K
R503 47K
R504 47K
419 (1/4)
R500 24K
C507 10 16V
R506 680
NOTE 2 FB402
R509 330
Q421
C512 0.001 SERIAL NOS 10001 to 10150
CN402
AUDIO (MONO) 1
AUDIO-GND 2
+12V 3
AUDIO-GND 4
CHASSIS GROUND
CN401
FROM CN115/SY-143
A15 BEEP
B14 POWER GOOD

Note: 1. As to the serial Nos. 10001 through 10150, C511 is disused in case of replacing FB401.
2. As to the serial Nos. 10001 through 10150, C512 is disused in case of replacing FB402.

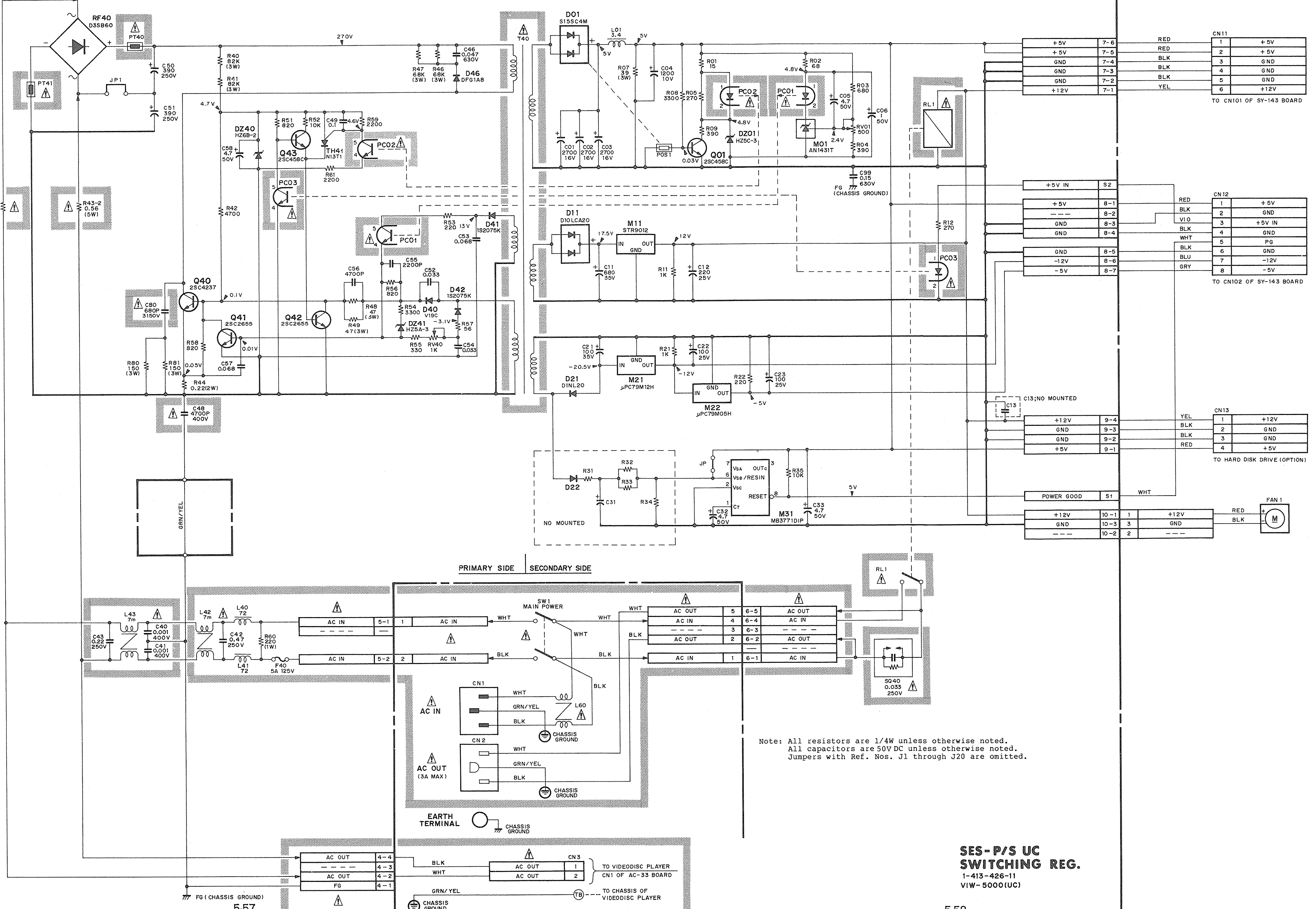
VS-39(2/2)
1-630-201-11
VIW-5000(UC)

Ref. No.	TYPE	PIN No. +12V	PIN No. GND
IC601	LM386N	6	4


IC601 LM386N
CN601
1 AUDIO(MONO)
2 AUDIO-GND
3 +12V
4 AUDIO-GND
R604 15K
C604 10 16V
R602 16K
RV601 10K
601
C601 0.1
C602 47 16V
C605 10 16V
R601 10
C606 0.047
FB601
R603 680
C608 47 16V
C609 0.001
C607 220 16V
J601
HEADPHONES JACK
A-1
SPEAKER 8Ω 0.2W
RV601; VOLUME

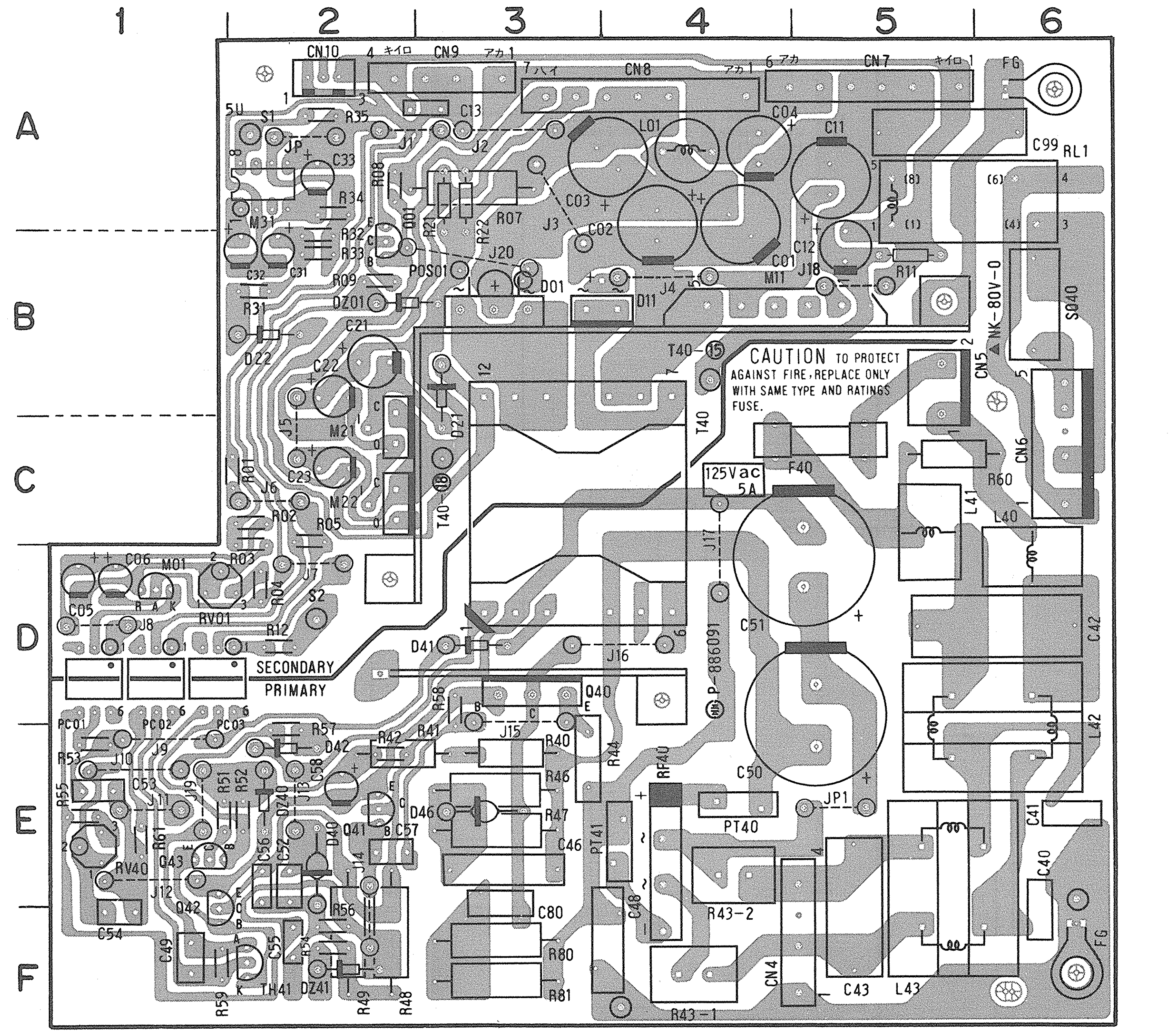
SP-7
1-701-152-11
VIW-5000(UC)

5-7. SWITCHING REGULATOR


RF40 D3SB60
PT40
PT41
JP1
C50 390 250V
C51 390 250V
270V
R40 82K (3W)
R41 82K (3W)
R47 68K (3W)
R46 68K (3W)
C46 0.047 630V
D46 DFG1A8
4.7V
DZ40 HZ6B-2
C58 4.7 50V
R51 820
R52 10K
C49 0.1
R59 2200
Q43 2SC458C
TH41 N13T1
PC02
R61 2200
PC03
R42 4700
PC01
R53 220
D41 1S2075K
C53 0.068
C55 2200P
C56 4700P
C52 0.033
R56 820
R54 3300
D40 V19C
D42 1S2075K
R48 47 (3W)
R49 47(3W)
DZ41 HZ5A-3
R55 330
RV40 1K
R57 56
C54 0.033
Q40 2SC4237
Q41 2SC2655
Q42 2SC2655
C80 680P 3150V
R58 820
C57 0.068
R80 150 (3W)
R81 150 (3W)
R44 0.22(2W)
C48 4700P 400V
R43-1 0.56 (5W)
R43-2 0.56 (5W)
GRN/YEL
D01 S15SC4M
L01 3.4
5V
R07 39 (3W)
C04 1200 10V
C01 2700 16V
C02 2700 16V
C03 2700 16V
R08 3300
R05 270
R01 15
R09 390
Q01 2SC458C
POS1
PC02
PC01
DZ01 HZ5C-3
R02 68
4.8V
M01 AN1431T
C05 4.7 50V
R03 680
RV01 500
R04 390
C06 1 50V
C99 0.15 630V
FG (CHASSIS GROUND)
D11 D10LCA20
17.5V
M11 STR9012
C11 680 35V
R11 1K
C12 220 25V
12V
C21 100 35V
-20.5V
M21 µPC79M12H
R21 1K
C22 100 25V
-12V
R22 220
C23 100 25V
D21 D1NL20
M22 µPC79M05H
-5V
RL1
R12 270
PC03
C13;NO MOUNTED
C13
D22
R31
R32
R33
R34
C31
NO MOUNTED
JP
M31 MB3771DIP
R35 10K
C32 4.7 50V
C33 4.7 50V
VSA OUTc VSB/RESIN VSC RESET CT
+5V 7-6
+5V 7-5
GND 7-4
GND 7-3
GND 7-2
+12V 7-1
RED
RED
BLK
BLK
BLK
YEL
CN11
1 +5V
2 +5V
3 GND
4 GND
5 GND
6 +12V
TO CN101 OF SY-143 BOARD
+5V IN S2
+5V 8-1
--- 8-2
GND 8-3
GND 8-4
GND 8-5
-12V 8-6
-5V 8-7
RED
BLK
VIO
BLK
WHT
BLK
BLU
GRY
CN12
1 +5V
2 GND
3 +5V IN
4 GND
5 PG
6 GND
7 -12V
8 -5V
TO CN102 OF SY-143 BOARD
+12V 9-4
GND 9-3
GND 9-2
+5V 9-1
YEL
BLK
BLK
RED
CN13
1 +12V
2 GND
3 GND
4 +5V
TO HARD DISK DRIVE (OPTION)
POWER GOOD S1
WHT
+12V 10-1 1 +12V
GND 10-3 3 GND
--- 10-2 2 ---
RED
BLK
FAN 1
M
PRIMARY SIDE
SECONDARY SIDE
L43 7m
C43 0.22 250V
C40 0.001 400V
C41 0.001 400V
L42 7m
L40 72
C42 0.47 250V
R60 220 (1W)
L41 72
F40 5A 125V
AC IN 5-1
AC IN 5-2
AC IN
SW1 MAIN POWER
WHT
BLK
AC OUT 5 6-5 AC OUT
AC IN 4 6-4 AC IN
3 6-3
AC OUT 2 6-2 AC OUT
AC IN 1 6-1 AC IN
RL1
SQ40 0.033 250V
CN1
AC IN
WHT
GRN/YEL
BLK
L60
CHASSIS GROUND
CN2
AC OUT (3A MAX)
EARTH TERMINAL
CHASSIS GROUND
AC OUT 4-4
4-3
AC OUT 4-2
FG 4-1
BLK
WHT
GRN/YEL
AC OUT 1
AC OUT 2
CN3
TO VIDEODISC PLAYER CN1 OF AC-33 BOARD
TB
TO CHASSIS OF VIDEODISC PLAYER
CHASSIS GROUND
FG (CHASSIS GROUND)

Note: All resistors are 1/4W unless otherwise noted.
All capacitors are 50V DC unless otherwise noted.
Jumpers with Ref. Nos. J1 through J20 are omitted.

SES-P/S UC
SWITCHING REG.
1-413-426-11
VIW-5000(UC)


1
2
3
4
5
6
A
B
C
D
E
F
CN10
CN9
CN8
CN7
CN4
CN5
CN6
CAUTION TO PROTECT AGAINST FIRE, REPLACE ONLY WITH SAME TYPE AND RATINGS FUSE.
125Vac 5A
F40
SECONDARY
PRIMARY
P-886091
T40
SQ40
RL1
FG
C99
JP1
PT40
PT41
RF40
C50
C51
C42
C41
C40
L40
L41
L42
L43
C43
R43-1
R43-2
C80
R80
R81
M11
M21
M22
M31
M01
D01
D11
D21
D22
D40
D41
D46
Q40
Q41
Q42
Q43
PC01
PC02
PC03
TH41
DZ41
RV01
RV40
POS01
S1
S2

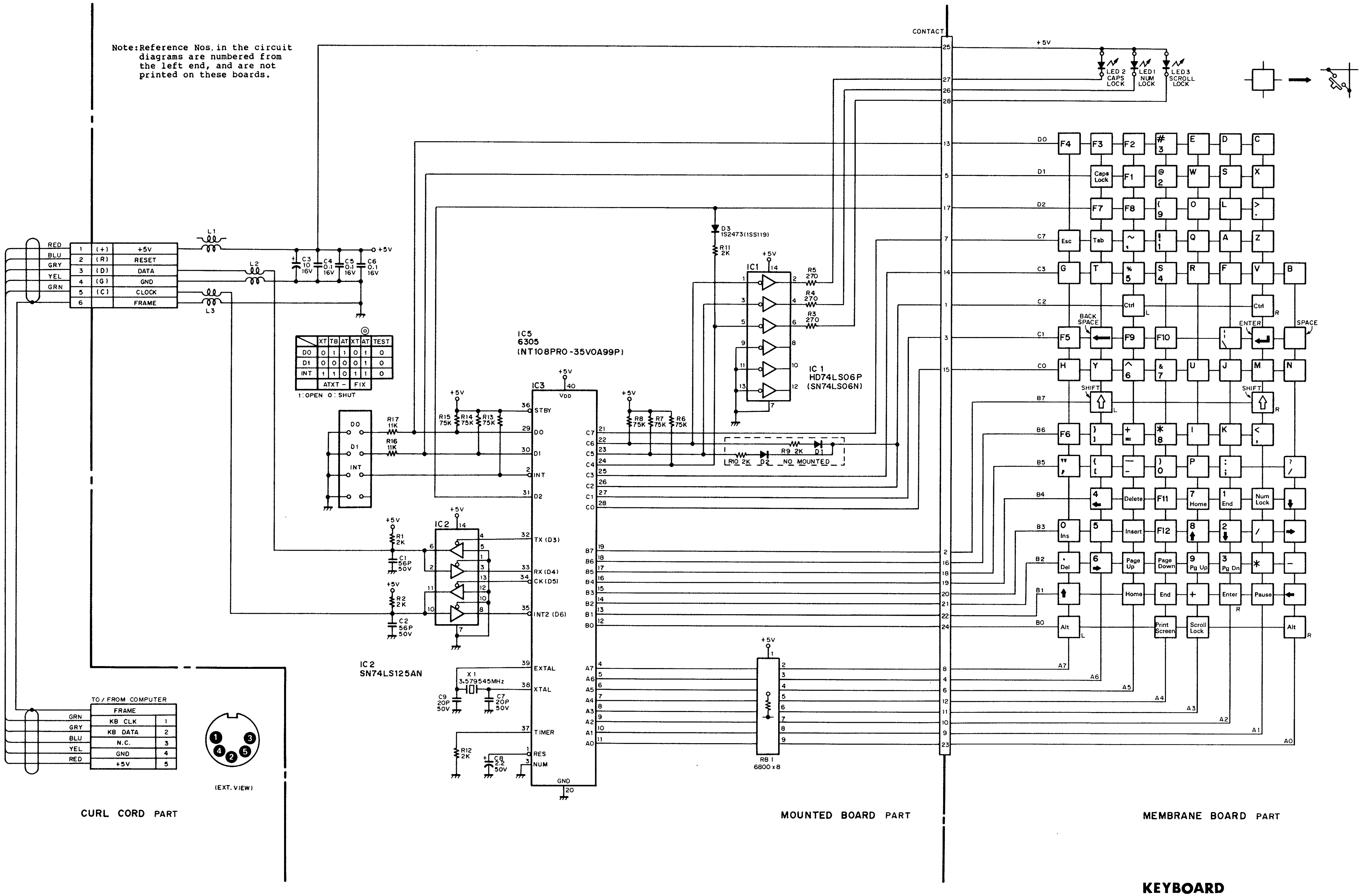
P-886091-5 –COMPONENT SIDE–

VIW-5000(UC)

C01	B-4
C02	A-4
C03	A-3
C04	A-4
C05	D-1
C06	D-1
C11	A-5
C12	B-5
C13	A-3
C21	B-2
C22	B-2
C23	C-2
C31	B-2
C32	B-2
C33	A-2
C40	E-6
C41	E-6
C42	D-6
C43	F-5
C46	E-3
C48	F-4
C49	F-1
C50	E-4
C51	D-4
C52	E-2
C53	E-1
C54	F-1
C55	F-2
C56	E-2
C57	E-2
C58	E-2
C80	F-3
C99	A-6
CN4	F-4
CN5	B-6
CN6	C-6
CN7	A-5
CN8	A-4
CN9	A-3
CN10	A-2
D01	B-3
D11	B-4
D21	C-3
D22	B-2
D40	E-2
D41	D-3
D42	E-2
D46	E-3
F40	C-5
J1	A-2
J2	A-3
J3	A-3
J4	B-4
J5	C-2
J6	C-2
J7	D-2
J8	D-1
J9	E-1
J10	E-1
J11	E-1
J12	E-1
J13	E-2
J14	E-2
J15	E-3
J16	D-4
J17	D-4
J18	B-5
J19	E-1
J20	B-3
JP	A-2
JP1	E-5
L01	A-4
L40	C-6
L41	C-5
L42	E-6
L43	F-5
M01	D-1
M11	B-4
M21	C-2
M22	C-2
M31	A-2
PC01	D-1
PC02	D-1
PC03	D-1
POS01	B-3
PT40	E-4
PT41	E-4
Q01	A-2
Q40	D-3
Q41	E-2
Q42	F-1
Q43	E-1
R01	C-2
R02	C-2
R03	D-2
R04	D-2
R05	C-2
R07	A-3
R08	A-2
R09	B-2
R11	B-5
R12	D-2
R21	A-3
R22	A-3
R31	B-2
R32	B-2
R33	B-2
R34	A-2
R35	A-2
R40	E-3
R41	E-3
R42	E-2
R43-1	F-4
R43-2	F-4
R44	E-4
R46	E-3
R47	E-3
R48	F-2
R49	F-2
R51	E-1
R52	E-2
R53	E-1
R54	F-2
R55	E-1
R56	F-2
R57	E-2
R58	D-3
R59	F-1
R60	C-6
R61	E-1
R80	F-3
R81	F-3
RF40	E-4
RL1	A-6
RV01	D-1
RV40	E-1
S1	A-2
S2	D-2
SQ40	B-6
T40	C-4
TH41	F-2

5-8. KEYBOARD

Note: Reference Nos. in the circuit diagrams are numbered from the left end, and are not printed on these boards.


RED
BLU
GRY
YEL
GRN
1 (+) +5V
2 (R) RESET
3 (D) DATA
4 (G) GND
5 (C) CLOCK
6 FRAME
L1
L2
L3
C3 10 16V
C4 0.1 16V
C5 0.1 16V
C6 0.1 16V
+5V
IC5
6305
(NT108PRO-35V0A99P)
IC3
VDD
STBY
D0
D1
INT
D2
TX (D3)
RX (D4)
CK (D5)
INT2 (D6)
EXTAL
XTAL
TIMER
RES
NUM
GND
C7 C6 C5 C4 C3 C2 C1 C0
B7 B6 B5 B4 B3 B2 B1 B0
A7 A6 A5 A4 A3 A2 A1 A0
R17 11K
R16 11K
R15 75K
R14 75K
R13 75K
R8 75K
R7 75K
R6 75K
IC2
SN74LS125AN
R1 2K
C1 56P 50V
R2 2K
C2 56P 50V
X1 3.579545MHz
C9 20P 50V
C7 20P 50V
R12 2K
C8 2.2 50V
D3 1S2473(1SS119)
R11 2K
IC1
HD74LS06P
(SN74LS06N)
R5 270
R4 270
R3 270
R10 2K
D2
R9 2K
D1
NO MOUNTED
RB1 6800 x 8
CONTACT
LED 2 CAPS LOCK
LED1 NUM LOCK
LED3 SCROLL LOCK
TO / FROM COMPUTER
GRN FRAME
GRY KB CLK 1
BLU KB DATA 2
YEL N.C. 3
RED GND 4
+5V 5
(EXT. VIEW)
CURL CORD PART
MOUNTED BOARD PART
MEMBRANE BOARD PART
F4 F3 F2 # 3 E D C
Caps Lock F1 @ 2 W S X
F7 F8 (9 O L >
Esc Tab ~ ! 1 Q A Z
G T % 5 $ 4 R F V B
Ctrl L Ctrl R
BACK SPACE
F5 F9 F10 ENTER SPACE
H Y ^ 6 & 7 U J M N
SHIFT L SHIFT R
F6 }] + = * 8 I K < ,
" ' { [— -) 0 P : ; ? /
4 Delete F11 7 Home 1 End Num Lock
0 Ins 5 Insert F12 8 2
. Del 6 Page Up Page Down 9 Pg Up 3 Pg Dn *
Home End + Enter R Pause
Alt L Print Screen Scroll Lock Alt R

	XT	TB	AT	XT	AT	TEST
D0	0	1	1	0	1	0
D1	0	0	0	0	1	0
INT	1	1	0	1	1	0
	ATXT –		FIX			

1 : OPEN 0 : SHUT

KEYBOARD
1-466-050-11, 21
VIW-3015A (UC)
VIW-5000 (UC)

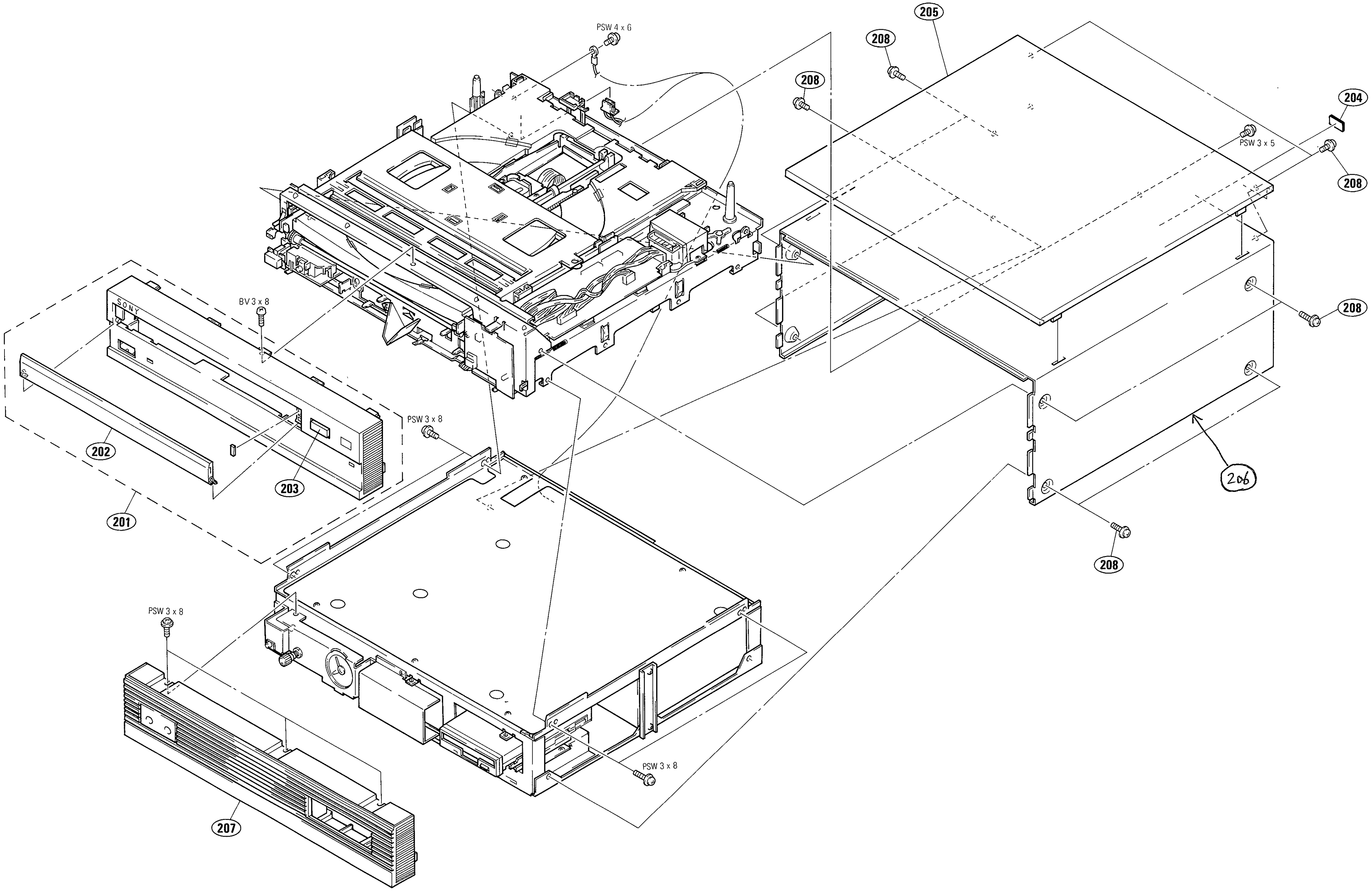
CHAPTER 9
REPAIR PARTS AND FIXTURES

- Refer to the service manual (9-975-189-XX) of MP-F17W for the micro floppydisk drive unit of VIW-5000.
- Refer to the service manual (9-972-629-XX) of LDP-1200 for the videodisc player prat of VIW-5000.

9-1. MECHANICAL PARTS LIST

9-1-1. Cover Block

No.	Parts No.	Description
201	A-6408-149-A	PANEL ASSY, FRONT (including No. 202 and No. 203)
202	X-3688-256-1	DOOR ASSY, FRONT
203	3-715-924-31	BUTTON, EJECT
204	*4-615-804-01	SEAL, BAUD RATE
205	4-615-814-01	TABLE, MONITOR
206	4-615-817-01	CASE, UPPER
207	4-615-823-01	PANEL, FRONT
208	4-820-330-21	SCREW, CASE

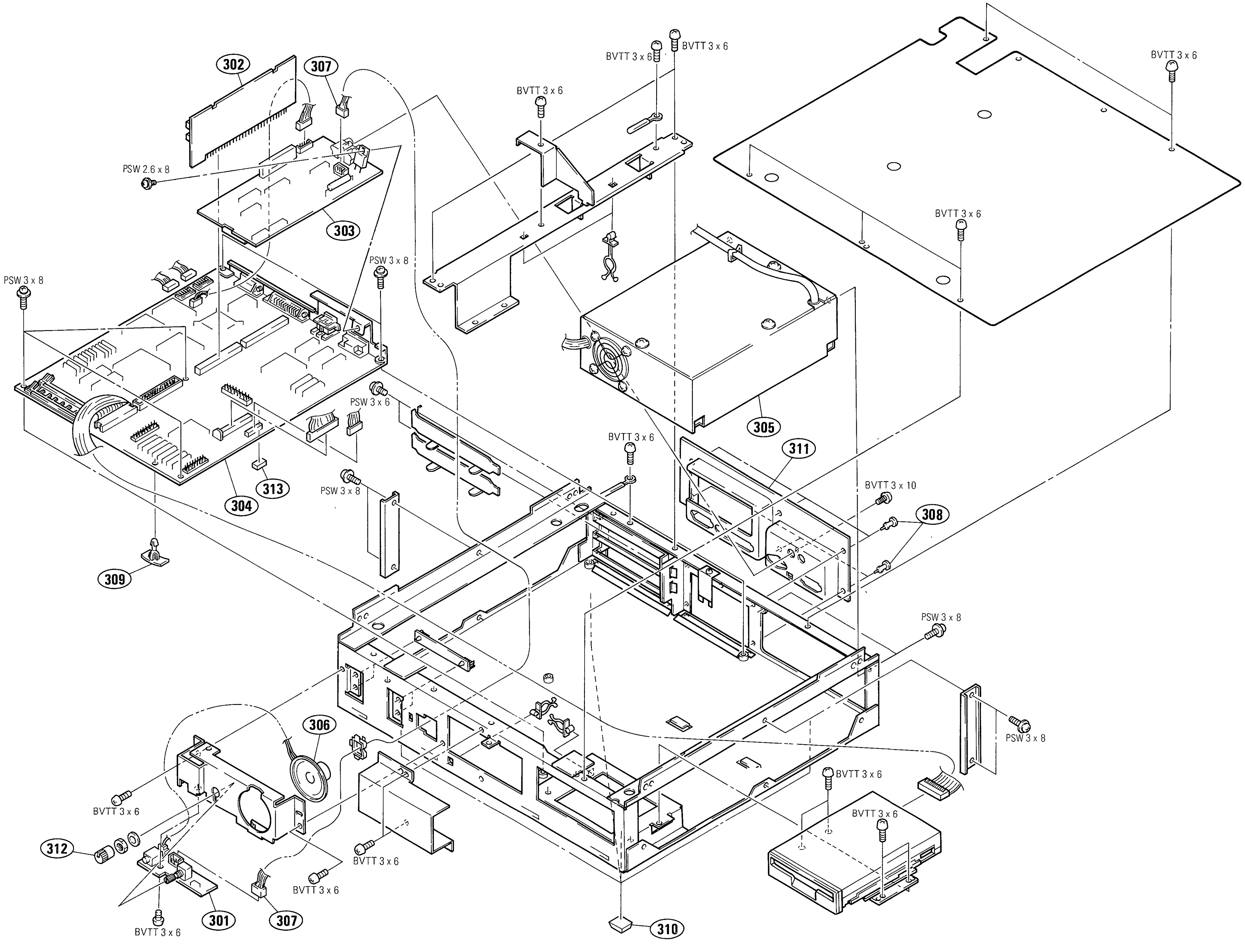


NOTE:

1. **The shaded and ⚠ -marked components are critical to safety. Replace only with same components as specified.**
2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
3. Item with no part number and/or description are not stocked because they are seldom required for routine service.

9-1-2. Computer Chassis Block

No.	Parts No.	Description
301	*A-8051-508-A	MOUNTED C B, SP-7
302	*A-8051-509-A	MOUNTED C B, MB-232
⚠ 303	*A-8051-510-A	MOUNTED C B, VS-39
304	*A-8051-511-B	MOUNTED C B, SY-143 (including No. 309, No. 313 and DUS-307 board)
⚠ 305	*1-413-426-11	REGULATOR, SWITCHING (SES-P/S UC)
306	1-503-637-11	SPEAKER
307	*1-943-606-11	HARNESS (VS-SP)
308	3-531-576-11	RIVET, NYLON
309	*3-704-198-21	SUPPORT, PC
310	4-611-214-01	FOOT, RUBBER
311	4-615-816-01	PANEL, REAR
312	4-902-067-41	KNOB, CONTROL
313	*9-911-841-99	CUSHION


302
307
PSW 2.6 x 8
303
PSW 3 x 8
PSW 3 x 8
BVTT 3 x 6
BVTT 3 x 6
BVTT 3 x 6
BVTT 3 x 6
BVTT 3 x 6
304
313
PSW 3 x 6
PSW 3 x 8
309
305
311
BVTT 3 x 6
BVTT 3 x 10
308
PSW 3 x 8
PSW 3 x 8
306
BVTT 3 x 6
BVTT 3 x 6
312
BVTT 3 x 6
BVTT 3 x 6
BVTT 3 x 6
301
307
BVTT 3 x 6
BVTT 3 x 6
310

NOTE:

1. **The shaded and ⚠ -marked components are critical to safety. Replace only with same components as specified.**
2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
3. Item with no part number and/or description are not stocked because they are seldom required for routine service.

9-1-3. Keyboard Block

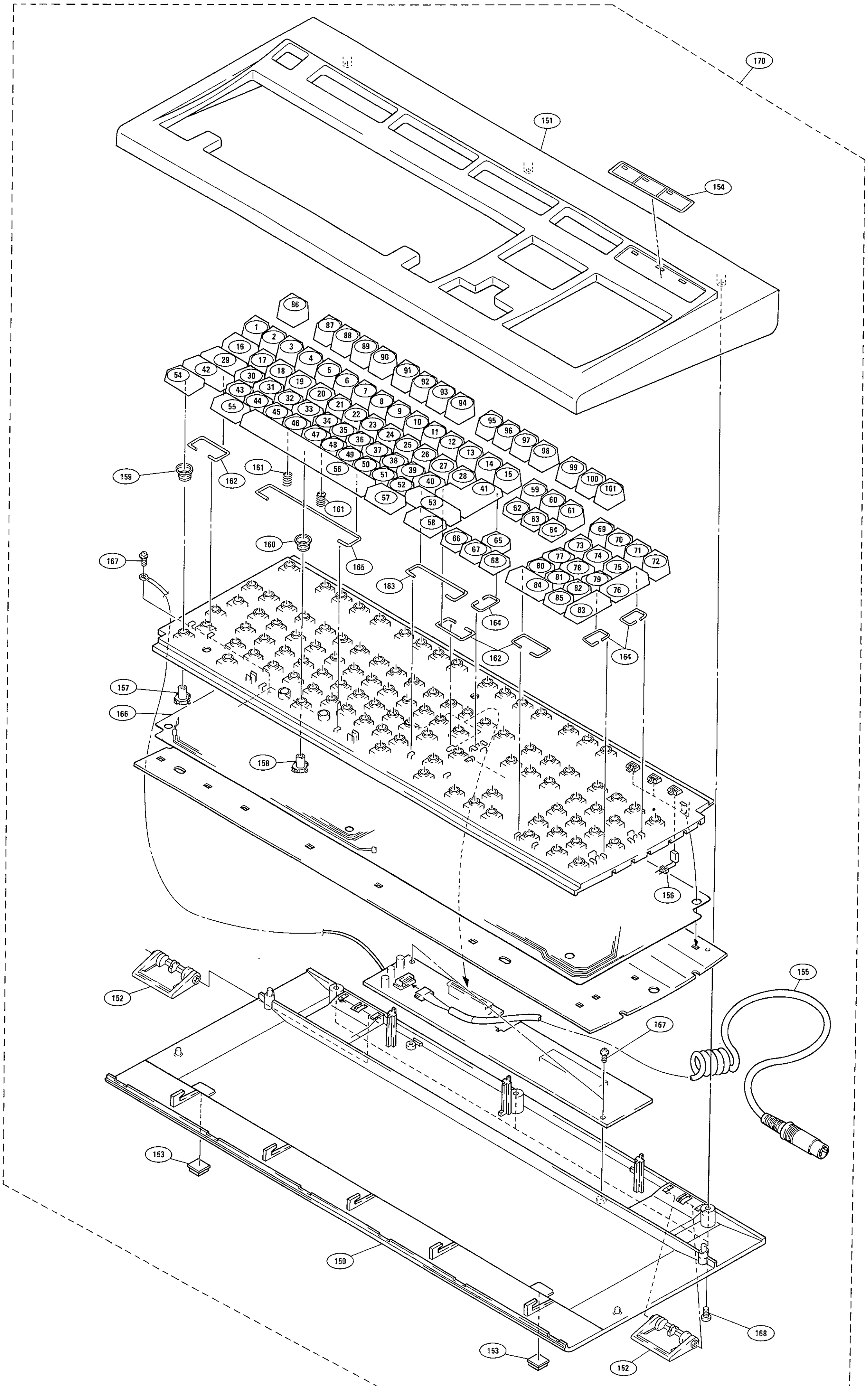
No.	Parts No.	Description
1	3-707-696-14	KEYTOP (C4C100) ' (SINGLE QUOTES)
2	3-707-696-15	KEYTOP (C4C100) 1
3	3-707-696-16	KEYTOP (C4C100) 2
4	3-707-696-17	KEYTOP (C4C100) 3
5	3-707-696-18	KEYTOP (C4C100) 4
6	3-707-696-19	KEYTOP (C4C100) 5
7	3-707-696-20	KEYTOP (C4C100) 6
8	3-707-696-21	KEYTOP (C4C100) 7
9	3-707-696-22	KEYTOP (C4C100) 8
10	3-707-696-23	KEYTOP (C4C100) 9
11	3-707-696-24	KEYTOP (C4C100) 0
12	3-707-696-25	KEYTOP (C4C100) -
13	3-707-696-26	KEYTOP (C4C100) =
14	3-707-696-27	KEYTOP (C4C100) \(BACK SLASH)
15	3-707-696-28	KEYTOP (C4C100) ←(BACK SPACE)
16	3-707-675-01	KEYTOP (C4C150) Tab
17	3-707-696-36	KEYTOP (C4C100) Q
18	3-707-696-37	KEYTOP (C4C100) W
19	3-707-696-38	KEYTOP (C4C100) E
20	3-707-696-39	KEYTOP (C4C100) R
21	3-707-696-40	KEYTOP (C4C100) T
22	3-707-696-41	KEYTOP (C4C100) Y
23	3-707-696-42	KEYTOP (C4C100) U
34	3-707-696-43	KEYTOP (C4C100) I
25	3-707-696-44	KEYTOP (C4C100) O
26	3-707-696-45	KEYTOP (C4C100) P
27	3-707-696-46	KEYTOP (C4C100) [
28	3-707-696-47	KEYTOP (C4C100)]
29	3-707-678-01	KEYTOP (C4CJ175) Caps Lock
30	3-707-696-54	KEYTOP (C4C100) A
31	3-707-696-55	KEYTOP (C4C100) S
32	3-707-696-56	KEYTOP (C4C100) D
33	3-707-674-01	KEYTOP (C4CH100) F
34	3-707-696-57	KEYTOP (C4C100) G
35	3-707-696-58	KEYTOP (C4C100) H
36	3-707-674-11	KEYTOP (C4CH100) J
37	3-707-696-59	KEYTOP (C4C100) K
38	3-707-696-60	KEYTOP (C4C100) L
39	3-707-696-61	KEYTOP (C4C100) ; (SEMICOLON)
40	3-707-696-62	KEYTOP (C4C100) ' (APOSTROPHE)
41	3-707-680-01	KEYTOP (C4CCG225) Enter
42	3-707-677-01	KEYTOP (C4C225) Shift
43	3-707-696-65	KEYTOP (C4C100) Z
44	3-707-696-66	KEYTOP (C4C100) X
45	3-707-696-67	KEYTOP (C4C100) C
46	3-707-696-68	KEYTOP (C4C100) V
47	3-707-696-69	KEYTOP (C4C100) B
48	3-707-696-70	KEYTOP (C4C100) N
49	3-707-696-71	KEYTOP (C4C100) M
50	3-707-696-72	KEYTOP (C4C100) , (COMMA)
51	3-707-696-73	KEYTOP (C4C100) .
52	3-707-696-74	KEYTOP (C4C100) /
53	3-707-681-01	KEYTOP (C4C275) Shift
54	3-707-675-11	KEYTOP (C4C150) Ctrl
55	3-707-675-21	KEYTOP (C4C150) Alt
56	3-707-682-01	KEYTOP (C5CMG700A) (SPACE)
57	3-707-675-21	KEYTOP (C4C150) Alt
58	3-707-675-11	KEYTOP (C4C150) Ctrl
59	3-707-696-29	KEYTOP (C4C100) Insert
60	3-707-696-30	KEYTOP (C4C100) Home
61	3-707-696-31	KEYTOP (C4C100) Page Up
62	3-707-696-48	KEYTOP (C4C100) Delete
63	3-707-696-49	KEYTOP (C4C100) End
64	3-707-696-50	KEYTOP (C4C100) Page Down
65	3-707-696-75	KEYTOP (C4C100) ↑ (CURSOR UP)
66	3-707-696-79	KEYTOP (C4C100) ←(CURSOR LEFT)
67	3-707-696-80	KEYTOP (C4C100) ↓ (CURSOR DOWN)
68	3-707-696-81	KEYTOP (C4C100) →(CURSOR RIGHT)
69	3-707-696-32	KEYTOP (C4C100) Num Lock
70	3-707-696-33	KEYTOP (C4C100) /
71	3-707-696-34	KEYTOP (C4C100) * (ASTRISK)
72	3-707-696-35	KEYTOP (C4C100) -
73	3-707-696-51	KEYTOP (C4C100) 7
74	3-707-696-52	KEYTOP (C4C100) 8
75	3-707-696-53	KEYTOP (C4C100) 9
76	3-707-679-01	KEYTOP (C4CCG100) +
77	3-707-696-63	KEYTOP (C4C100) 4
78	3-707-674-21	KEYTOP (C4CH100) 5
79	3-707-696-64	KEYTOP (C4C100) 6
80	3-707-696-76	KEYTOP (C4C100) 1
81	3-707-696-77	KEYTOP (C4C100) 2
82	3-707-696-78	KEYTOP (C4C100) 3
83	3-707-679-11	KEYTOP (C4CCG100) Enter
84	3-707-676-01	KEYTOP (C4C200) 0
85	3-707-696-82	KEYTOP (C4C100) .
86	3-707-696-85	KEYTOP (C4C100) Esc
87	3-707-696-01	KEYTOP (C4C100) F1
88	3-707-696-02	KEYTOP (C4C100) F2
89	3-707-696-03	KEYTOP (C4C100) F3
90	3-707-696-04	KEYTOP (C4C100) F4
91	3-707-696-05	KEYTOP (C4C100) F5
92	3-707-696-06	KEYTOP (C4C100) F6
93	3-707-696-07	KEYTOP (C4C100) F7
94	3-707-696-08	KEYTOP (C4C100) F8
95	3-707-696-09	KEYTOP (C4C100) F9
96	3-707-696-10	KEYTOP (C4C100) F10
97	3-707-696-11	KEYTOP (C4C100) F11
98	3-707-696-12	KEYTOP (C4C100) F12
99	3-707-696-83	KEYTOP (C4C100) Print Screen
100	3-707-696-13	KEYTOP (C4C100) Scroll Lock
101	3-707-696-84	KEYTOP (C4C100) Pause

KEYBOARD BLOCK

No.	Parts No.	Description
150	3-707-683-01	CASE, LOWER
151	3-707-684-01	CASE, UPPER
152	3-707-685-01	STAND
153	3-707-686-01	FOOT, RUBER
154	3-707-687-01	LALEL, LED
155	1-575-029-21	COAD, CURL
156	3-707-697-01	LED-R BLOCK ASSY
157	3-707-688-01	CONTACT BLOCK ASSY
158	3-707-689-01	CONTACT BLOCK ASSY, for SPACE KEY
159	3-707-690-01	CLICK RUBER
160	3-707-691-01	CLICK RUBER, for SPACE KEY
161	3-707-692-01	SPRING, COIL
162	3-707-693-01	SHAFT, CLANK
163	3-707-693-11	SHAFT, CLANK
164	3-707-693-21	SHAFT, CLANK
165	3-707-693-31	SHAFT, CLANK
166	3-707-694-01	MEMBRANE BOARD
167	3-669-480-21	SCREW, +PTPWH 2x6
168	7-685-647-79	SCREW, +BVTP 3x10 TYPE2
170	*1-466-050-21	KEYBOARD ASSY

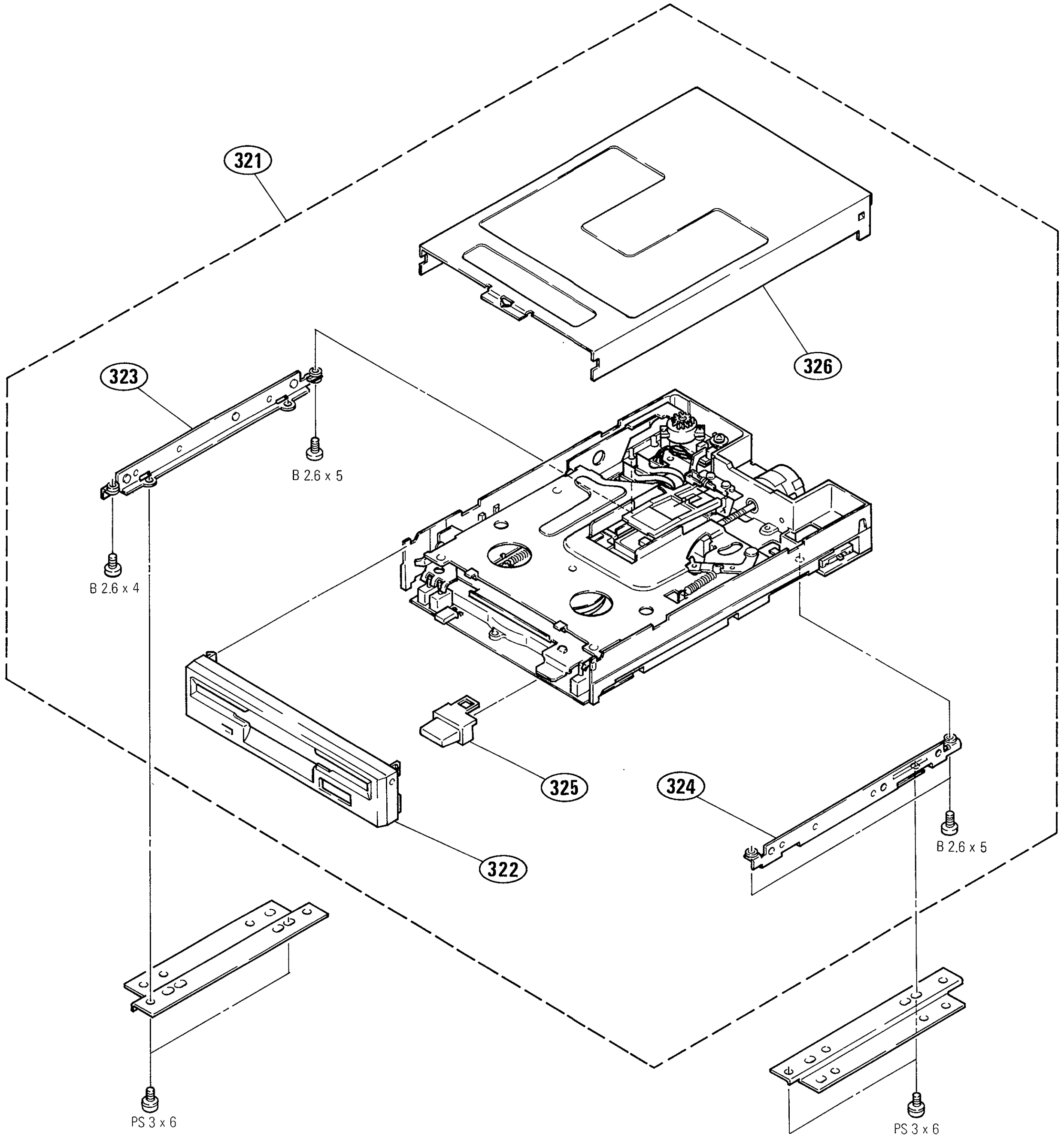
NOTE:

1. **The shaded and ⚠ -marked components are critical to safety. Replace only with same components as specified.**
2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
3. Item with no part number and/or description are not stocked because they are seldom required for routine service.



9-1-4. Micro Floppydisk Drive Block

No.	Parts No.	Description
321 ~~351~~	A-8041-277-A	MFD-17W-53E (SVA)
322 ~~352~~	A-8030-619-A	PANEL ASSY, FRONT
323 ~~353~~	*X-4613-106-1	BRACKET ASST, RIGHT
324 ~~354~~	*X-4613-118-1	BRACKET ASST, LEFT
325 ~~355~~	4-613-121-25	BUTTON, EJECT
326 ~~356~~	4-613-145-03	COVER



NOTE:

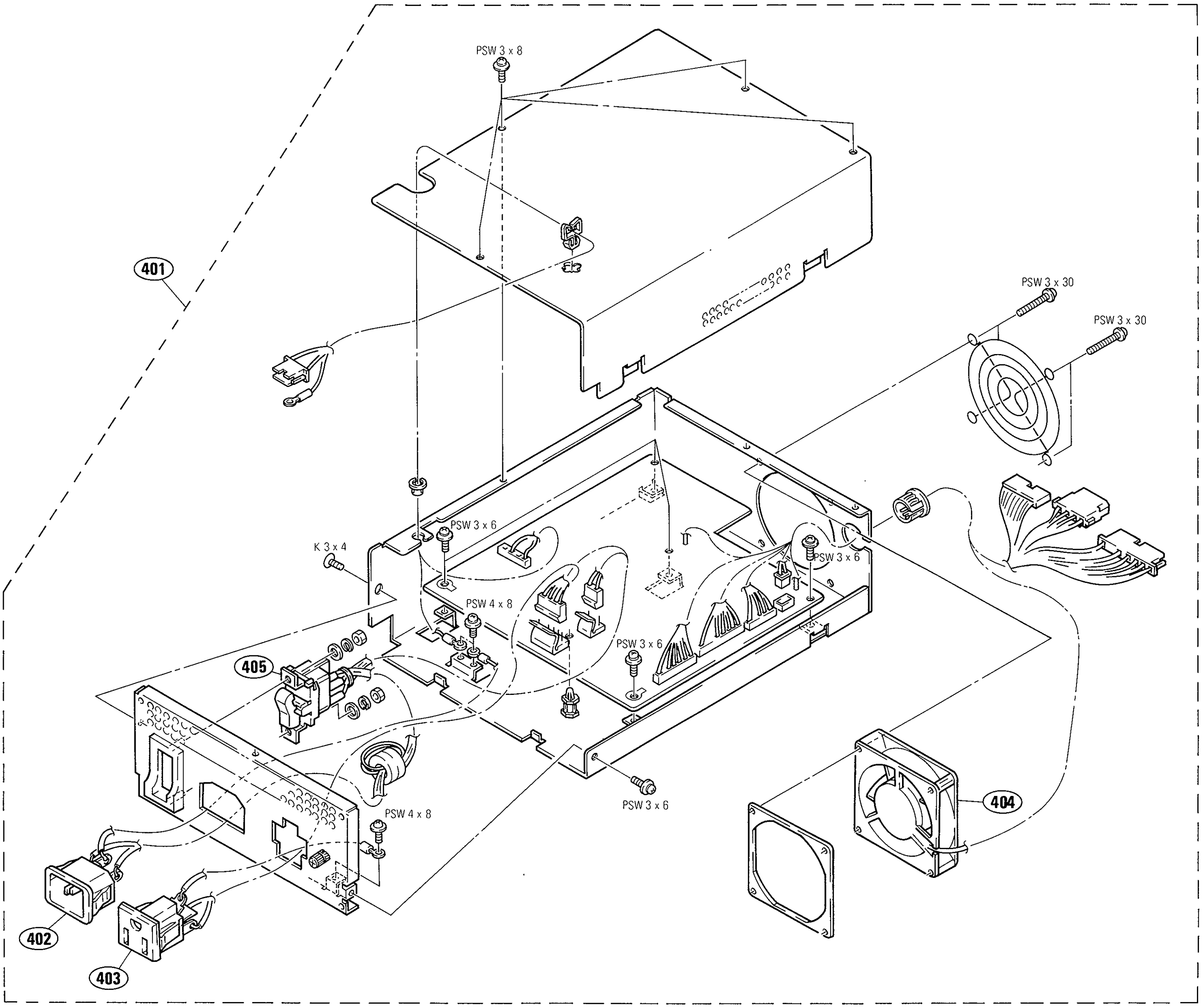
1. **The shaded and ⚠ -marked components are critical to safety. Replace only with same components as specified.**
2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
3. Item with no part number and/or description are not stocked because they are seldom required for routine service.

9-1-5. Switching Regulator Block

No.	Parts No.	Description
⚠ 401	*1-413-426-11	REGULATOR, SWITCHING (SES-P/S)
⚠ 402	1-540-088-11	INLET, AC (CN1)
⚠ 403	1-540-079-11	OUTLET, AC (CN2)
404	1-541-678-11	FAN (FAN1)
⚠ 405	1-571-947-11	POWER, SWITCH (SW1)

NOTE:

1. **The shaded and ⚠ -marked components are critical to safety. Replace only with same components as specified.**
2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
3. Item with no part number and/or description are not stocked because they are seldom required for routine service.


PSW 3 x 8
401
PSW 3 x 30
PSW 3 x 30
K 3 x 4
PSW 3 x 6
PSW 3 x 6
PSW 4 x 8
PSW 3 x 6
405
PSW 3 x 6
PSW 4 x 8
404
402
403

9-2. ELECTRICAL PARTS LIST OF COMPUTER PART

9-2-1. DUS-307 Board

Ref. No.	Parts No.	Description
	*1-631-737-12	PRINTED C B, DUS-307
IC001	8-759-993-12	74F373SJ

9-2-2. Keyboard

Ref. No.	Parts No.	Description
	1-101-884-00	CAP, CERAMIC 56pF 5% 50V
	1-102-985-00	CAP, CERAMIC 20pF 5% 50V
	1-123-356-00	CAP, ELECT 10 20% 16V
	1-123-381-00	CAP, ELECT 2.2 20% 50V
	1-162-851-11	CAP, CERAMIC 0.1 20% 16V
	1-235-335-11	RES, BLOCK 6.8K x 8
	1-247-138-00	RES, CARBON 2K 5% 1/4W
	1-247-156-00	RES, CARBON 11K 5% 1/4W
	1-247-176-00	RES, CARBON 75K 5% 1/4W
	1-247-705-11	RES, CARBON 270 5% 1/4W
	*1-564-521-11	PLUG, CONNECTOR 6P
	1-567-505-11	VIBRATOR, CRYSTAL
	1-568-890-11	PIN, CONNECTOR 28P
	1-575-029-21	CORD, CURL
	1-808-801-11	IC NT-108EX
	8-719-911-19	DIODE 1SS119
	8-759-901-25	IC SN74LS125AN
	8-759-914-03	IC SN74LS06N

9-2-3. MB-232 Board

Ref. No.	Parts No.	Description
	*A-8051-509-A	MOUNTED C B, MB-232
	8-719-903-27	DIODE 1SS168

9-2-4. SP-7 Board

Ref. No.	Parts No.	Description
	*A-8051-508-A	MOUNTED C B, SP-7
C601	1-161-458-00	CERAMIC 0.1 50V
C602	1-124-589-11	ELECT 47 20% 16V
C604	1-126-157-11	ELECT 10 20% 16V
C605	1-126-157-11	ELECT 10 20% 16V
C606	1-130-491-00	MYLAR 0.047 10% 50V
C607	1-124-120-11	ELECT 220 20% 16V
C608	1-124-589-11	ELECT 47 20% 16V
C609	1-102-074-00	CERAMIC 0.001 10% 50V
CN601	1-506-469-11	PIN, 4P
FB601	1-543-236-11	BEAD, FERRITE
IC601	8-759-903-86	LM386N
J601	1-507-995-11	JACK, MICROPHONE
R601	1-249-393-11	CARBON 10 5% 1/4W
R602	1-247-860-11	CARBON 16K 5% 1/4W
R603	1-249-415-11	CARBON 680 5% 1/4W
R604	1-249-431-11	CARBON 15K 5% 1/4W
RV601	1-237-790-21	VAR, CARBON 10K

NOTE:

1. **The shaded and ⚠-marked components are critical to safety.**
   Replace only with same components as specified.
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9-2-5. Switching Regulator

Ref. No.	Parts No.	Description
	1-533-221-11	CLIP, FUSE
C01-03	1-126-624-11	ELECT 2700 20% 16V
C04	1-126-623-11	ELECT 1200 20% 10V
C05	1-126-626-11	ELECT 4.7 20% 50V
C06	1-126-625-11	ELECT 1 20% 50V
C11	1-126-622-11	ELECT 680 20% 35V
C12	1-126-628-11	ELECT 220 20% 25V
C21	1-126-612-11	ELECT 100 20% 35V
C22, 23	1-126-627-11	ELECT 100 20% 25V
C32, 33	1-126-626-11	ELECT 4.7 20% 50V
⚠C40, 41	1-164-290-11	CERAMIC 0.001 10% 400V
⚠C42	1-136-537-11	FILM 0.47 20% 250V
⚠C43	1-130-711-00	FILM 0.22 20% 250V
C46	1-136-909-11	FILM 0.047 10% 630V
⚠C48	1-164-291-11	CERAMIC 0.0047 20% 400V
C49	1-136-915-11	MYLAR 0.1 10% 50V
C50, 51	1-125-567-11	ELECT 390 20% 250V
C52	1-136-913-11	MYLAR 0.033 10% 50V
C53	1-136-914-11	MYLAR 0.068 10% 50V
C54	1-136-913-11	MYLAR 0.033 10% 50V
C55	1-136-911-11	MYLAR 0.0022 10% 50V
C56	1-136-912-11	MYLAR 0.0047 10% 50V
C57	1-136-914-11	MYLAR 0.068 10% 50V
C58	1-126-626-11	ELECT 4.7 20% 50V
⚠C80	1-164-292-11	CERAMIC 680pF 10% 3150V
C99	1-136-910-11	FILM 0.15 10% 630V
⚠CN1	1-540-088-11	INLET, AC
⚠CN2	1-540-079-11	OUTLET, AC

Ref. No.	Parts No.	Description
D01	8-719-510-24	S15SC4M
D11	8-719-510-25	D10LCA20
D21	8-719-510-26	D1NL20
D40	8-719-971-20	ERC38-06
D41, 42	8-719-912-20	1SS120
D46	8-719-510-23	DFG1A8
DZ01	8-719-109-86	DIODE, RD5.1ES-B3
DZ40	8-719-109-90	DIODE, RD5.6ES-B3
DZ41	8-719-109-81	DIODE, RD4.7ES-B2
⚠F40	1-532-747-11	GLASS TUBE 5A 125V
FAN1	1-541-678-11	FAN
L01	1-424-238-11	COIL, CHOCK 3.4
⚠L40, 41	1-424-239-11	COIL, CHOCK 72
⚠L42, 43	1-424-237-11	COIL, CHOCK 7m
⚠L60	1-543-637-11	CHOCK, DATA LINE
M01	8-759-420-19	IC, AN1431T
M11	8-749-990-12	IC, STR9012
M21	8-759-604-39	IC, M5F79M12
M22	8-759-604-41	IC, M5F79M05
M31	8-759-988-44	IC, MB3771DIP
⚠PC01-03	8-719-510-21	PHOTOCOUPLER, PC111S
POS1	1-808-738-11	THERMISTOR, POSITIVE

NOTE:

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Ref. No.	Parts No.	Description
⚠PT40, 41	1-808-737-11	THERMISTOR, POWER
Q01	8-729-922-82	2SC458C
Q40	8-729-922-81	2SC4237
Q41, 42	8-729-265-52	2SC2655
Q43	8-729-922-82	2SC458C
R01	1-247-690-11	CARBON 15 5% 1/4W
R02	1-247-698-11	CARBON 68 5% 1/4W
R03	1-247-711-11	CARBON 680 5% 1/4W
R04	1-247-707-11	CARBON 390 5% 1/4W
R05	1-247-705-11	CARBON 270 5% 1/4W
R07	1-216-472-00	METAL OXIDE 39 5% 3W
R08	1-247-719-11	CARBON 3.3K 5% 1/4W
R09	1-247-707-11	CARBON 390 5% 1/4W
R11	1-247-713-11	CARBON 1K 5% 1/4W
R12	1-247-705-11	CARBON 270 5% 1/4W
R21	1-247-713-11	CARBON 1K 5% 1/4W
R22	1-247-704-11	CARBON 220 5% 1/4W
R35	1-247-725-11	CARBON 10K 5% 1/4W
R40, 41	1-216-492-11	METAL OXIDE 82K 5% 3W
R42	1-247-721-11	CARBON 4.7K 5% 1/4W
⚠R43-1, 43-2	1-219-111-11	WIREWOUND 0.56 5W
R44	1-218-360-11	METAL PLATE 0.22 2W
R46, 47	1-215-928-11	METAL OXIDE 68K 5% 3W
R48, 49	1-215-909-11	METAL OXIDE 47 5% 3W
R51	1-247-712-11	CARBON 820 5% 1/4W
R52	1-247-725-11	CARBON 10K 5% 1/4W
R53	1-247-704-11	CARBON 220 5% 1/4W
R54	1-247-719-11	CARBON 3.3K 5% 1/4W
R55	1-247-706-11	CARBON 330 5% 1/4W
R56	1-247-712-11	CARBON 820 5% 1/4W
R57	1-247-697-11	CARBON 56 5% 1/4W
R58	1-247-712-11	CARBON 820 5% 1/4W
R59	1-247-717-11	CARBON 2.2K 5% 1/4W
⚠R60	1-259-886-11	CARBON 220K 5% 1W
R61	1-247-717-11	CARBON 2.2K 5% 1/4W
R80, 81	1-215-912-11	METAL OXIDE 150 5% 3W

Ref. No.	Parts No.	Description
RF40	8-719-510-22	DIODE, D3SB60
⚠RL1	1-515-739-11	RELAY, POWER
RV01	1-238-608-11	ADJ, CARBON 500
RV40	1-238-609-11	ADJ, CARBON 1K
⚠SQ40	1-136-908-11	SPARK KILLER 0.033μF 20% 250V
⚠SW1	1-571-947-11	SWITCH, POWER
⚠T40	1-449-684-11	TRANSFORMER, SWITCHING
TH41	8-729-101-31	TRANSISTOR, N13T1

NOTE:

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9-2-6. SY-143 Board

Ref. No.	Parts No.	Description
	*A-8051-511-B	MOUNTED C B, SY-143 (including DUS-307 board)
	*3-704-198-21	SUPPORT, PC
	*9-911-841-99	CUSHION
C101-129	1-163-038-00	CERAMIC CHIP 0.1 25V
C130	1-124-589-11	ELECT 47 20% 16V
C131	1-163-038-00	CERAMIC CHIP 0.1 25V
C132	1-124-589-11	ELECT 47 20% 16V
C133	1-163-038-00	CERAMIC CHIP 0.1 25V
C137	1-126-157-11	ELECT 10 20% 16V
C138	1-126-096-11	ELECT 10 20% 25V
C139	1-124-229-00	ELECT 33 20% 10V
C140	1-102-820-00	CERAMIC 330pF 5% 50V
C141	1-124-229-00	ELECT 33 20% 10V
C142	1-126-096-11	ELECT 10 20% 25V
C143	1-163-357-91	CERAMIC CHIP 15pF 5% 50V
C144	1-163-109-00	CERAMIC CHIP 47pF 5% 50V
C145, 146	1-163-038-00	CERAMIC CHIP 0.1 25V
C147	1-163-809-11	CERAMIC CHIP 0.047 10% 25V
C148-150	1-163-038-00	CERAMIC CHIP 0.1 25V
C151-158	1-163-161-11	CERAMIC CHIP 0.0022 50V
C159	1-163-038-00	CERAMIC CHIP 0.1 25V
C160	1-163-161-11	CERAMIC CHIP 0.0022 50V
C161, 162	1-163-038-00	CERAMIC CHIP 0.1 25V
C167, 168	1-163-038-00	CERAMIC CHIP 0.1 25V
C169	1-124-589-11	ELECT 47 20% 16V
C171-174	1-163-038-00	CERAMIC CHIP 0.1 25V
C175	1-124-229-00	ELECT 33 20% 10V
C177-181	1-163-038-00	CERAMIC CHIP 0.1 25V
C186	1-163-038-00	CERAMIC CHIP 0.1 25V
C201	1-163-109-00	CERAMIC CHIP 47pF 5% 50V
C202-206	1-163-141-00	CERAMIC CHIP 0.001 5% 50V
C208-219	1-163-141-00	CERAMIC CHIP 0.001 5% 50V
C220-222	1-101-880-00	CERAMIC 47pF 5% 50V
C224	1-161-039-00	CERAMIC 0.001 20% 25V
C227, 228	1-163-123-00	CERAMIC CHIP 180pF 5% 50V
C301-303	1-163-021-00	CERAMIC CHIP 0.01 10% 50V
C304	1-126-157-11	ELECT 10 20% 16V
C305-313	1-163-038-00	CERAMIC CHIP 0.1 25V
C314	1-126-157-11	ELECT 10 20% 16V
C315	1-124-438-00	ELECT 1 20% 50V
C316-318	1-163-038-00	CERAMIC CHIP 0.1 25V
C319	1-126-157-11	ELECT 10 20% 16V
C320	1-124-438-00	ELECT 1 20% 50V
C321-323	1-163-038-00	CERAMIC CHIP 0.1 25V
C324	1-126-157-11	ELECT 10 20% 16V
C325	1-124-438-00	ELECT 1 20% 50V
C326	1-163-038-00	CERAMIC CHIP 0.1 25V
C327, 328	1-126-157-11	ELECT 10 20% 16V
C329, 330	1-163-038-00	CERAMIC CHIP 0.1 25V
C332	1-136-173-00	FILM 0.47 5% 50V
C333	1-163-111-00	CERAMIC CHIP 56pF 5% 50V
C334	1-126-157-11	ELECT 10 20% 16V
C335	1-163-038-00	CERAMIC CHIP 0.1 25V
C336	1-136-173-00	METALIZED FILM 0.47 5% 50V
C337	1-126-157-11	ELECT 10 20% 16V
C338	1-163-038-00	CERAMIC CHIP 0.1 25V
C339	1-106-353-00	MYLAR 0.0027 5% 50V
C340	1-163-121-00	CERAMIC CHIP 150pF 5% 50V
C341, 342	1-163-135-00	CERAMIC CHIP 560pF 10% 50V
C343	1-126-157-11	ELECT 10 20% 16V
C344-358	1-163-038-00	CERAMIC CHIP 0.1 25V
C359	1-124-589-11	ELECT 47 20% 16V
C360, 361	1-163-038-00	CERAMIC CHIP 0.1 25V
C364, 368	1-163-038-00	CERAMIC CHIP 0.1 25V
C370	1-163-123-00	CERAMIC CHIP 180pF 5% 50V
C371-373	1-163-038-00	CERAMIC CHIP 0.1 25V
CN101	*1-564-423-11	HEADDER, SPRING (POWER) 6P
CN102	*1-506-737-11	HEADDER, SPRING 8P
CN103	1-574-746-11	WIRE ASSY, FLAT SLIT (34 CORE)
CN104	1-563-161-11	D-SUB (MOUNT TYPE) 25P
CN105	1-568-492-11	D-SUB (MOUNT TYPE) 9P
CN106	1-563-496-12	DIN 5P
CN108, 109	*1-568-592-11	SOCKET (DIP TYPE)
CN110	1-568-463-11	D-SUB (SOCKET) 15P
CN111	*1-565-709-11	HEADDER (STRAIGHT TYPE) 40P
CN112	*1-506-485-11	PIN, 6P
CN113	*1-943-604-11	HARNESS (SY-VS)
CN114	*1-506-487-11	PIN, 8P
CN115	*1-568-458-11	MALE 34P
CN116	1-540-075-11	SOCKET, IC (SIP MODULE) 30P
CN301	*1-568-464-11	PIN, 20P
CN302	*1-568-465-11	PIN, 22P

NOTE:

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Ref. No.	Parts No.	Description
D301-303	8-719-800-76	1SS226
D305, 306	8-713-300-88	1T33C-01
DL100	8-759-948-40	IC DS1000M-50
FB208-224	1-543-623-11	BEAD, FERRITE (CHIP)
IC100	8-759-973-94	N80286-10
IC101	8-759-989-01	74F08SJ
IC102	8-759-930-35	SN74LS125ANS
IC103	8-759-987-85	FE3001
IC104	8-759-930-35	SN74LS125ANS
IC105	8-759-948-01	74F04SJ
IC106	8-759-989-03	74F32SJ
IC107	8-759-987-87	FE3010B
IC108	8-759-930-40	SN74LS138NS
IC109	8-759-987-86	FE3021
IC110	8-759-987-74	Am29827ASC
IC111	8-759-987-92	SN74ALS10ANS
IC112	8-759-922-49	SN74LS74ANS
IC113	8-759-987-77	FE3031
IC114	8-759-744-52	27C512-SY143S3. 10E02
IC115	8-759-744-53	27C512-SY143S3. 10002
IC116-119	8-759-987-75	MB81C4256-10PSZ
IC120, 121	8-759-929-72	MB81256-10PSZ
IC122-125	8-759-944-61	MB81464-10PSZ
IC126, 127	8-759-929-72	MB81256-10PSZ
IC128	8-759-742-79	P8742AH-SY143K2. 4800
IC129	8-759-987-84	SN7406NS
IC131	8-759-987-76	DS1287
IC132	8-759-929-99	SN74LS32NS
IC133	8-759-987-55	VL16C452QC
IC134, 135	8-759-031-68	MC1489AM
IC136	8-759-031-69	MC1488M
IC137	8-759-987-78	WD37C65B
IC138, 139	8-759-987-80	SN74LS245NS
IC140	8-759-933-65	SN74LS244NS
IC141	8-759-145-78	μPD65005GC-306-3B6
IC142	8-759-930-36	SN74LS126ANS
IC143	8-759-987-92	SN74ALS10ANS
IC144	8-759-929-78	SN74LS04NS
IC201-208	8-759-944-61	MB81464-10PSZ

Ref. No.	Parts No.	Description
IC209, 210	8-759-933-65	SN74LS244NS
IC211, 212	8-759-987-80	SN74LS245NS
IC213	8-759-987-79	PVGA1A
IC214, 215	8-759-987-81	SN74F241NS
IC217	8-759-987-82	74AC00SJ
IC218	8-759-982-21	RC78L05A
IC219	8-759-100-94	μPC358G2
IC220	8-759-918-71	CX23065
IC221-223	8-759-145-77	μPD42102G-3
IC224	8-759-143-57	μPD65006GF-325-3B8
IC225	8-759-987-83	SN74F240NS
IC226	8-759-930-35	SN74LS125ANS
IC227	8-759-987-80	SN74LS245NS
IC228	8-759-143-59	μPD65013S-526
IC229	8-759-934-11	SN74ALS32NS
IC230-232	8-759-231-68	TMM2018AP-25
IC233-235	8-759-143-58	μPD6902C
IC236	8-759-100-94	μPC358G2
IC240	8-759-945-29	TL601CPS
ICS100	1-526-962-11	SOCKET, IC (PCC PACKAGE) 68P
ICS114	*1-526-971-11	SOCKET, IC 28P
ICS115	*1-526-971-11	SOCKET, IC 28P
ICS131	1-526-970-11	SOCKET, IC 24P
JP201	*1-564-948-11	PIN, CONNECTOR 3P
JP202	1-564-952-21	PIN, CONNECTOR 6P
JP204, 205	1-564-947-11	PIN, CONNECTOR 2P
L307	1-459-940-11	COIL, VARIABLE
L308	1-408-773-31	INDUCTOR CHIP 4. 7 20%
L309-312	1-410-180-51	INDUCTOR CHIP 0. 1 20%
L313	1-410-670-31	INDUCTOR 39 20%
OSC100	1-577-440-11	OSCILLATOR, CRYSTAL
OSC101	1-577-442-11	OSCILLATOR, CRYSTAL
OSC102	1-577-443-11	OSCILLATOR, CRYSTAL
OSC103	1-577-441-11	OSCILLATOR, CRYSTAL

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Ref. No.	Parts No.	Description
R001-005	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R017-023	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R030-038	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R101-120	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R123-165	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R166-192	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R193-197	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R198-205	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R206	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R207	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R208-212	1-216-036-00	METAL GLAZE CHIP 300 5% 1/10W
R213-216	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R217-225	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R226-231	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R234, 235	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R236, 240	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R241-243	1-216-295-00	METAL GLAZE CHIP 0 5% 1/10W
R246	1-216-295-00	METAL GLAZE CHIP 0 5% 1/10W
R247, 248	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R249	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R250	1-216-073-00	METAL GLAZE CHIP 10K 5% 1/10W
R252-293	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R295-299	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R301-303	1-216-009-00	METAL GLAZE CHIP 22 5% 1/10W
R303-312	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R313	1-216-295-00	METAL GLAZE CHIP 0 5% 1/10W
R314, 315	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R316	1-216-295-00	METAL GLAZE CHIP 0 5% 1/10W
R317, 318	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R319-326	1-216-295-00	METAL GLAZE CHIP 0 5% 1/10W
R327-345	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R346	1-216-009-00	METAL GLAZE CHIP 22 5% 1/10W
R347-351	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R352	1-216-624-11	METAL GLAZE CHIP 75 1% 1/10W
R353	1-216-634-11	METAL GLAZE CHIP 200 1% 1/10W
R354	1-216-624-11	METAL GLAZE CHIP 75 1% 1/10W
R355	1-216-634-11	METAL GLAZE CHIP 200 1% 1/10W
R356	1-216-624-11	METAL GLAZE CHIP 75 1% 1/10W
R357	1-216-634-11	METAL GLAZE CHIP 200 1% 1/10W
R358	1-216-332-11	METAL GLAZE CHIP 11K 1% 1/10W
R359	1-216-324-11	METAL GLAZE CHIP 10K 1% 1/10W
R360	1-216-057-00	METAL GLAZE CHIP 2.2K 5% 1/10W
R365	1-216-085-00	METAL GLAZE CHIP 33K 5% 1/10W
R366	1-216-105-00	METAL GLAZE CHIP 220K 5% 1/10W
R367	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R368	1-216-061-00	METAL GLAZE CHIP 3.3K 5% 1/10W
R369	1-216-101-00	METAL GLAZE CHIP 150K 5% 1/10W
R370, 371	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R372	1-216-081-00	METAL GLAZE CHIP 22K 5% 1/10W
R373	1-216-045-00	METAL GLAZE CHIP 680 5% 1/10W
R374, 375	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R378	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R379	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R380	1-216-326-11	METAL GLAZE CHIP 1.8K 1% 1/10W
R381	1-216-083-00	METAL GLAZE CHIP 27K 5% 1/10W
R382	1-216-057-00	METAL GLAZE CHIP 2.2K 5% 1/10W
R383	1-216-295-00	METAL GLAZE CHIP 0 5% 1/10W
R384	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
R385	1-216-057-00	METAL GLAZE CHIP 2.2K 5% 1/10W
R386	1-216-017-00	METAL GLAZE CHIP 47 5% 1/10W
R390-399	1-216-013-00	METAL GLAZE CHIP 33 5% 1/10W
SW301	1-553-510-00	SLIDE
TH301, 302	1-202-850-00	THERMISTOR, POSITIVE
X100	1-567-881-11	VIBRATOR, CRYSTAL
X201	1-577-575-11	OSCILLATOR, CRYSTAL
X202	1-577-436-11	OSCILLATOR, CRYSTAL
X203	1-577-437-11	OSCILLATOR, CRYSTAL

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9-2-7. VS-39 Board

Ref. No.	Parts No.	Description
⚠	*A-8051-510-A	MOUNTED C B, VS-39
C400, 401	1-124-589-11	ELECT 47 20% 16V
C402	1-163-115-00	CERAMIC CHIP 82pF 5% 50V
C403	1-163-101-00	CERAMIC CHIP 22pF 5% 50V
C404	1-126-101-11	ELECT 100 20% 16V
C405	1-163-038-00	CERAMIC CHIP 0.1 25V
C406	1-124-438-00	ELECT 1 20% 50V
C407	1-163-121-00	CERAMIC CHIP 150pF 5% 50V
C408-410	1-163-021-00	CERAMIC CHIP 0.01 10% 50V
C411	1-163-038-00	CERAMIC CHIP 0.1 25V
C412	1-124-589-11	ELECT 47 20% 16V
C413	1-126-157-11	ELECT 10 20% 16V
C414	1-163-145-00	CERAMIC CHIP 0.0015 5% 50V
C415	1-163-111-00	CERAMIC CHIP 56pF 5% 50V
C416	1-163-123-00	CERAMIC CHIP 180pF 5% 50V
C417	1-163-119-00	CERAMIC CHIP 120pF 5% 50V
C418, 419	1-124-589-11	ELECT 47 20% 16V
C420	1-126-101-11	ELECT 100 20% 16V
C421	1-163-038-00	CERAMIC CHIP 0.1 25V
C422	1-124-438-00	ELECT 1 20% 50V
C423	1-163-021-00	CERAMIC CHIP 0.01 10% 50V
C424	1-163-038-00	CERAMIC CHIP 0.1 25V
C425	1-163-099-00	CERAMIC CHIP 18pF 5% 50V
C426	1-163-101-00	CERAMIC CHIP 22pF 5% 50V
C427, 428	1-136-161-00	FILM 0.047 5% 50V
C429	1-124-465-00	ELECT 0.47 20% 50V
C430	1-124-589-11	ELECT 47 20% 16V
C431	1-163-038-00	CERAMIC CHIP 0.1 25V
C432-434	1-124-438-00	ELECT 1 20% 50V
C435	1-163-038-00	CERAMIC CHIP 0.1 25V
C436	1-124-589-11	ELECT 47 20% 16V
C437, 438	1-163-038-00	CERAMIC CHIP 0.1 25V
C439	1-124-589-11	ELECT 47 20% 16V
C440	1-126-157-11	ELECT 10 20% 16V
C441, 442	1-163-038-00	CERAMIC CHIP 0.1 25V
C443	1-126-157-11	ELECT 10 20% 16V
C444-447	1-163-038-00	CERAMIC CHIP 0.1 25V
C448	1-126-157-11	ELECT 10 20% 16V
C449-452	1-163-038-00	CERAMIC CHIP 0.1 25V
C453	1-163-021-00	CERAMIC CHIP 0.01 10% 50V
C454	1-163-125-00	CERAMIC CHIP 220pF 10% 50V

Ref. No.	Parts No.	Description
C455	1-131-342-00	TANTALUM 0.15 10% 35V
C456	1-163-141-00	CERAMIC CHIP 0.001 5% 50V
C457	1-163-038-00	CERAMIC CHIP 0.1 25V
C458	1-108-792-11	MYLAR 0.001 5% 50V
C459	1-163-145-00	CERAMIC CHIP 0.0015 5% 50V
C460	1-163-038-00	CERAMIC CHIP 0.1 25V
C461	1-124-589-11	ELECT 47 20% 16V
C462	1-163-021-00	CERAMIC CHIP 0.01 10% 50V
C463	1-126-157-11	ELECT 10 20% 16V
C464, 465	1-163-038-00	CERAMIC CHIP 0.1 25V
C466	1-163-135-00	CERAMIC CHIP 560pF 10% 50V
C467	1-163-038-00	CERAMIC CHIP 0.1 25V
C468	1-136-156-00	FILM 0.018 5% 50V
C469	1-163-141-00	CERAMIC CHIP 0.001 5% 50V
C470	1-136-167-00	FILM 0.15 5% 50V
C471	1-163-038-00	CERAMIC CHIP 0.1 25V
C472, 473	1-163-101-00	CERAMIC CHIP 22pF 5% 50V
C474	1-163-038-00	CERAMIC CHIP 0.1 25V
C475, 476	1-124-438-00	ELECT 1 20% 50V
C477	1-163-021-00	CERAMIC CHIP 0.01 10% 50V
C478	1-130-728-00	FILM 0.0022 5% 50V
C479	1-108-798-11	MYLAR 0.0033 5% 50V
C480	1-124-589-11	ELECT 47 20% 16V
C482	1-136-161-00	FILM 0.047 5% 50V
C483	1-136-157-00	FILM 0.022 5% 50V
C484	1-124-589-11	ELECT 47 20% 16V
C485	1-163-038-00	CERAMIC CHIP 0.1 25V
C486	1-124-589-11	ELECT 47 20% 16V
C487	1-126-157-11	ELECT 10 20% 16V
C488	1-108-792-11	MYLAR 0.001 5% 50V
C489	1-163-141-00	CERAMIC CHIP 0.001 5% 50V
C490	1-126-157-11	ELECT 10 20% 16V
C491	1-163-038-00	CERAMIC CHIP 0.1 25V
C492	1-126-157-11	ELECT 10 20% 16V
C493	1-163-038-00	CERAMIC CHIP 0.1 25V
C494	1-124-589-11	ELECT 47 20% 16V
C495	1-163-038-00	CERAMIC CHIP 0.1 25V
C496	1-126-157-11	ELECT 10 20% 16V
C497	1-163-038-00	CERAMIC CHIP 0.1 25V
C498	1-124-589-11	ELECT 47 20% 16V
C499, 500	1-163-038-00	CERAMIC CHIP 0.1 25V
C501-503	1-126-157-11	ELECT 10 20% 16V
C504, 505	1-163-038-00	CERAMIC CHIP 0.1 25V
C506-508	1-126-157-11	ELECT 10 20% 16V
C509	1-163-038-00	CERAMIC CHIP 0.1 25V
C510	1-163-125-00	CERAMIC CHIP 220pF 10% 50V
C511, 512	1-163-141-00	CERAMIC CHIP 0.001 5% 50V (serial Nos. 10001-10150)
C513, 514	1-124-589-11	ELECT 47 20% 16V
C515	1-163-125-00	CERAMIC CHIP 220pF 5% 50V
C516	1-124-234-00	ELECT 22 20% 16V

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Ref. No.	Parts No.	Description
CN400	1-506-471-11	PIN, 6P
CN401	1-568-541-11	SQUARE TYPE (S) 34P
CN402	1-506-469-11	PIN, 4P
CN403	1-568-540-11	JACK, PIN 2P
D400-404	8-719-108-24	1SS223
D405	8-719-800-76	1SS226
D406	8-719-108-24	1SS223
D407	8-719-903-27	1SS168
DL400	1-415-356-11	DELAY LINE, 1H
DL401	1-415-251-00	DELAY LINE
FB401, 402	1-543-645-11	BEAD, FERRITE (CHIP) (See NOTE on Page 5-60)
IC400	8-752-030-75	V7020
IC401	8-759-135-80	μPD358C
IC402-404	8-752-329-47	CXD1172M
IC405	8-759-007-21	MC74HC4053N
IC406	8-759-103-93	μPD393C
IC407, 408	8-759-205-21	TC74HC221F
IC409	8-759-232-31	TC74HC74AP
IC410	8-759-202-86	TC74HC123P
IC411	8-759-204-94	TC74HC00F
IC412	8-759-206-28	TC74HC123F
IC413	8-752-321-16	CXD1030M
IC414	8-759-205-00	TC74HC14F
IC415	8-759-800-11	LA7801
IC416	8-759-206-28	TC74HC123F
IC417	8-759-278-09	TA78L009AP
IC418	8-759-982-05	RC7805FA
IC419	8-759-990-84	TL084CN
L400, 401	1-408-780-21	INDUCTOR CHIP 18
L402	1-408-779-31	INDUCTOR CHIP 15
L403, 404	1-408-785-21	INDUCTOR CHIP 47
L405	1-408-780-21	INDUCTOR CHIP 18
L406-411	1-408-785-21	INDUCTOR CHIP 47
L412	1-408-797-11	INDUCTOR CHIP 470
L413	1-408-785-21	INDUCTOR CHIP 47
L415	1-408-773-31	INDUCTOR CHIP 4.7
L416	1-408-785-21	INDUCTOR CHIP 47

Ref. No.	Parts No.	Description
LV400	1-408-513-00	COIL, VARIABLE
LV401	1-235-161-00	FILTER, BAND-PASS
Q400	8-729-216-22	2SA1162
Q401-407	8-729-100-66	2SC1623
Q408, 409	8-729-216-22	2SA1162
Q410-414	8-729-100-66	2SC1623
Q415	8-729-216-22	2SA1162
Q416-419	8-729-100-66	2SC1623
Q420, 421	8-729-100-66	2SC1623
Q422	8-729-216-22	2SA1162
R400	1-216-083-00	METAL GLAZE CHIP 27K 5% 1/10W
R401	1-216-073-00	METAL GLAZE CHIP 10K 5% 1/10W
R402	1-216-037-00	METAL GLAZE CHIP 330 5% 1/10W
R403, 404	1-216-041-00	METAL GLAZE CHIP 470 5% 1/10W
R405	1-216-053-00	METAL GLAZE CHIP 1.5K 5% 1/10W
R406	1-216-041-00	METAL GLAZE CHIP 470 5% 1/10W
R407	1-216-057-00	METAL GLAZE CHIP 2.2K 5% 1/10W
R408	1-216-045-00	METAL GLAZE CHIP 680 5% 1/10W
R409	1-216-041-00	METAL GLAZE CHIP 470 5% 1/10W
R410	1-216-021-00	METAL GLAZE CHIP 68 5% 1/10W
R411	1-216-031-00	METAL GLAZE CHIP 180 5% 1/10W
R412	1-216-037-00	METAL GLAZE CHIP 330 5% 1/10W
R413-417	1-216-045-00	METAL GLAZE CHIP 680 5% 1/10W
R418, 419	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R420	1-216-043-00	METAL GLAZE CHIP 560 5% 1/10W
R421	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R422	1-216-053-00	METAL GLAZE CHIP 1.5K 5% 1/10W
R423	1-216-054-00	METAL GLAZE CHIP 1.6K 5% 1/10W
R424	1-216-067-00	METAL GLAZE CHIP 5.6K 5% 1/10W
R425	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R426	1-216-027-00	METAL GLAZE CHIP 120 5% 1/10W
R427	1-216-099-00	METAL GLAZE CHIP 120K 5% 1/10W
R428	1-216-037-00	METAL GLAZE CHIP 330 5% 1/10W
R429	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R430	1-216-041-00	METAL GLAZE CHIP 470 5% 1/10W
R431, 432	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R433	1-216-035-00	METAL GLAZE CHIP 270 5% 1/10W
R434	1-216-037-00	METAL GLAZE CHIP 330 5% 1/10W
R435	1-216-043-00	METAL GLAZE CHIP 560 5% 1/10W
R436	1-216-055-00	METAL GLAZE CHIP 1.8K 5% 1/10W

NOTE:

1. **The shaded and ⚠-marked components are critical to safety. Replace only with same components as specified.**
2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.

Ref. No.	Parts No.	Description
R437	1-216-057-00	METAL GLAZE CHIP 2.2K 5% 1/10W
R438	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R439	1-216-073-00	METAL GLAZE CHIP 10K 5% 1/10W
R440	1-216-079-00	METAL GLAZE CHIP 18K 5% 1/10W
R441	1-216-061-00	METAL GLAZE CHIP 3.3K 5% 1/10W
R442	1-216-051-00	METAL GLAZE CHIP 1.2K 5% 1/10W
R443	1-216-097-00	METAL GLAZE CHIP 100K 5% 1/10W
R444	1-216-051-00	METAL GLAZE CHIP 1.2K 5% 1/10W
R445	1-216-067-00	METAL GLAZE CHIP 5.6K 5% 1/10W
R446	1-216-057-00	METAL GLAZE CHIP 2.2K 5% 1/10W
R447	1-216-077-00	METAL GLAZE CHIP 15K 5% 1/10W
R448	1-216-103-00	METAL GLAZE CHIP 180K 5% 1/10W
R449	1-216-111-00	METAL GLAZE CHIP 390K 5% 1/10W
R450	1-216-050-00	METAL GLAZE CHIP 1.1K 5% 1/10W
R451	1-216-053-00	METAL GLAZE CHIP 1.5K 5% 1/10W
R452	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R453	1-216-025-00	METAL GLAZE CHIP 100 5% 1/10W
R454	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R455	1-216-025-00	METAL GLAZE CHIP 100 5% 1/10W
R456	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R457	1-216-025-00	METAL GLAZE CHIP 100 5% 1/10W
R458-460	1-216-017-00	METAL GLAZE CHIP 47 5% 1/10W
R461	1-216-069-00	METAL GLAZE CHIP 6.8K 5% 1/10W
R462	1-216-542-11	METAL GLAZE CHIP 12K 1% 1/10W
R463	1-216-656-11	METAL GLAZE CHIP 1.6K 1% 1/10W
R464	1-216-329-11	METAL GLAZE CHIP 5.1K 1% 1/10W
R465	1-216-081-00	METAL GLAZE CHIP 22K 5% 1/10W
R466	1-216-099-00	METAL GLAZE CHIP 120K 5% 1/10W
R467, 468	1-216-059-00	METAL GLAZE CHIP 2.7K 5% 1/10W
R469	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R470	1-216-100-00	METAL GLAZE CHIP 130K 5% 1/10W
R471	1-216-083-00	METAL GLAZE CHIP 27K 5% 1/10W
R472	1-218-161-11	METAL GLAZE CHIP 62K 1% 1/10W
R473	1-216-061-00	METAL GLAZE CHIP 3.3K 5% 1/10W
R474	1-216-099-00	METAL GLAZE CHIP 120K 5% 1/10W
R475	1-216-059-00	METAL GLAZE CHIP 2.7K 5% 1/10W
R476	1-216-099-00	METAL GLAZE CHIP 120K 5% 1/10W
R477	1-216-051-00	METAL GLAZE CHIP 1.2K 5% 1/10W
R478	1-216-073-00	METAL GLAZE CHIP 10K 5% 1/10W
R479	1-216-095-00	METAL GLAZE CHIP 82K 5% 1/10W
R480	1-216-089-00	METAL GLAZE CHIP 47K 5% 1/10W
R481	1-216-105-00	METAL GLAZE CHIP 220K 5% 1/10W
R482	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R483	1-216-075-00	METAL GLAZE CHIP 12K 5% 1/10W
R484	1-216-093-00	METAL GLAZE CHIP 68K 5% 1/10W
R485	1-216-067-00	METAL GLAZE CHIP 5.6K 5% 1/10W
R486	1-216-065-00	METAL GLAZE CHIP 4.7K 5% 1/10W
R487	1-216-073-00	METAL GLAZE CHIP 10K 5% 1/10W
R488	1-216-055-00	METAL GLAZE CHIP 1.8K 5% 1/10W
R489	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R490	1-216-061-00	METAL GLAZE CHIP 3.3K 5% 1/10W
R491	1-216-069-00	METAL GLAZE CHIP 6.8K 5% 1/10W
⚠R492	1-216-417-11	METAL OXIDE 4.7 5% 5W
R493-495	1-216-089-00	METAL GLAZE CHIP 47K 5% 1/10W
R496	1-216-053-00	METAL GLAZE CHIP 1.5K 5% 1/10W
R497	1-216-083-00	METAL GLAZE CHIP 27K 5% 1/10W
R498	1-216-059-00	METAL GLAZE CHIP 2.7K 5% 1/10W
R499, 500	1-216-082-00	METAL GLAZE CHIP 24K 5% 1/10W
R501-504	1-216-089-00	METAL GLAZE CHIP 47K 5% 1/10W
R505, 506	1-216-045-00	METAL GLAZE CHIP 680 5% 1/10W
R507	1-216-088-00	METAL GLAZE CHIP 43K 5% 1/10W
R508, 509	1-216-037-00	METAL GLAZE CHIP 330 5% 1/10W
R510, 511	1-216-089-00	METAL GLAZE CHIP 47K 5% 1/10W
R512	1-216-029-00	METAL GLAZE CHIP 150 5% 1/10W
R513	1-216-081-00	METAL GLAZE CHIP 22K 5% 1/10W
R520	1-216-029-00	METAL GLAZE CHIP 150 5% 1/10W
R521	1-216-049-00	METAL GLAZE CHIP 1K 5% 1/10W
R522	1-249-425-11	CARBON 4.7K 5% 1/4W
RV400	1-230-519-11	ADJ, METAL GLAZE 470
RV401	1-230-520-11	ADJ, METAL GLAZE 1K
RV402	1-230-523-11	ADJ, METAL GLAZE 10K
RV403	1-237-513-21	ADJ, CERMET 200
RV404	1-230-523-11	ADJ, METAL GLAZE 10K
RV406, 407	1-230-526-11	ADJ, METAL GLAZE 47K
RV408	1-237-517-21	ADJ, CERMET 5K
RV409	1-230-522-11	ADJ, METAL GLAZE 4.7K
RV410	1-230-521-11	ADJ, METAL GLAZE 2.2K
X400	1-567-505-11	OSCILLATOR, CRYSTAL
X401	1-567-878-11	VIBRATOR, CRYSTAL

NOTE:

1. **The shaded and ⚠-marked components are critical to safety.**
Replace only with same components as specified.

2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay shouid be anticipated when ordering these items.

Ref. No.	Parts No.	Description
9-3. ACCESSORIES AND PACKING MATERIAL		
⚠	1-551-812-00	CORD, POWER (WITH SHIELD)
	*3-694-922-01	SHEET, PROTECTION
	*3-701-625-01	BAG, POLYETHYLENE
	3-750-303-21	MANUAL, INSTRUCTION
9-4. FIXTURES		
	*J-6093-490-A	EXTENSION BOARD ASSY
	*J-6093-570-A	IC EXTRACTION TOOL, 68 PLCC
	*J-	BOARD STAND KIT, VS-39
	*J-6200-200-A	KEYTOP EXTRACTION TOOL

NOTE:

1. **The shaded and ⚠-marked components are critical to safety.**
   Replace only with same components as specified.
2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.

CHAPTER 10
EXPLANATION OF SCK-5015

10-1. OPERATION

10-1-1. Overview

The SCK-5015 is a internal hard disk drive unit for the Sony VIW-5000 VIEW System. The unit has a memory capacity of 42.6M bytes. It is controlled by the inner interface board. This manual explains procedures for installing the unit.

Notes

- After installing (or removing) the SCK-5015, set (reset) the VIW-5000's SETUP RAM using the installation program provided in the SMW-5001 VIEW/VGA Operating System Package. In addition, physically (and logically) format the hard disk, create DOS (Disk Operating System) partitions and install various utility programs using the same installation program.
- If the user intends to expand the VIW-5000's graphics memory, it is recommended install the SMI-5051 Graphics Memory Expansion board prior to installing the internal hard disk drive unit. Otherwise, the installed drive unit must be temporarily removed to access the graphics memory expansion connectors.

10-1-2. Installation

10-1-2-1. Precautions

- Before installation, turn off the power to the system and remove the power cable from the wall outlet.
- The hard disk unit consists of delicate high-precision component. Do not drop or bump it against other objects.

10-1-2-2. Removing

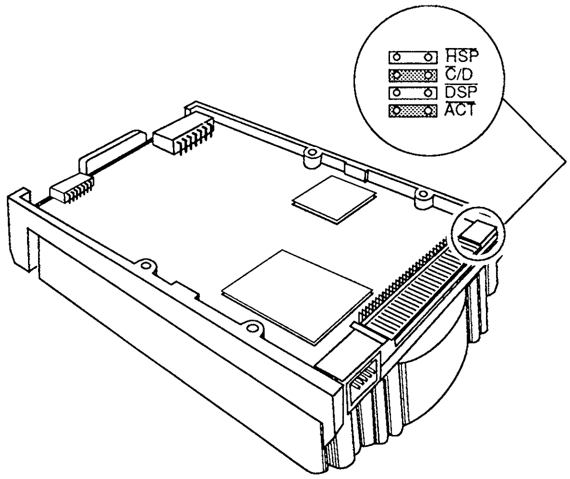
1. Remove the cover assembly.
   Refer to Chapter 2-1-1.

2. Remove the videodisc player part.
   Refer to Chapter 2-1-2.

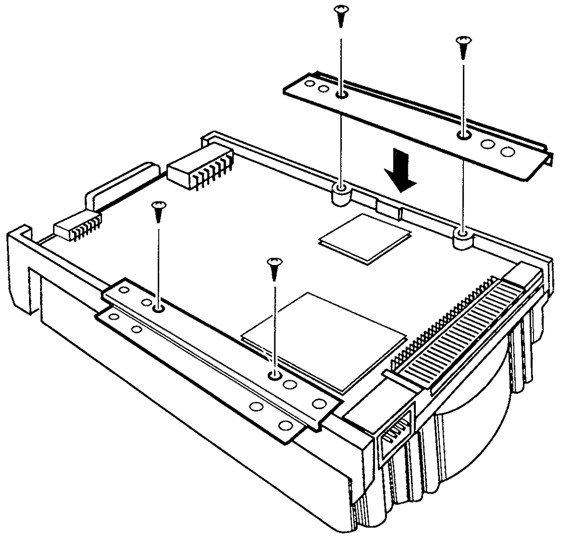
3. Remove the shielding sheet.
   Refer to Chapter 2-1-3.

10-1-2-3. Preparing

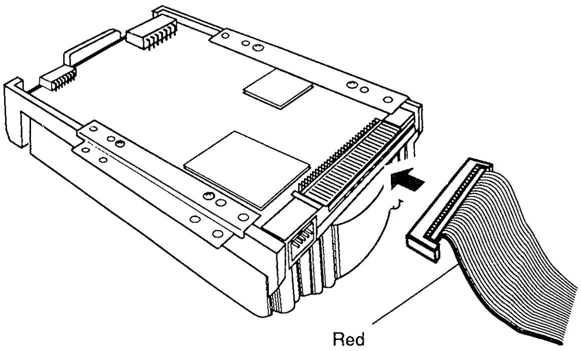
1. Place the unit in a flat surface with its interface board side up.
2. Check the jumper pin setting (J2). The jumpers must be installed on the $\overline{C}$/D and $\overline{ACT}$ pins as shown below.



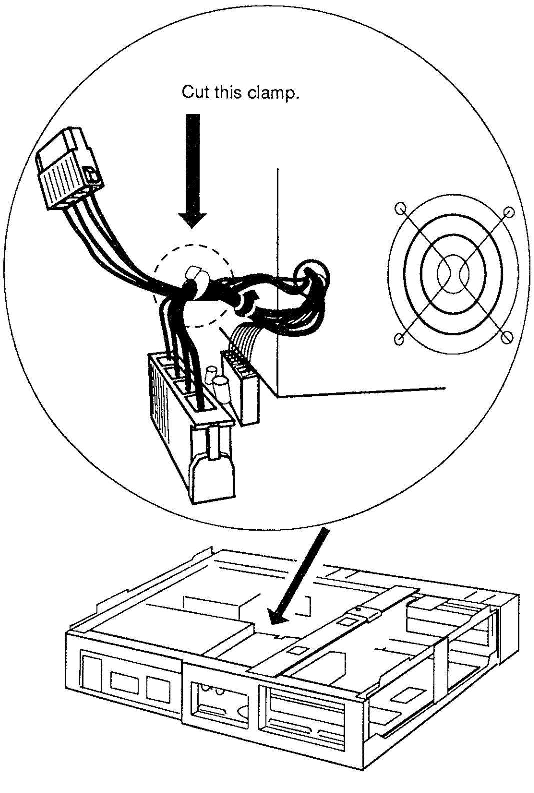
3. Attach the two mounting rails to the drive and secure the rails using four screws (those with paring washers).



4. Insert the flat data cable's connector (provided with a dummy pin) to the hard disk drive. The cable's red wire must be facing left.

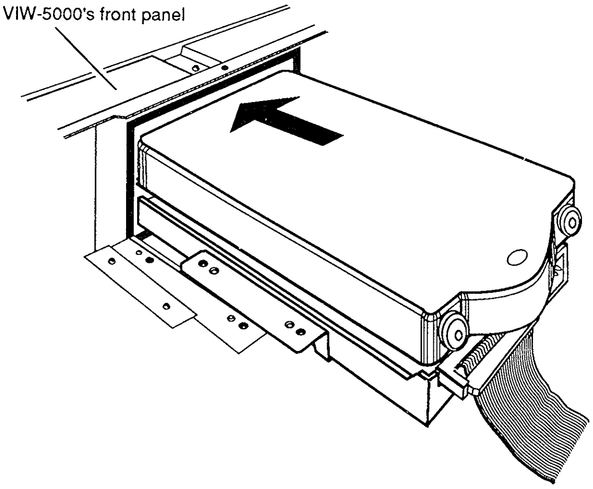


5. The VIW-5000 system provides a power cable for the hard disk drive, which is grouped together with other cables. Cut the clamp fastening the cables.

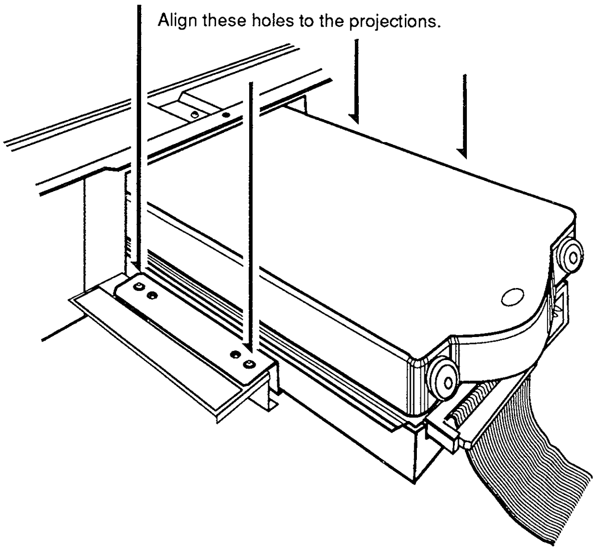

Cut this clamp.

10-1-2-4. Mounting

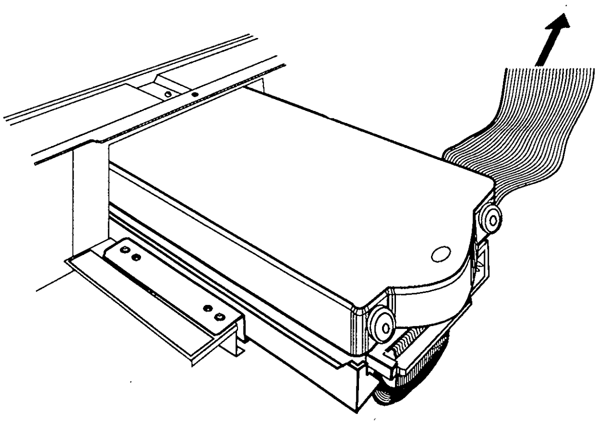
1. Hold the drive's mounting rails with the interface board side down.
2. Insert the drive's front end into the rectangular hole of the VIW-5000's chassis.


VIW-5000's front panel

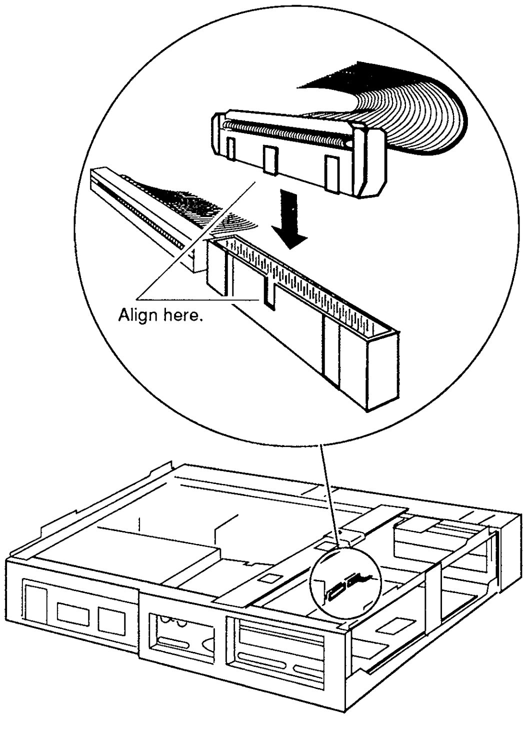
3. Align the holes of the mounting rails with the projections on the VIW-5000's chassis.


Align these holes to the projections.

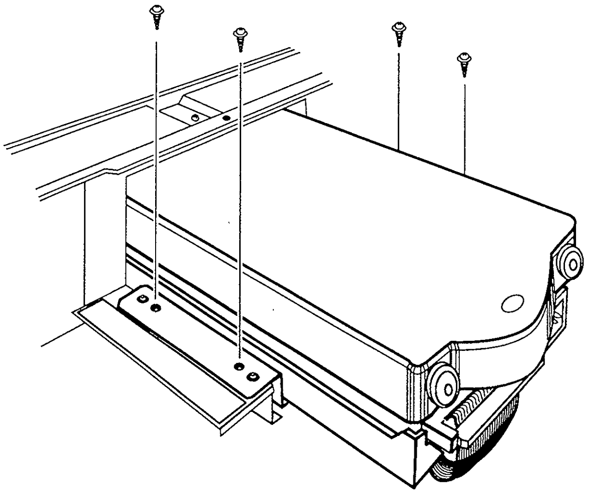
4. Place the drive's data cable under the drive so that it is not in close proximity with any internal power lines.



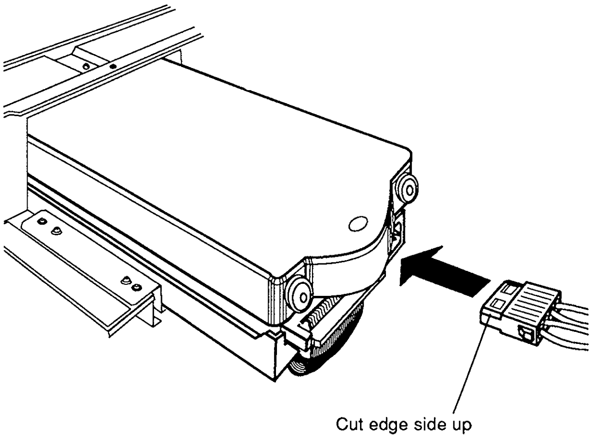
5. Insert the data cable's connector to the socket on the SY-143 board, aligning the groove provided on the cable's connector to that on the socket.



6. Secure the drive with four screws (those with paring washers).

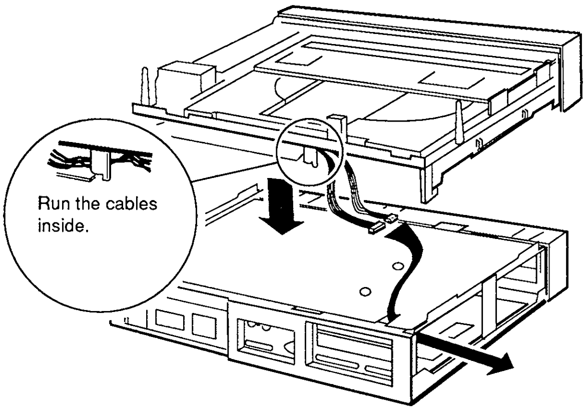


7. Connect the power cable to the drive.



12-1-2-4. Reinstalling

Follow the instructions provided in Section 10-1-2-2 "Removing" in reverse order.
Be sure to pass the data cables inside the computer part.



Tips

When placing the videodisc player part in position, shift it slightly forward and then pull it backward on the computer part. This will make the operation easier.

Notes

- Be sure to connect the internal cable before reinstalling the cover assembly.
- Be aware of internal wiring when placing the videodisc player part in position. Take a moment to check that no wires are squeezed under the unit.

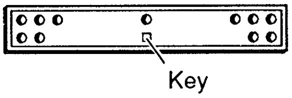
10-1-3. Specifications

Capacity	42.6M bytes (formatted)
Drive type	17 (translate mode)
Actuator type	Rotary voice-coil
Number of disks	2
Data surface	4
Data heads	4
Servomechanism	Embedded
Track per surface	805
Track density	1000 TPI
Track capacity	13,312 bytes (formatted)
Bytes per block	512
Blocks per track	26
Blocks per drive	83,270
Seek times	
Track to track :	10m sec.
Average :	29m sec.
Average latency	8.33m sec.
Rotation speed	3600 r.p.m. ± 0.1 %
Controller overhead	1m sec.
To/from media data transfer rate	1M bytes per sec.
To/from buffer data transfer rate	4/5M bytes per sec.
Start time	7 seconds typ.
Stop time	7 seconds typ.
Interleave	1 : 1
Buffer size	8K bytes
Power requirement	+12 V DC ± 5 %, 250 mA* typ. +5 V DC ± 5 %, 250 mA typ.
Operating conditions	
Temperature :	+5 to +35℃ (+41 to +95°F)
Humidity :	25 to 80 % (at +25℃ or +75°F)
Storage conditions	
Temperature :	−20 to +60℃ (−4 to +140°F)
Dimensions	38 × 101 × 146 mm (w/h/d) $\left(1\frac{1}{2} \times 4 \times 5\frac{3}{4}\text{ inches}\right)$
Weight	700 g (1 lb. 9 oz.)

*1A for 5 seconds at power on.

10-1-4. I/O Signal Pin Assignment

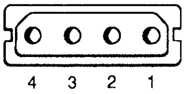
40-pin interface connector



Pin	Signal
1	– HOST RESET
3	HOST DATA 7
5	HOST DATA 6
7	HOST DATA 5
9	HOST DATA 4
11	HOST DATA 3
13	HOST DATA 2
15	HOST DATA 1
17	HOST DATA 0
19	GND
21	reserved
23	– HOST I/O WRITE
25	– HOST I/O READ
27	reserved
29	reserved
31	HOST IRQ 14
33	HOST ADDR 1
35	HOST ADDR 0
	– HOST CS0
	– HOST SLV/ACT

Pin	Signal
37	GND
39	HOST DATA 8
2	HOST DATA 9
4	HOST DATA 10
6	HOST DATA 11
8	HOST DATA 12
10	HOST DATA 13
12	HOST DATA 14
14	HOST DATA 15
16	(KEY)
18	GND
20	GND
22	GND
24	HOST ALE
26	GND
28	– HOST I/O 16
30	– HOST PDIAG
32	HOST ADDR 2
	– HOST CS1
	GND

J3 power-in connector



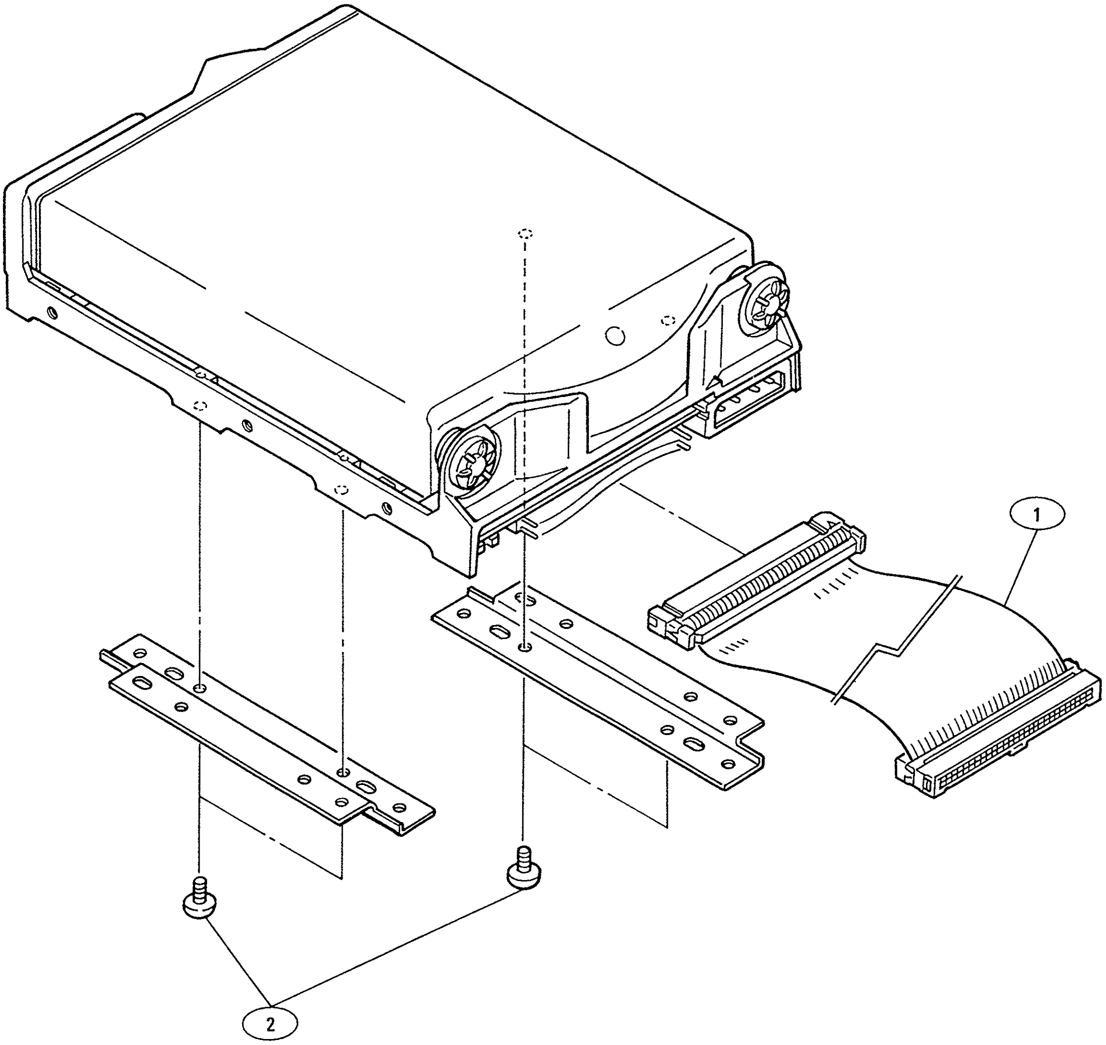
Pin	Signal
1	+ 12V
2	GND
3	GND
4	+ 5V

10-2. SERVICE INFORMATION

Unit exchange is applied for repairing of this model. Before starting the repair of the unit, perform diagnosis with the maintenance disk.

10-3. REPAIR PARTS

No.	Parts No.	Description
1	1-574-817-11	WIRE ASSY, FLAT SLIT (40 CORE)
2	4-606-940-01	SCREW (UNIFY), SMALL
	7-682-647-09	SCREW + PSW 3 × 6



NOTE:

1. **The shaded and ⚠ -marked components are critical to safety. Replace only with same components as specified.**
2. Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
3. Item with no part number and/or description are not stocked because they are seldom required for routine service.

CHAPTER 11
EXPLANATION OF SMI-5050

11-1. OPERATION

11-1-1. Features

The SMI-5050 is a 2M-byte expansion memory for the Sony VIW-5000 VIEW System, capable of increasing the system memory to 2.6M bytes. It consists of two 1M-byte modules which can easily be installed in the VIW-5000 mother (SY-143) board.

The SMI-5050 features :
- 2M-byte RAM (with parity), 100n sec. access time
- Conforms to the LIM (Lotus／Intel／Microsoft) EMS 4.0 standard and can be used as an expanded memory
- Can also be as used as an extended memory, allowing the user to configure a RAM disk (virtual disk)

Notes
- After installing (or removing) the SMI-5050, set (reset) the VIW-5000's SETUP RAM using the installation program provided in the SMW-5001 VIEW／VGA Operating System Package. For more information including use of the EMS device driver (MM.SYS) and RAM disk driver (RAMDRIVE. SYS), refer to the SMW-5001 manual.
- When used as an expansion memory, the SMI-5050 cannot coexist with a commercially available expansion memory board for the IBM PC／AT.

11-1-2. Installation

11-1-2-1. Precautions
- Before installation, turn off the power to the system and remove the power cable from the wall outlet.
- The module comes packed in an anti-electrostatic protective bag. Avoid touching the RAM chips on the module when removing it from the package or installing it to the system.
- The module is a delicate high-precision component. Do not drop or bump it against other objects.

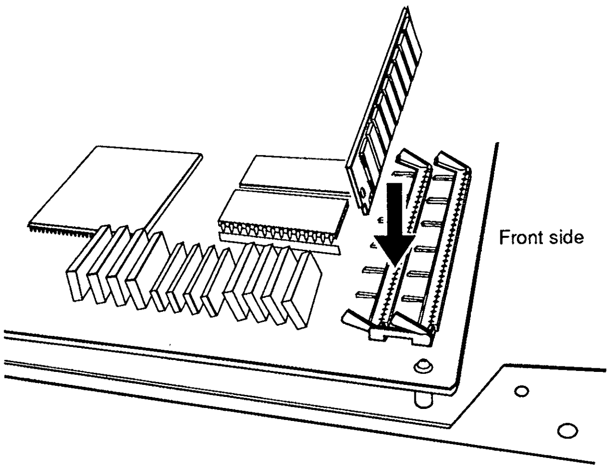
11-1-2-2. Removing
1. Remove the cover assembly.
   Refer to Chapter 2-1-1.

2. Remove the videodisc player part.
   Refer to Chapter 2-1-2.

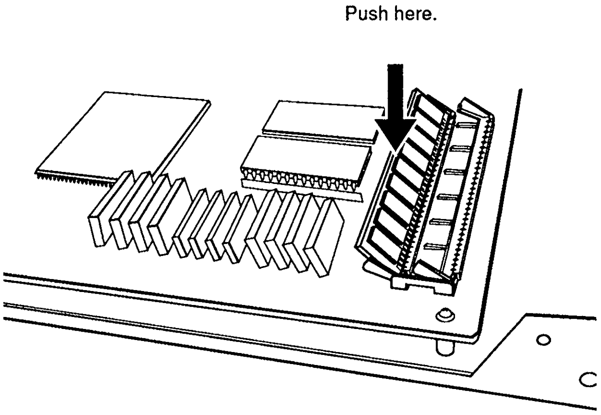
3. Remove the shielding sheet.
   Refer to Chapter 2-1-3.

11-1-2-3. Mounting
The memory module sockets are located in the left side corner (looking at the system from the front of the SY-143 board.

1. Insert one module in the socket (CN116-1／2).
   The module's metal contact side must go in first.



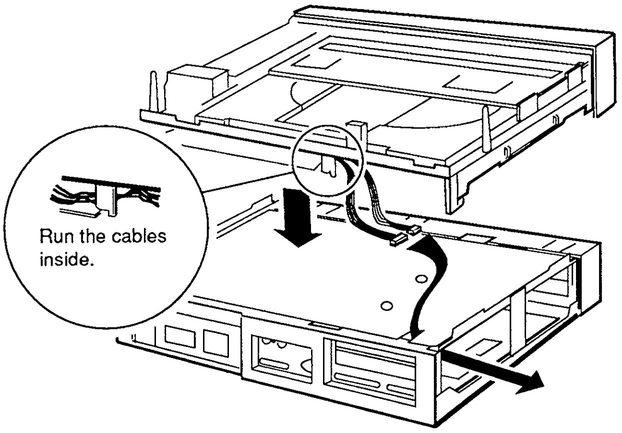
2. Lightly push the top of the module down until it snaps into the socket.



3. Insert the second module in the remaining socket (CN116-2／2).

11-1-2-4. Reinstalling

Follow the instructions provided in Section 11-1-2-2 "Removing" in reverse order.
Be sure to pass the data cables inside the unit.


Run the cables inside.

Tips

When placing the videodisc player part in position, shift it slightly forward and then pull it backward on the computer part. This will make the operation easier.

Notes

- Be sure to connect the internal cable before reinstalling the cover assembly.
- Be aware of internal wiring when placing the videodisc player part in position. Take a moment to check that no wires are squeezed under the unit.

11-1-3. Specifications

Memory RAM	2M bytes
Access time	100n sec.
Power requirement	+5V DC ±10%
Current consumption	60 mA typ.
Operating conditions	
Temperature :	+5 to +35℃ (+41 to +95°F)
Humidity :	25 to 80% (at +25℃ or +77°F)
Storage conditions	
Temperature :	−20 to +60℃ (−4 to +140°F)
Dimensions	Approx. 89×5×20.5 mm (w/h/d) $\left(3\frac{5}{8}\times\frac{7}{32}\times\frac{13}{16}\text{ inches}\right)$
Weight	13 g (0.46 oz.)

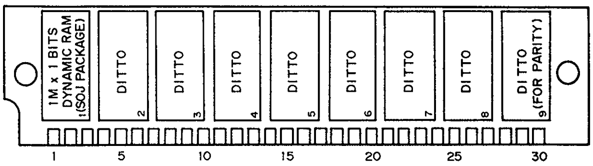
11-2. SERVICE INFORMATION

The SMI-5050 consists of two D-RAM modules [MB85235-10 (FUJITSU) or MH1M09A0J-10 (MITSUBISHI)].
In case of malfunctions, replace with a commercially available equivalent module.

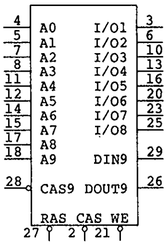
11-3. MODULE BLOCK DIAGRAM

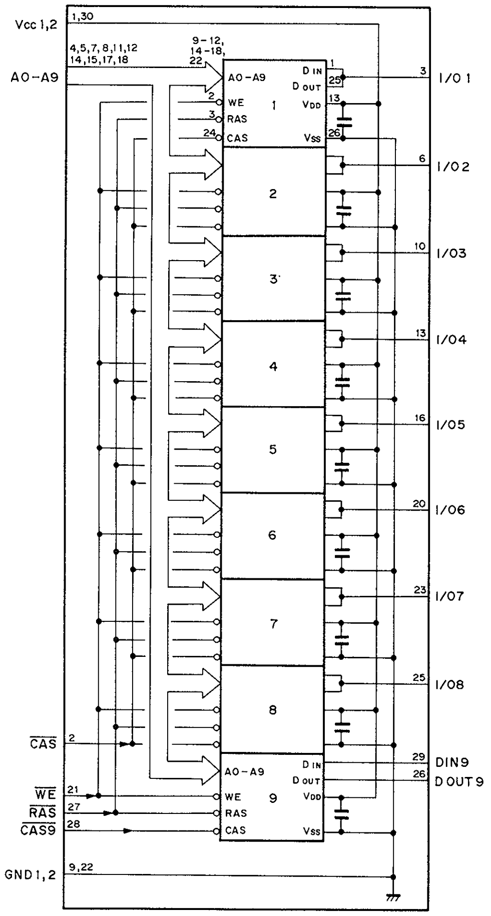
MB85235-10 (FUJITSU) (ACCESS TIME = 100nS)
MH1M09A0J-10 (MITSUBISHI) (ACCESS TIME = 100nS)

C-MOS 1,048,576x9 BITS DYNAMIC RAM MODULE
– MOUNTED VIEW –


1M x 1 BITS DYNAMIC RAM (SOJ PACKAGE)
1
DITTO 2
DITTO 3
DITTO 4
DITTO 5
DITTO 6
DITTO 7
DITTO 8
DITTO (FOR PARITY) 9
1
5
10
15
20
25
30

PIN	SYMBOL	DESCRIPTION
1	VCC1	+5V SUPPLY
2	$\overline{CAS}$	COLUMN ADDRESS STROBE INPUT
3	I/O1	DATA 1 INPUT/OUTPUT
4	A0	ADDRESS 0 INPUT
5	A1	ADDRESS 1 INPUT
6	I/O2	DATA 2 INPUT/OUTPUT
7	A2	ADDRESS 2 INPUT
8	A3	ADDRESS 3 INPUT
9	GND1	GROUND
10	I/O3	DATA 3 INPUT/OUTPUT
11	A4	ADDRESS 4 INPUT
12	A5	ADDRESS 5 INPUT
13	I/O4	DATA 4 INPUT/OUTPUT
14	A6	ADDRESS 6 INPUT
15	A7	ADDRESS 7 INPUT
16	I/O5	DATA 5 INPUT/OUTPUT
17	A8	ADDRESS 8 INPUT
18	A9	ADDRESS 9 INPUT
19	NC	NO CONNECTION
20	I/O6	DATA 6 INPUT/OUTPUT
21	$\overline{WE}$	WRITE ENABLE INPUT
22	GND2	GROUND
23	I/O7	DATA 7 INPUT/OUTPUT
24	NC	NO CONNECTION
25	I/O8	DATA 8 INPUT/OUTPUT
26	DOUT9	DATA 9 OUTPUT
27	$\overline{RAS}$	ROW ADDRESS STROBE INPUT
28	$\overline{CAS9}$	COLUMN ADDRESS STROBE INPUT
29	DIN9	DATA 9 INPUT
30	VCC2	+5V SUPPLY


4 A0
5 A1
7 A2
8 A3
11 A4
12 A5
14 A6
15 A7
17 A8
18 A9
28 CAS9
I/O1 3
I/O2 6
I/O3 10
I/O4 13
I/O5 16
I/O6 20
I/O7 23
I/O8 25
DIN9 29
DOUT9 26
RAS 27
CAS 2
WE 21


Vcc 1,2
1,30
A0–A9
4,5,7,8,11,12
14,15,17,18
9–12,
14–18,
22
A0–A9
D IN
D OUT
WE
RAS
CAS
VDD
VSS
1
2
3
24
25
13
26
1
2
3
4
5
6
7
8
9
3 I/O 1
6 I/O2
10 I/O3
13 I/O4
16 I/O5
20 I/O6
23 I/O7
25 I/O8
29 DIN9
26 D OUT 9
CAS 2
WE 21
RAS 27
CAS9 28
GND 1,2 9,22

CHAPTER 12
EXPLANATION OF SMI-5051

12-1. OPERATION

12-1-1. Features

The SMI-5051 is a graphics memory expansion board for the Sony VIW-5000 VIEW System. Installing this board (RAM-13 board) increases the system's 256K-byte standard graphics memory to 512K bytes and allows 256-color display in 640 × 480 pixel resolution (mode 5F, compatible with the Paradise VGA Professional Card) while the standard graphics memory to only features 16 colors. The RAM-13 board is mounted directly on the system mother board (SY-143 board).

12-1-2. Installation

12-1-2-1. Precautions

- Before installation, turn off the power to the system and remove the power cable from the wall outlet.
- The RAM-13 board comes packed in an anti-electrostatic protective bag. Avoid touching the pins and chips on the board when removing it from the package or installing it to the system.
- The RAM-13 board consists of delicate high-precision component. Do not drop or bump it against other objects.

12-1-2-2. Removing

1. Remove the cover assembly.
   Refer to Chapter 2-1-1.
2. Remove the videodisc player part.
   Refer to Chapter 2-1-2.
3. Remove the shielding sheet.
   Refer to Chapter 2-1-3.
4. Remove the center stay.
   Refer to Chapter 2-1-9 (③ and ④).

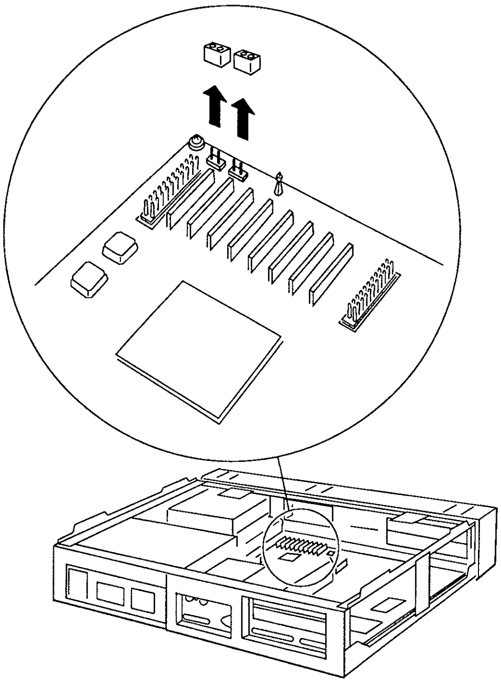
Note

If the SCK-5015 Internal Hard Disk Drive Unit has been installed in the VIW-5000 system, it must be temporarily removed to access the graphics memory expansion connectors. Refer to Chapter 10 "EXPLANATION OF SCK-5015" for details.

12-1-2-3. Mounting

The male-pin connectors for the RAM-13 board are located near the front panel on the SY-143 board.

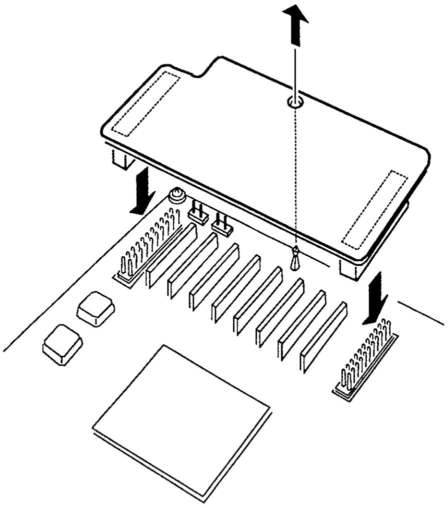
1. Remove the two jumper pins (JP204 and JP205).



Note

Do not lose these jumper pins. Put them in a plastic bag and give them to the user together with Installation Manual. The user may need to reinstall them in the future.

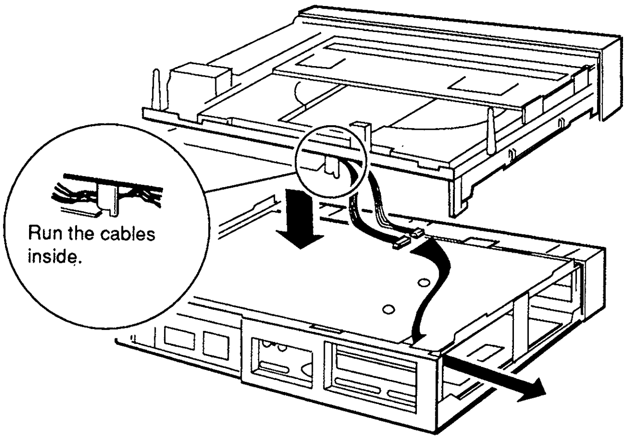
2. Align the SMI-5051's female-pin connectors to the male-pin connectors of the SY-143 board should go into the small hole on the RAM-13 board as shown in the illustration.



3. Lightly push the side edges of the RAM-13 board down until its connectors lock firmly with the SY-143 board connectors.

12-1-2-4. Reinstalling

Follow the instructions provided in Section 12-1-2-2 "Removing" in reverse order.
Be sure to pass the data cables inside the unit.



Tips

When placing the videodisc player part in position, shift it slightly forward and then pull it backward on the computer part. This will make the operation easier.

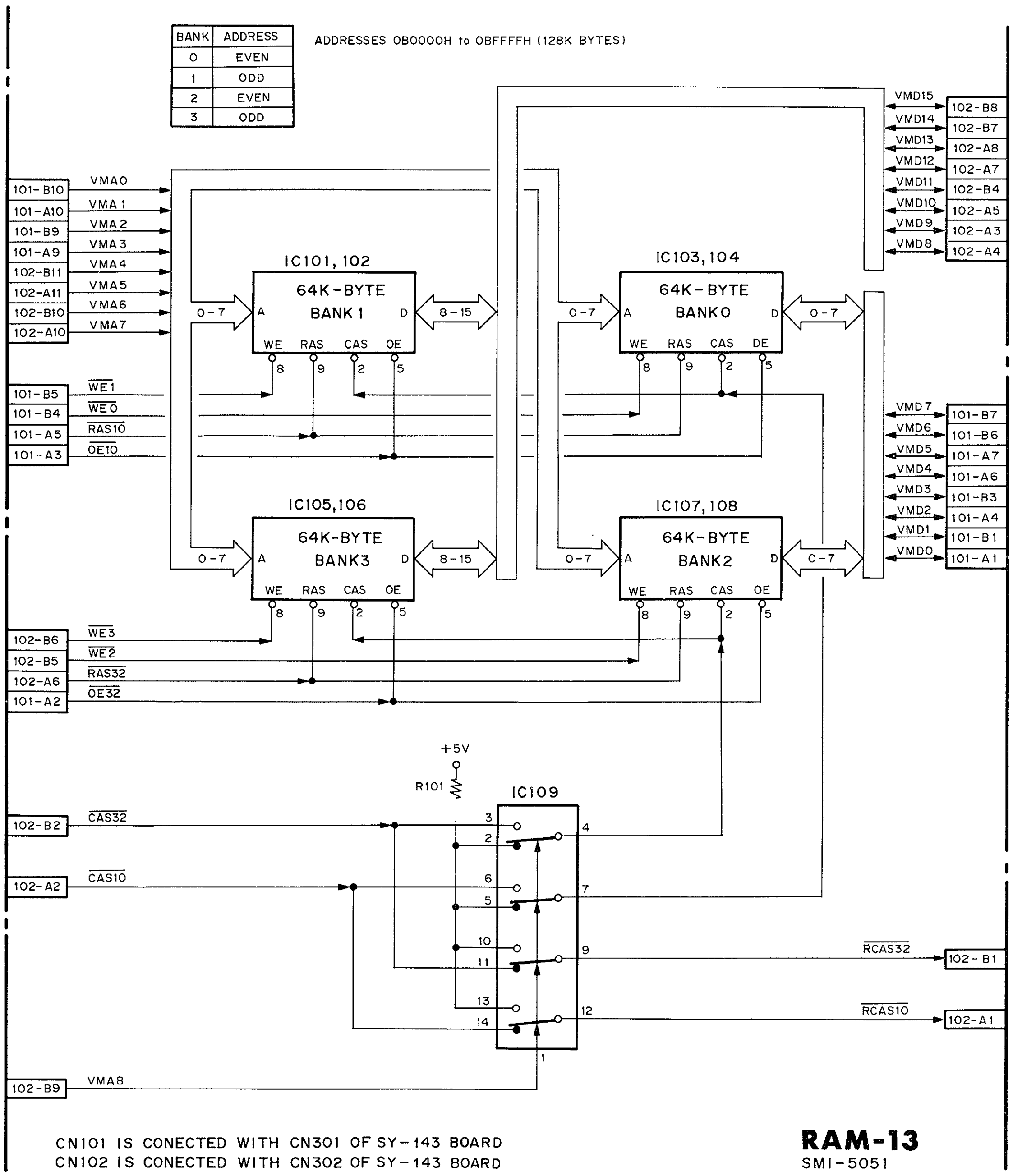
Notes

- Be sure to connect the internal cable before reinstalling the cover assembly.
- Be aware of internal wiring when placing the videodisc player part in position. Take a moment to check that no wires are squeezed under the unit.

12-1-3. Specifications

Graphics memory	256K bytes
Access time	100n sec.
Power requirement	+5V DC ±10%
Current consumption	80 mA typ.
Operating conditions	
Temperature :	+5 to +35℃ (+41 to +95°F)
Humidity :	25 to 85% (at +25℃ or +77°F)
Storage conditions	
Temperature :	−20 to +60℃ (−4 to +140°F)
Dimensions	Approx. 84 × 12 × 54 mm (w/h/d) $\left(3\frac{3}{8}\times\frac{1}{2}\times 2\frac{1}{4}\text{ inches}\right)$
Weight	35 g (1.23 oz.)

12-2. BLOCK DIAGRAM



BANK	ADDRESS
0	EVEN
1	ODD
2	EVEN
3	ODD

ADDRESSES 0B0000H to 0BFFFFH (128K BYTES)

101-B10
VMA0
101-A10
VMA1
101-B9
VMA2
101-A9
VMA3
102-B11
VMA4
102-A11
VMA5
102-B10
VMA6
102-A10
VMA7
IC101, 102
64K-BYTE
BANK 1
A
D
WE RAS CAS OE
8 9 2 5
0-7
8-15
IC103, 104
64K-BYTE
BANK 0
WE RAS CAS DE
0-7
101-B5
WE1
101-B4
WE0
101-A5
RAS10
101-A3
OE10
IC105, 106
64K-BYTE
BANK3
IC107, 108
64K-BYTE
BANK2
102-B6
WE3
102-B5
WE2
102-A6
RAS32
101-A2
OE32
VMD15
102-B8
VMD14
102-B7
VMD13
102-A8
VMD12
102-A7
VMD11
102-B4
VMD10
102-A5
VMD9
102-A3
VMD8
102-A4
VMD7
101-B7
VMD6
101-B6
VMD5
101-A7
VMD4
101-A6
VMD3
101-B3
VMD2
101-A4
VMD1
101-B1
VMD0
101-A1
+5V
R101
IC109
102-B2
CAS32
102-A2
CAS10
3 2 4
6 5 7
10 11 9
13 14 12
1
RCAS32
102-B1
RCAS10
102-A1
102-B9
VMA8

CN101 IS CONECTED WITH CN301 OF SY-143 BOARD
CN102 IS CONECTED WITH CN302 OF SY-143 BOARD

RAM-13
SMI-5051

12-3. SCHEMATIC DIAGRAM

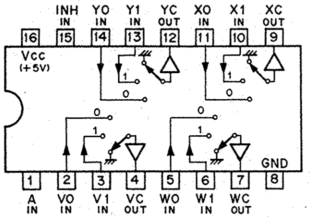
Abbreviations and Units

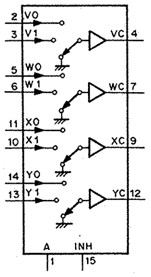
Ref. No.	Description	Unit
C□□	CAPACITOR	μF
CN□□	CONNECTOR	–
IC□□	IC	–
R□□	RESISTOR	Ω

12-3-1. Semiconductor Pin Assignments

74F157APC (FSC)
MC74F157AN (MOTOROLA)

TTL 2-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER
– TOP VIEW –

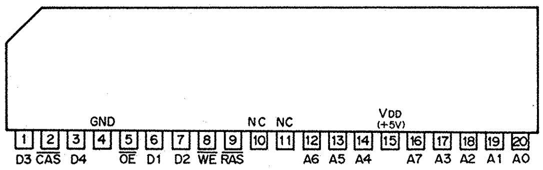

INH IN
Y0 IN
Y1 IN
YC OUT
X0 IN
X1 IN
XC OUT
16
15
14
13
12
11
10
9
Vcc (+5V)
GND
1
2
3
4
5
6
7
8
A IN
V0 IN
V1 IN
VC OUT
W0 IN
W1 IN
WC OUT

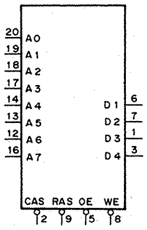

2 V0
3 V1
VC 4
5 W0
6 W1
WC 7
11 X0
10 X1
XC 9
14 Y0
13 Y1
YC 12
A
INH
1
15

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE

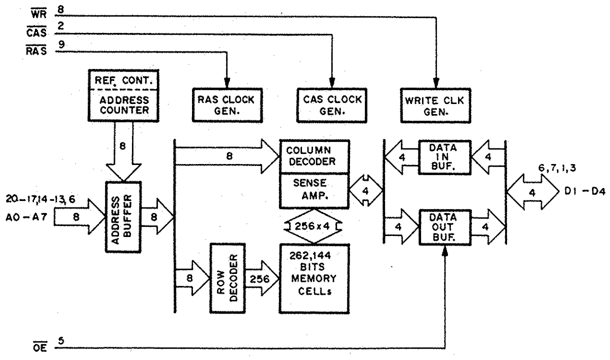
CONT. IN		ON CHANNEL
INH	A	
0	0	0
0	1	1
1	X	GND

MB81464-10PSZ (FUJITSU) (ACCESS TIME = 100nS)
N-MOS 262,144-BIT (65,536x4) DYNAMIC RAM
– SIDE VIEW –

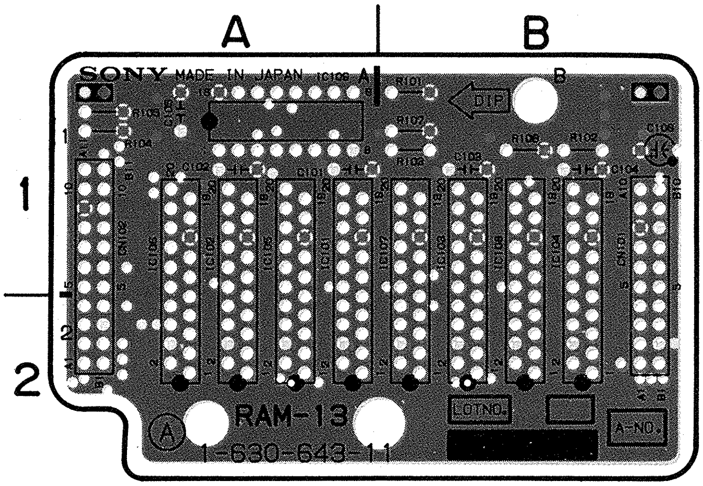

GND
NC
NC
VDD (+5V)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
D3
CAS
D4
OE
D1
D2
WE
RAS
A6
A5
A4
A7
A3
A2
A1
A0


20 A0
19 A1
18 A2
17 A3
14 A4
13 A5
12 A6
16 A7
D1 6
D2 7
D3 1
D4 3
CAS
RAS
OE
WE
2
9
5
8

A0–A7 ; ADDRESS INPUT
$\overline{\text{CAS}}$; COLUMN ADDRESS STROBE
D1–D4 ; DATA IN/OUT
$\overline{\text{OE}}$; OUTPUT ENABLE
$\overline{\text{RAS}}$; ROW ADDRESS STROBE
$\overline{\text{WE}}$; WRITE ENABLE

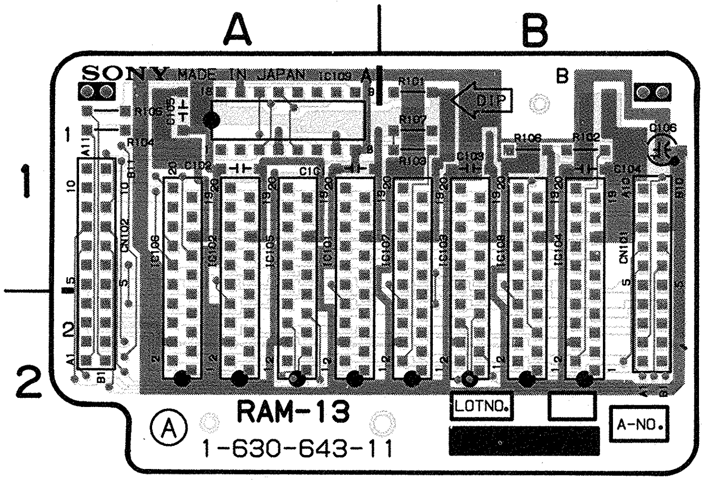

WR 8
CAS 2
RAS 9
REF. CONT.
ADDRESS COUNTER
RAS CLOCK GEN.
CAS CLOCK GEN.
WRITE CLK GEN.
8
COLUMN DECODER
SENSE AMP.
DATA IN BUF.
4
6,7,1,3
D1 – D4
20–17,14–13,6
A0 – A7
ADDRESS BUFFER
256x4
DATA OUT BUF.
ROW DECODER
256
262,144 BITS MEMORY CELLs
OE 5

12-3-2. RAM-13 Board


A
B
1
2
SONY MADE IN JAPAN
DIP
RAM-13
1-630-643-11
LOTNO.
A-NO.
IC106
IC102
IC105
IC101
IC107
IC103
IC108
IC104
CN102
CN101
IC109
R101
R102
R103
R104
R105
R106
C101
C102
C103
C104
C105
C106

RAM-13 – COMPONENT SIDE –

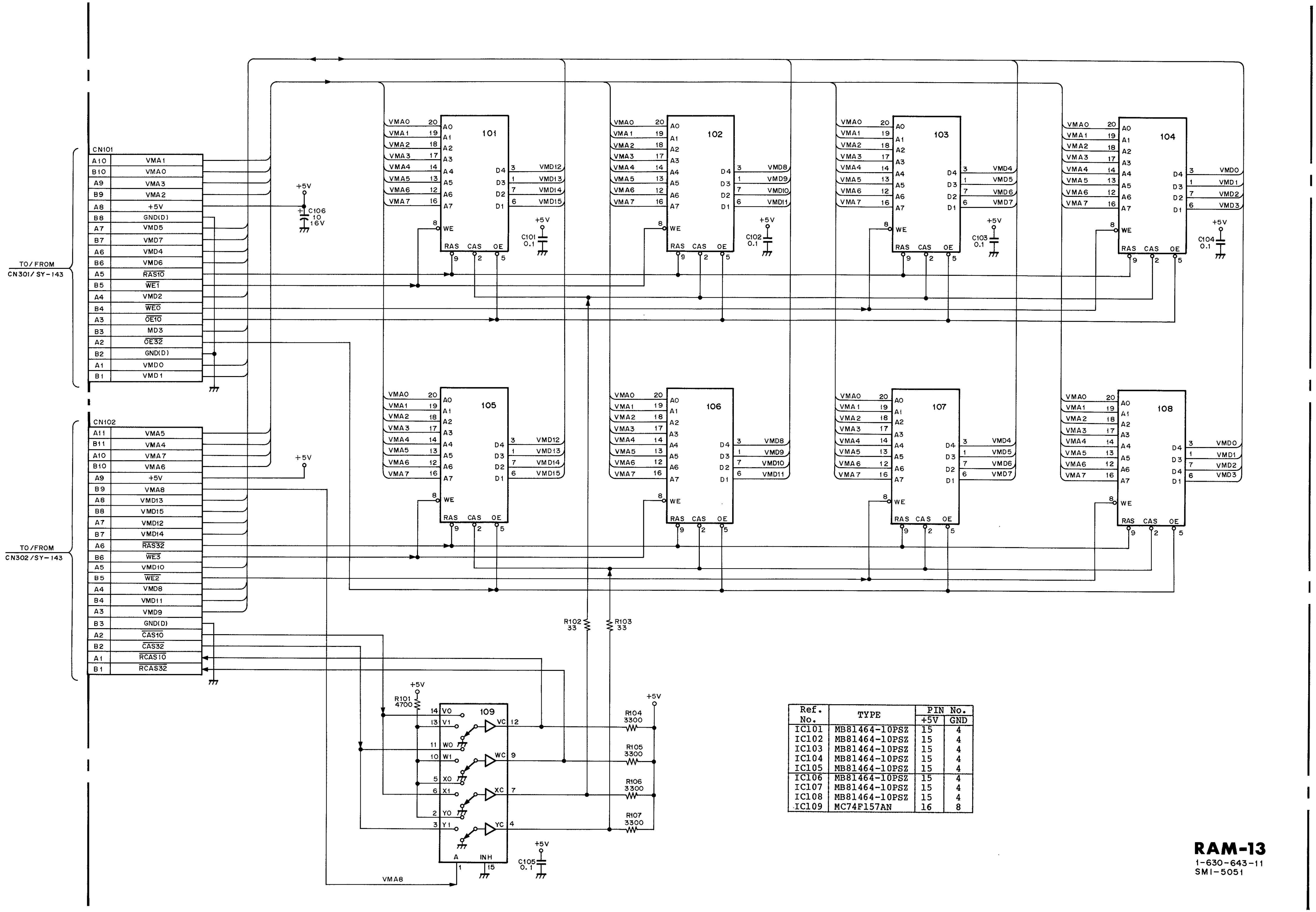
1-630-643-11
SMI-5051


A
B
1
2
SONY MADE IN JAPAN
DIP
RAM-13
1-630-643-11
LOTNO.
A-NO.
IC106
IC102
IC105
IC101
IC107
IC103
IC108
IC104
CN102
CN101
IC109
R101
R102
R103
R104
R105
R106
R107
C101
C102
C103
C104
C105
C106

RAM-13 – COMPONENT SIDE –

1-630-643-11
SMI-5051

C101	A-1	IC101	A-1	R101	B-1
C102	A-1	IC102	A-1	R102	B-1
C103	B-1	IC103	B-1	R103	B-1
C104	B-1	IC104	B-1	R104	A-1
C105	A-1	IC105	A-1	R105	A-1
C106	B-1	IC106	A-1	R106	B-1
		IC107	B-1	R107	B-1
CN101	B-1	IC108	B-1		
CN102	A-1	IC109	A-1		


CN101
A10 VMA1
B10 VMA0
A9 VMA3
B9 VMA2
A8 +5V
B8 GND(D)
A7 VMD5
B7 VMD7
A6 VMD4
B6 VMD6
A5 RAS10
B5 WE1
A4 VMD2
B4 WE0
A3 OE10
B3 MD3
A2 OE32
B2 GND(D)
A1 VMD0
B1 VMD1
TO/FROM CN301/SY-143
CN102
A11 VMA5
B11 VMA4
A10 VMA7
B10 VMA6
A9 +5V
B9 VMA8
A8 VMD13
B8 VMD15
A7 VMD12
B7 VMD14
A6 RAS32
B6 WE3
A5 VMD10
B5 WE2
A4 VMD8
B4 VMD11
A3 VMD9
B3 GND(D)
A2 CAS10
B2 CAS32
A1 RCAS10
B1 RCAS32
TO/FROM CN302/SY-143
+5V
C106 10 16V
101
102
103
104
105
106
107
108
VMA0 20 A0
VMA1 19 A1
VMA2 18 A2
VMA3 17 A3
VMA4 14 A4
VMA5 13 A5
VMA6 12 A6
VMA7 16 A7
8 WE
RAS CAS OE
9 2 5
D4 D3 D2 D1
VMD12 VMD13 VMD14 VMD15
VMD8 VMD9 VMD10 VMD11
VMD4 VMD5 VMD6 VMD7
VMD0 VMD1 VMD2 VMD3
C101 0.1
C102 0.1
C103 0.1
C104 0.1
R102 33
R103 33
109
R101 4700
14 V0
13 V1
11 W0
10 W1
5 X0
6 X1
2 Y0
3 Y1
VC 12
WC 9
XC 7
YC 4
A 1
INH 15
VMA8
R104 3300
R105 3300
R106 3300
R107 3300
C105 0.1

Ref. No.	TYPE	PIN No.	
		+5V	GND
IC101	MB81464-10PSZ	15	4
IC102	MB81464-10PSZ	15	4
IC103	MB81464-10PSZ	15	4
IC104	MB81464-10PSZ	15	4
IC105	MB81464-10PSZ	15	4
IC106	MB81464-10PSZ	15	4
IC107	MB81464-10PSZ	15	4
IC108	MB81464-10PSZ	15	4
IC109	MC74F157AN	16	8

RAM-13
1-630-643-11
SMI-5051

12-4. REPAIR PARTS

12-4-1. RAM-13 Board

Ref. No.	Parts No.	Description
	3-531-675-01	RIVET
C101 – 105	1-164-159-11	CERAMIC 0.1 50V
C106	1-126-157-11	ELECT 10 20% 16V
CN101	*1-568-499-11	HOUSING, 20P
CN102	*1-568-500-11	HOUSING, 22P
IC101 – 108	8-759-944-61	MB81464-10PSZ
IC109	8-759-938-93	74F157APC
R101	1-249-425-11	CARBON 4.7K 5% 1/4W
R102, 103	1-249-399-11	CARBON 33 5% 1/4W
R104 – 107	1-249-423-11	CARBON 3.3K 5% 1/4W

Note

Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.

Abbreviations and Units

Ref. No.	Description	Unit
C□□	CAPACITOR	μF
CN□□	CONNECTOR	–
IC□□	IC	–
R□□	RESISTOR	Ω

VIW-5000 (UC)

9-972-805-11

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Home Video Group

English
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VIW-5000

SERVICE MANUAL

SUPPLEMENT-1

This supplement-1 is added SELF-DIAGNOSTICS, TROUBLESHOOTING and ADJUSTMENT.
Refer to the service manual for OPERATION, SERVICE INFORMATION, SCHEMATIC DIAGRAM and REPAIR PARTS AND FIXTURES.

Sony VIEW System

SONY®

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CHAPTER 6
SELF-DIAGNOSTICS

The self-diagnostic can be performed by means of the system ROM setup program or with the SMW-5001 (VIEW/VGA operating system package) diagnostic program.

6-1. SELF-DIAGNOSTIC PERFORMED WITH THE SETUP PROGRAM

6-1-1. Setup Program In the System ROM

When you first start the system after purchase or after you change the hardware configuration, you must set up the system using the Installation Program included in the SMW-5001 VIEW/VGA Operating System Package.
However, when you want to change the configuration for the keyboard to "not installed," for example when you do not need the keyboard for a VIEW system as the keyboard is not used for demonstration, or when you want to change the CPU clock frequency as the optional board requires, you must use the setup program in the system ROM. The procedure is described below.

1. Turn on the power of the system.

2. When the message "Strike the F1 key to continue, F2 to run the setup utility" appears on the screen, press the F2 key.
   When the MS-DOS has started, press the Ctrl, Alt and Esc keys simultaneously.
   The setup program will start.

3. Select the item to be set using the ↓ or ↑ key and then select the setting using the → or ← key.

4. After you have changed the setting, press the Esc key.
   The system will restart with the new setting.

Notes:

- In step 3, the following items also appear and they can be changed. However, as they have already been set properly by using the SMW-5001 installation program, do not change their setting.

Diskette A:	3.5 inch, 1.44 MB
Diskette B:	Note Installed
Hard disk drive 1:	Type 17 when the SCK-5015 is installed or Not Installed
Hard disk drive 2:	Not Installed
Base memory size:	640 Kbytes
Extended memory size:	Specify the size or Not Installed 2048 Kbytes when the SMI-5050 is installed.
Display	VGA/EGA
Coprocessor	"Not Installed" will be displayed.

- When an item is selected and you press the F1 key, the explanation for that item will be displayed on the screen.
- You can temporarily change the CPU clock frequency by pressing the Ctrl + Alt + ↑ or ↓.
- The setup program in the system ROM may not be started when the TSR (Terminate and Stay Resident) program which is started by pressing the Ctrl, Alt or Esc is in the memory.

6-1-2. Self-diagnostic Performed with the Setup Program

During or after the power-on process, an error or an informational message may be displayed on the screen. The messages and how to correct the error are as shown below.

6-1-2-1. Setup trouble messages

When one of the following messages is displayed, set the correct configuration information executing the "Set SETUP RAM" of the Installation Program included in SMW-5001.

Message	Possible Cause	Solution
Diskette configuration error	The specified configuration is not supported	Rerun the SETUP program and change the configuration.
Errors found disk X: Failed initialization	Hard disk configuration information is incorrect.	Rerun the SETUP program and enter correct hard disk information.
Errors found Incorrect configuration information memory size miscompare	The size of base or expansion memory does not agree with configuration information.	Rerun the SETUP program and enter correct memory size.
Hard disk configuration error	The specified configuration is not supported.	Correct the hard disk configuration.
Invalid configuration information — please run SETUP program	• Memory size is incorrect. • Display adapter is configured incorrectly. • Wrong number of diskette drives.	Run the SETUP program.
Time-of-day clock stopped	The Time-of-day clock chip has failed.	Run the SETUP program.
Time-of-day not set — please run SETUP program	Clock not set.	Run the SETUP program.

6-1-2-2. Hardware trouble messages

When one of the following messages is displayed, turn off the unit and turn it on again. If the error message is displayed again, there is hardware trouble.

Message	Possible Cause	Solution
Diskette drive reset failed	The diskette drive has failed	Check the diskette drive.
Diskette drive 0 seek failure	The A: drive has either failed or is missing.	Check the A: drive.
Display adapter failed; using alternate	• The graphic control block failed.	• Check the graphic control block.
Gate A20 failure	Protected mode cannot be enabled.	Check the system control block.
Hard disk failure	Bad disk	Retry boot. If that doesn't work, replace the hard disk.
Hard disk read failure — strike F1 to retry boot	The hard disk is defective.	Retry boot. If that doesn't work, replace the hard disk.
Keyboard clock line failure *	Either the keyboard or the keyboard cable connection is defective.	Make sure the keyboard cable and keyboard are connected properly.
Keyboard data line failure *		
Keyboard controller failure *	The keyboard controller firmware has failed.	Check the keyboard controller.
Keyboard stuck key failure *	A key (s) is jammed.	Try pressing the key (s) again.

Message	**Possible Cause**	**Solution**
Memory address line failure at *hex-value*, read *hex-value*, expecting *hex-value*	Circuitry associated with the memory chips has failed.	Check the circuitry.
Memory data line, failure at *hex-value*, read *hex-value*, *hex-value*	One of the memory chips or associated circuitry has failed.	Replace the memory chips.
Memory high address line failure at *hex-value*, read *hex-value*, expecting *hex-value*	Circuitry associated with the memory chips has failed.	Check the circuitry.
Memory double word logic failure at *hex-value*, read *hex-value*, expecting *hex-value*	Memory chip circuitry failed.	Replace the memory chip.
Memory odd/even logic failure at *hex-value*, read *hex-value*, expecting *hex-value*	Circuitry associated with the memory chips has failed.	Check the circuitry.
Memory parity failure at *hex-value*, read *hex-value*, expecting *hex-value*	One of the parity memory chips has failed.	Try replacing the memory chips.
Memory write/read failure at *hex-value*, read *hex-value*, expecting *hex-value*	One of the memory chips has failed.	Try replacing the memory chips.
Not timer tick interrupt	The timer chip has failed.	Check the timer chip on the system board.
Hex-value optional ROM bad checksum=*hex-value*	The peripheral card contains a defective ROM.	Replace the peripheral card.
Shutdown failure	The keyboard controller or its associated logic has failed.	Check the keyboard controller.
Timer chip counter 2 failed	Chip failed.	Check the timer chip system board.
Timer or interrupt controlled bad	Either the timer chip or the interrupt controller is defective.	Check the timer chip or the interrupt controller on the system board.
Unexpected interrupt in protected mode	The non-maskable interrupt (NMI) port can't be disable.	Check the system board, particularly the logic associated with the non-maskable interrupt.

* One of these messages may be displayed when you press a key on the keyboard during the system start-up procedure.

6-1-2-3. Other message

Message	Possible Cause	Solution
Diskette drive 1 seek failure.	The configuration information is incorrect.	Run the SETUP program. At "Diskette B:", select "Not installed".
Diskette read failure strive F1 to retry boot.	The diskette is either not formatted or defective.	Replace the diskette with a bootable diskette and retry boot.
Hard disk controller failure	• Hard disk configuration information is incorrect. • The controller circuitry has failed.	• Rerun the SETUP program and enter correct hard disc information. • Check the circuitry.
No boot device available — strike F1 to retry boot	Either diskette drive A:, the hard disk, or the diskette itself is defective.	Retry boot. If that doesn't work, replace the floppy diskette or the hard disk.
No boot sector on hard disk — strike F1 to retry boot	The C: drive is not formatted or is not bootable.	Format the C: drive, make it bootable.
Not a boot diskette — strike F1 to retry boot	The diskette in drive A: is not formatted as a bootable diskette.	Replace the diskette with a bootable diskette and retry boot.
I/O card parity interrupt at *address*. Type (S) hut off NMI, (R) boot, other keys to continue	The peripheral card has failed.	Type (S) hut off NMI. Note: This will only temporarily allow you to continue. You must replace the peripheral card.
Memory parity interrupt at *address*. Type (S) hut off NMI, (R) boot, other keys to continue	A memory chip (s) has failed.	Type (s) hut off NMI. Note: This will only temporarily allow you to continue. You must replace the memory chip (s).

6-1-2-4. Informational message

The following are the message that provide information and require no action.

- *Hex-value* Base Memory
  Shows the size of the base memory that was tested successfully.

- *Hex-value* Extended Memory
  Shows the size of extended memory that was tested successfully.

- Decreasing available memory
  Displayed immediately after an error message, indicating that the memory chips failed. Refer to the solution for that error message.

- Memory tests terminated by keystroke
  Indicates that you have pressed the spacebar during the memory tests and have stopped the memory tests.

- Strike the F1 key to continue
  Indicates that an error was detected during the self-test diagnostics. Press the F1 key to attempt to boot.

6-2. SELF-DIAGNOSTIC PERFORMED WITH THE SMW-5001

SMW-5001 includes a diagnostics program which helps check the functions of the VIW-5000 hardware and its peripheral devices. Run this program whenever you encounter a problem with the VIW-5000 hardware (including its boards, videodisc player and monitor).
Using this program permits minute checking compared with the system start-up ROM diagnostics or the install program's diagnostics.

Functions of the diagnostics program are divided into three groups as follows:
- Board level diagnostics
- Video/monitor diagnostics
- Peripheral diagnostics

The diagnostics program features the following menu structure:

1. Board Level Diagnostics
   - 1.1 System
     - 1.1.1 Once
     - 1.1.2 Multiple times
   - 1.2 Display
     - 1.2.1 Once
     - 1.2.2 Multiple times
   - 1.3 Extended Memory
     - 1.3.1 Once
     - 1.3.2 Multiple times
   - 1.4 Expanded Memory
     - 1.4.1 Once
     - 1.4.2 Multiple times

2. Video/Monitor Diagnostics
   - 2.1 Automatic Mode
   - 2.2 Manual Mode

3. Peripheral Diagnostics
   - 3.1 Floppydisk Drive Read
   - 3.2 Harddisk Drive Read
   - 3.3 Printer
   - 3.4 Keyboard
   - 3.5 Mouse/RS-232C
     - 3.5.1 Using RS-232C (1)
     - 3.5.2 Using RS-232C (3)
     - 3.5.3 Using RS-232C (4)
   - 3.6 Videodisc Player

Note:

The devices indicated with an asterisk on the screen during diagnostics are optional equipment. These devices cannot be tested unless they are actually installed.

6-2-1. Getting Started with the Diagnostics Program

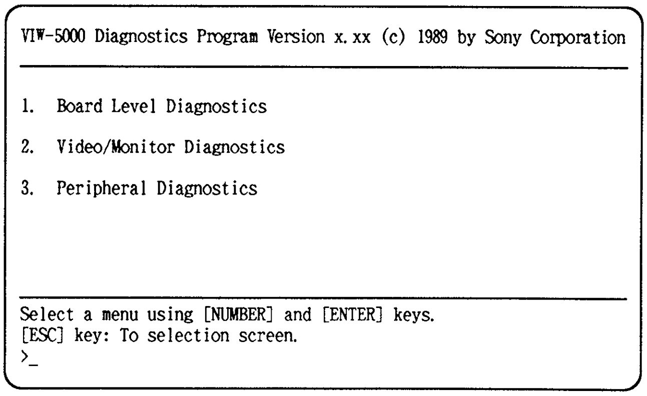
1. Start up MS-DOS.
   Insert the SMW-5001 VIEW/VGA Operating System Package's backup disk into the floppydisk drive and turn on the power. MS-DOS boots from the floppydisk.

When the installation program is started, select "Exit to MS-DOS".

2. When the MS-DOS prompt, A>, is displayed, type "CD\DIAG" (either uppercase or lowercase) and press Enter to change the current directory.

3. Type "DIAG" and press Enter to start the diagnostics program.

The following main menu will be displayed:



```
VIW-5000 Diagnostics Program Version x.xx (c) 1989 by Sony Corporation
------------------------------------------------------------------------
1.  Board Level Diagnostics

2.  Video/Monitor Diagnostics

3.  Peripheral Diagnostics



------------------------------------------------------------------------
Select a menu using [NUMBER] and [ENTER] keys.
[ESC] key: To selection screen.
>_
```

To quit diagnostics program

Press Esc in the main menu displayed at the above step 3. The system will be restarted.

If an error message is displayed and the system does not start

The system ROM diagnostics program has probably detected a hardware problem. Refer to the VIW-5000's operating instructions and follow the instructions provided there.

Notes

- Once the diagnostics program is started, ending the program always restarts the system. There is no way to quit the session without restarting the system.
- To execute the diagnostic item 1.4 "Expanded Memory", the MM.SYS EMS device driver must be installed in your CONFIG.SYS. For details on the CONFIG.SYS file and device driver, refer to Chapter 3 of the SMW-5001 instruction manual.
- Diagnostics-related files other than the DIAG.COM file are hidden. These files cannot be displayed on the screen using MS-DOS's "DIR" command.

6-2-2. Board Level Diagnostics

Items tested in the board level diagnostics are as follows:

System

- CPU 80286
- Timer, interrupt controller
- Printer interface
- RS-232C chip
- Address gate A20
- Shutdown function
- Harddisk controller
- Main memory

Display

- Video RAM
- Color register
- Palette RAM
- Transparent color
- I/O addresses

Extended memory

Whether the memory area increased by the optional SMI-5050 Memory Expansion can be used as "extended" memory.

Expanded memory

Whether the memory area increased by the optional SMI-5050 Memory Expansion can be used as "expanded" memory.

Notes

- Disconnect the equipment connected to the VIW-5000's RS-232C connector before you perform the system board diagnostics.
- During the display board diagnostics, the screen may flicker. This is a part of the test procedure and is not a system malfunction.
- The diagnostics program tests the extended memory and expanded memory only for the sizes specified by in SETUP RAM.

6-2-2-1. Operation

1. Type "1" (for "Board Level Diagnostics") at the main menu and press Enter.

2. Type the sub-digit of the menu item and press Enter. For example, type "1" to test the system board and press Enter.

   Type "1" to test only once or "2" to repeat the test. Then press Enter.

3. The multiple times diagnostics has 10-second intervals between each test. When the "C" key is pressed during the interval, the next test starts immediately regardless of the time elapsed since the previous test.
   To stop the test, press Esc.

   The test starts. Test items are displayed on the screen.
   When the test has been successfully completed, "OK" appears for each item.
   If an error is detected, "NG" is displayed. In that case, exit from this diagnostics program and turn off the power. Then start the diagnostics program and repeat the test. If the same error persists, contact your authorized Sony representative for assistance.

4. Press Esc to return to the submenu (1.1 screen).

Note

Press Esc to return to the pervious higher menu level in the hierarchy structure. For example, if Esc is pressed at the menu 1-1, the menu 1 (1. Board Level Diagnostics) reappears.

6-2-3. Video/Monitor Diagnostics

Items tested in the video/monitor diagnostics are as follows:

Display mode

In the Automatic mode, screens are displayed one by one.
In the Manual mode, you can test the display mode according to the screen instructions using the following keys:

N/P keys	Next/Previous screen
G key	Sets Genlock mode (automatic or internal).
S key	Sets superimposing mode (computer graphics only, superimpose, or video image only).
T key	Sets transparent color mode (single or multiple transparent color).
↑ ↓ ← → and Enter keys	Select a color palette using the cursor keys, and press Enter to set/remove it as the transparent color. Pressing Enter acts as a toggle switch to turn on/off the transparent color.
Esc key	Ends the test.

Note

Select a video image using the "3-6 Videodisc Player" menu for superimposing with the computer graphics.

6-2-4. Peripheral Diagnostics

Tests performed in the peripheral diagnostics are as follows:

Floppydisk drive read

Performs the read test. You will be asked to replace the backup disk with another disk for this test. When the test is completed, be sure to reinstall the backup disk in the floppydisk drive.

Harddisk drive read

Performs the read test.

Printer

Tests the printer by printing alphanumeric characters.

Keyboard

Displays the characters associated with each key on the keyboard. Press a key and see whether the corresponding character is displayed.

Mouse/RS-232C

Tests the mouse (SMI-3062) and RS-232C interface when the mouse is connected to the VIW-5000's RS-232C connector. To check the COM ports (RS-232C) 3 and 4, use the SMI-3031 Dual RS-232C Board.

Videodisc player

Tests the videodisc player performance. Refer to the Remote controller commands.

Note

Errors detected during the floppydisk drive read test may be attributable to damage on the floppydisk being used. To determine the cause of the error, repeat the test using another floppydisk.

6-2-4-1. Operation

Type "3" (for "Peripheral Diagnostics") at the main menu and press Enter.
The following submenu will be displayed.

1. Type the sub-digit of the menu item and press Enter. For example, type "5" to test the mouse/RS-232C and press Enter.

2. Enter the item number and press Enter.

Follow the instructions on the screen for the rest of the operation.

3. Press Esc to quit the test.

Note

To quit the keyboard diagnostics, press Esc followed by Enter.

6-2-5. Remote Controller Commands

In the simulated remote controller, the following keys may be used to control the videodisc player.

Key	Functions
C	Clears videodisc player status.
H	Switches audio channels 1 and 2. (CH-1, CH-2)=(ON, ON) → (ON, OFF) → (OFF, ON) → (OFF, OFF) → (ON, ON)...
I	Switches index on/off.
M	Changes access mode. Frame number mode ↔ Chapter number mode
R	Performs repeat play from current frame to specified frame with specified times or within a specified chapter.
S	Performs frame or chapter search for the specified number.
Enter	For repeat play operation, sets the frame number, chapter number and repeat count. For search operation, sets the frame number and chapter number.
Space	Performs still.
F1/F2	Performs reverse/forward scan.
F3/F4	Performs reverse/forward fast play.
F5/F6	Performs reverse/forward step and still.
F7/F8	Performs reverse/forward play.
Up/Down Arrow key	Changes current mode. — (PLAY) — (STILL/STEP) — (FAST) — (SCAN) —
Left/Right Arrow key	Reverse/forward with current mode.
Esc	Turns commander on/off.
Ctrl+Up/Down Ctrl+Left/Right	Moves commander's position.
Q	Ends process.

When you select a certain command using the corresponding key (such as "S" for search and "R" for repeat play), an appropriate dialogue will appear on the screen for you to specify various values including a frame number and chapter.

How to quit

To quit this program, press the "Q" key. The system returns to the menu 3-6.

CHAPTER 7
TROUBLESHOOTING

7-1. OUTLINE

Causes can almost be limited by a trouble condition or its occurrence situation, and by self-diagnosis of the system ROM. Each boards checking, however, is needed because it is difficult to restrict causes within a board.

7-1-1. Procedure

*1. Power supply checking
(SW Reg. power supply line)
↓
*2. Abnormal board checking

*1. Confirm whether the switching regulator or the power supply line are normal or not. (Refer to section 7-2.)
*2. Check the corresponding sections following the section 7-3.

7-1-2. Attentions

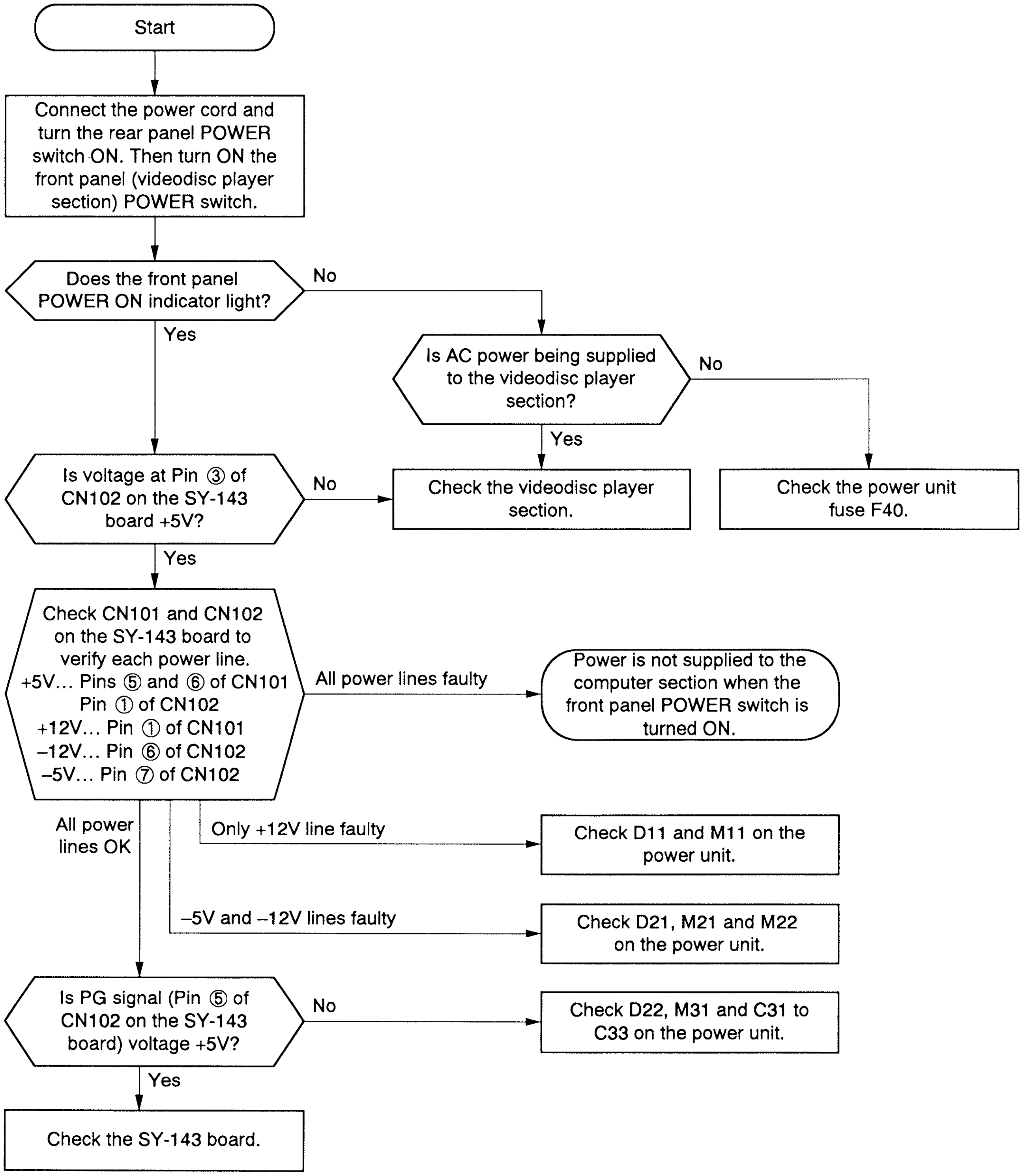
Be sure to check the following items previously; servicing for maintenance or improvement has been done properly, setting of jumpers or switches has been done correctly, boards or mechanism parts are free from remarkable deformity or damage, pin of sockets or connectors is free from deformity or short-circuit, etc.
Also, as for usage or operation of each devices, refer to the data sheets (data book) or user's manuals released from respective manufacturers. When servicing, refer to circuit diagrams, block diagrams and circuit descriptions.

7-2. POWER SUPPLY UNIT

Check the power supply line around the switching regulator. When the unit does not work, the switching regulator or its feeding lines is considered to be troubled.
Perform the checking in 7-2 page.

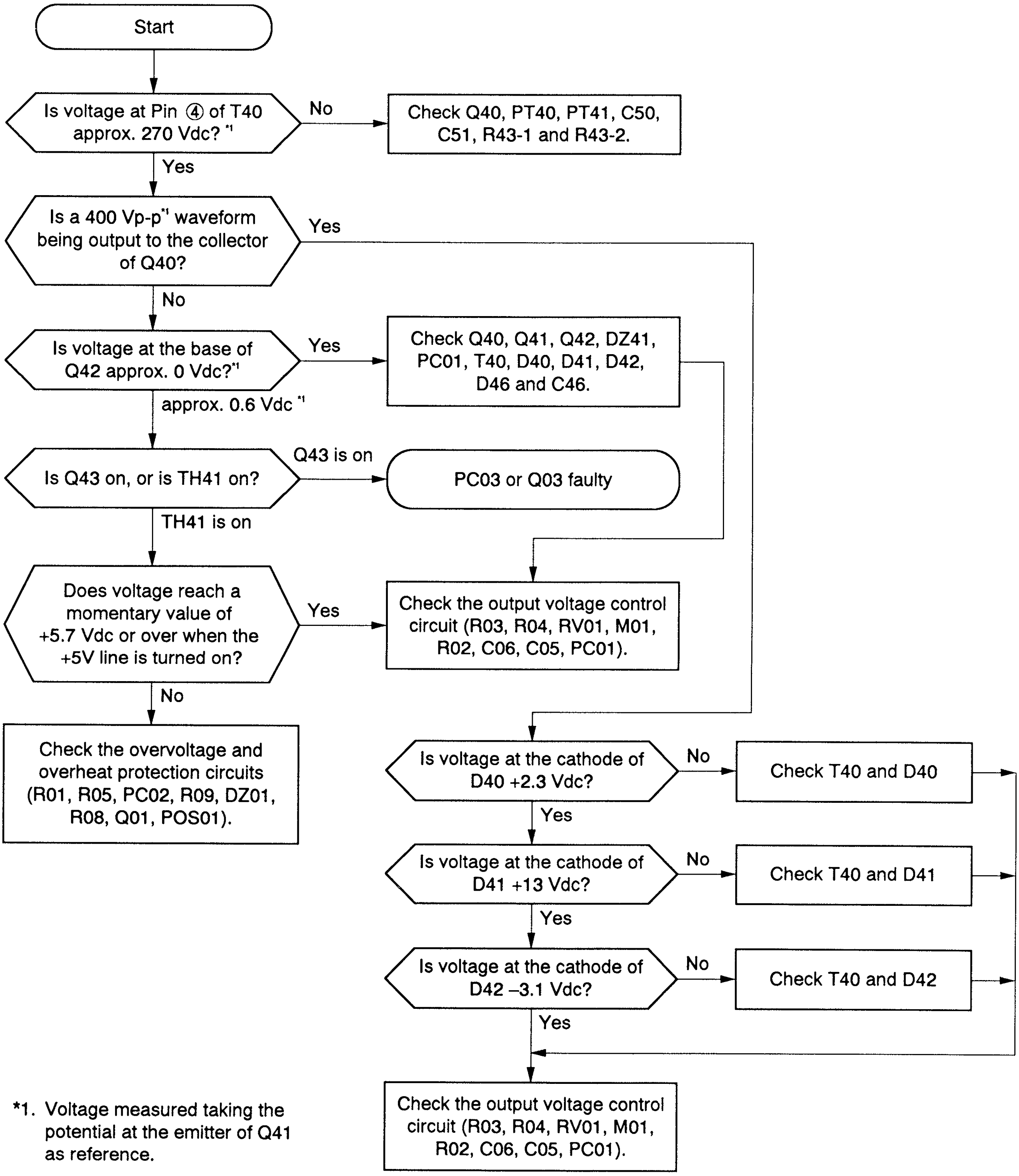
Connector Pin No.	Voltage (V)	
	SY-143 BOARD CN101	SY-143 BOARD CN102
1	+5	+5
2	+5	0
3	0	+5
4	0	0
5	0	+5
6	+12	0
7		−12
8		−5

Table 7-1.


Start
Connect the power cord and turn the rear panel POWER switch ON. Then turn ON the front panel (videodisc player section) POWER switch.
Does the front panel POWER ON indicator light?
No
Yes
Is AC power being supplied to the videodisc player section?
No
Yes
Is voltage at Pin ③ of CN102 on the SY-143 board +5V?
No
Check the videodisc player section.
Check the power unit fuse F40.
Yes
Check CN101 and CN102 on the SY-143 board to verify each power line.
+5V... Pins ⑤ and ⑥ of CN101
Pin ① of CN102
+12V... Pin ① of CN101
–12V... Pin ⑥ of CN102
–5V... Pin ⑦ of CN102
All power lines faulty
Power is not supplied to the computer section when the front panel POWER switch is turned ON.
All power lines OK
Only +12V line faulty
Check D11 and M11 on the power unit.
–5V and –12V lines faulty
Check D21, M21 and M22 on the power unit.
Is PG signal (Pin ⑤ of CN102 on the SY-143 board) voltage +5V?
No
Check D22, M31 and C31 to C33 on the power unit.
Yes
Check the SY-143 board.

7-2-1. Power Is Not Supplied to the Computer Section When the Front Panel (Videodisc Player Section) POWER Switch Is Turned ON.

Check the following on the power unit.

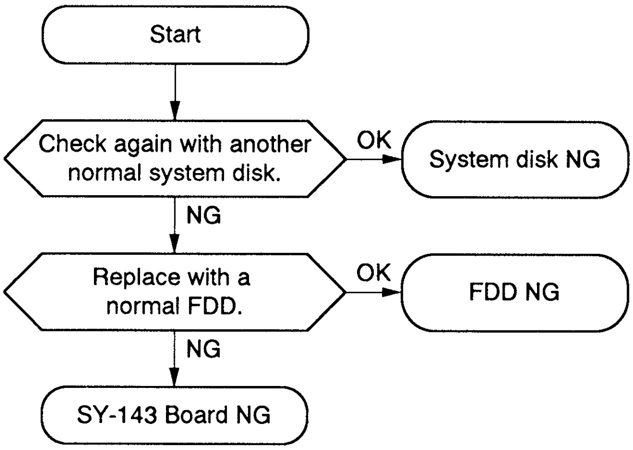

Start
Is voltage at Pin ④ of T40 approx. 270 Vdc? *1
No
Check Q40, PT40, PT41, C50, C51, R43-1 and R43-2.
Yes
Is a 400 Vp-p*1 waveform being output to the collector of Q40?
Yes
No
Is voltage at the base of Q42 approx. 0 Vdc?*1
Yes
Check Q40, Q41, Q42, DZ41, PC01, T40, D40, D41, D42, D46 and C46.
approx. 0.6 Vdc *1
Is Q43 on, or is TH41 on?
Q43 is on
PC03 or Q03 faulty
TH41 is on
Does voltage reach a momentary value of +5.7 Vdc or over when the +5V line is turned on?
Yes
Check the output voltage control circuit (R03, R04, RV01, M01, R02, C06, C05, PC01).
No
Check the overvoltage and overheat protection circuits (R01, R05, PC02, R09, DZ01, R08, Q01, POS01).
Is voltage at the cathode of D40 +2.3 Vdc?
No
Check T40 and D40
Yes
Is voltage at the cathode of D41 +13 Vdc?
No
Check T40 and D41
Yes
Is voltage at the cathode of D42 –3.1 Vdc?
No
Check T40 and D42
Yes
Check the output voltage control circuit (R03, R04, RV01, M01, R02, C06, C05, PC01).

*1. Voltage measured taking the potential at the emitter of Q41 as reference.

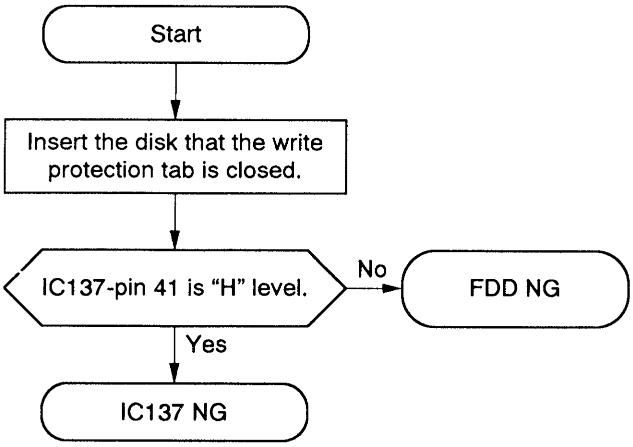
7-3. SY-143 BOARD (SYSTEM BOARD)

7-3-1. Floppydisk Control Circuit

1) When the system disk will not start, and the message "Diskette read failure-strike F1 key to retry boot." is displayed;
   Point: The system disk or FDD is considered to be troubled.


Start
Check again with another normal system disk.
OK
System disk NG
NG
Replace with a normal FDD.
OK
FDD NG
NG
SY-143 Board NG

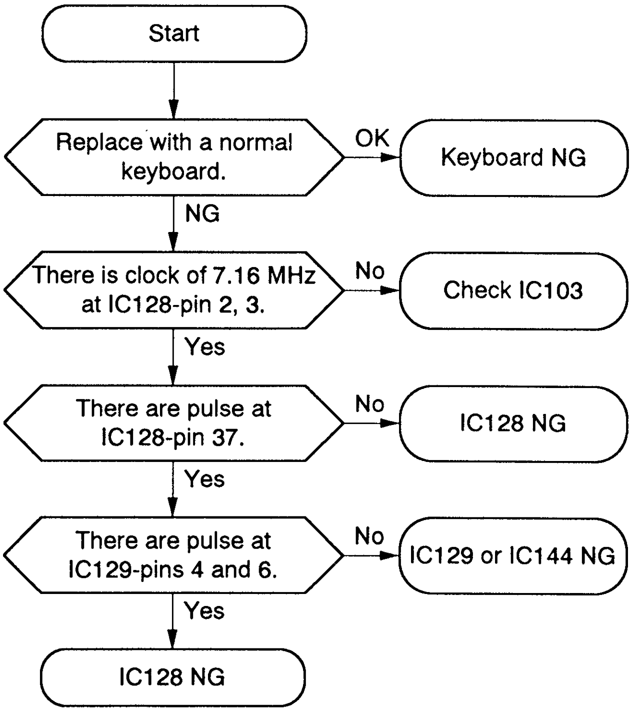
2) The write protection error is occurred without the write protection;
   Point: FDD or the write protection signal system is considered to be troubled.


Start
Insert the disk that the write protection tab is closed.
IC137-pin 41 is "H" level.
No
FDD NG
Yes
IC137 NG

7-3-2. Keyboard Control Circuit

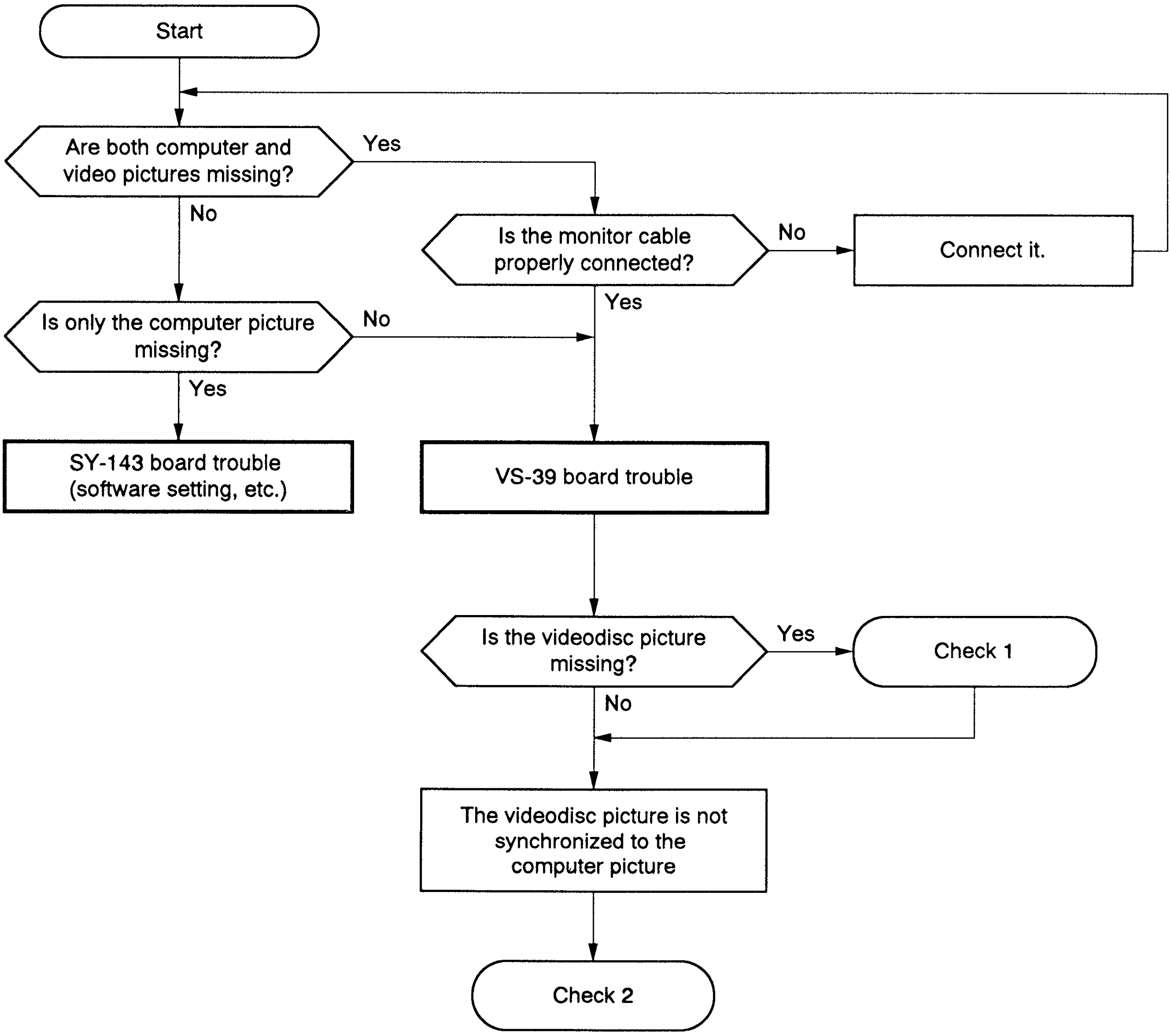
7-3-2-1. When the keyboard is abnormal

Observation of the various signals is mode after applying a RESET.

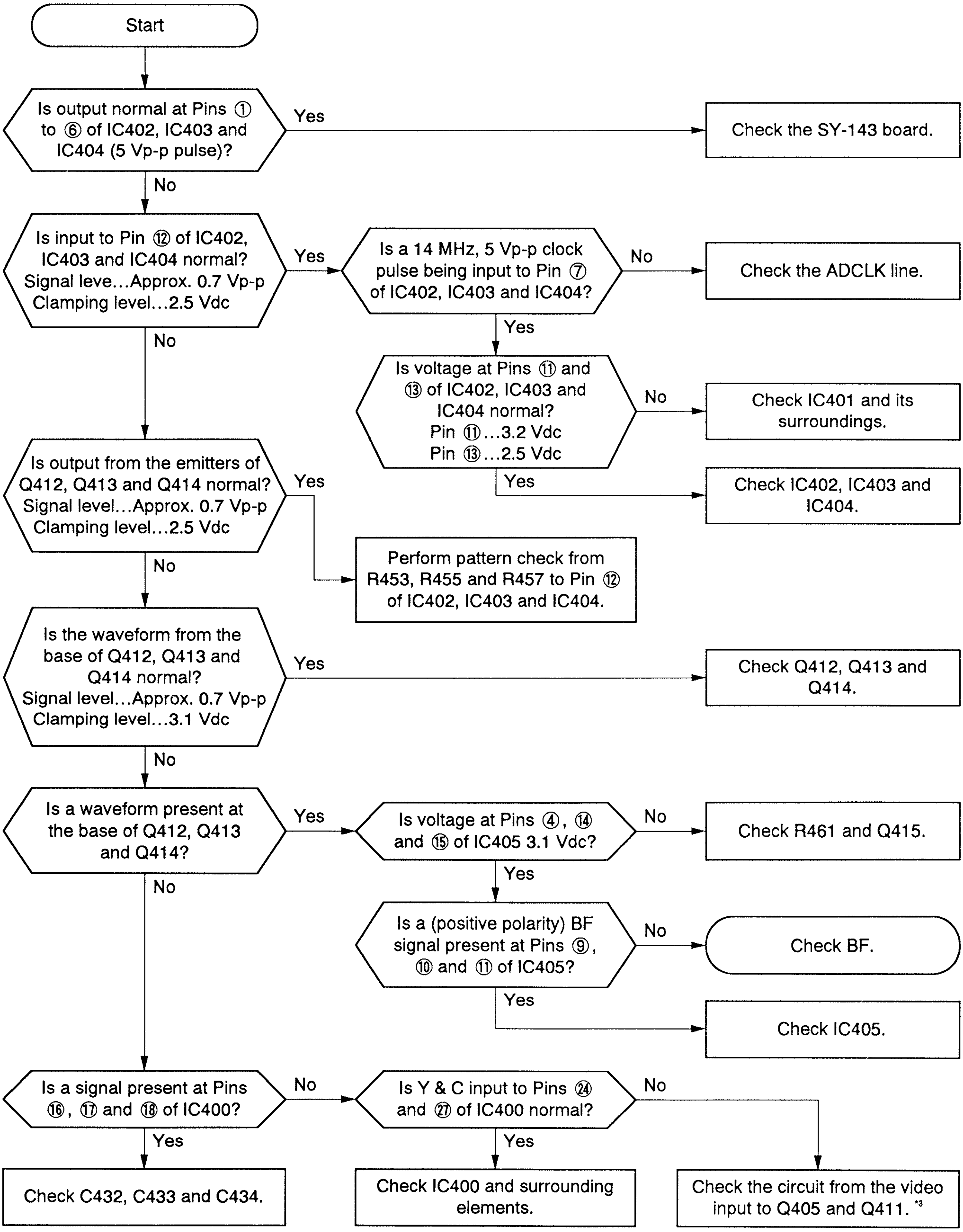

Start
Replace with a normal keyboard.
OK
Keyboard NG
NG
There is clock of 7.16 MHz at IC128-pin 2, 3.
No
Check IC103
Yes
There are pulse at IC128-pin 37.
No
IC128 NG
Yes
There are pulse at IC129-pins 4 and 6.
No
IC129 or IC144 NG
Yes
IC128 NG

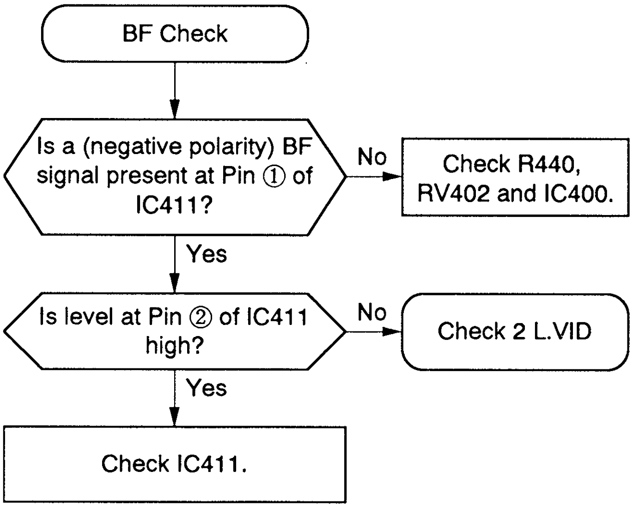
7-4. VS-39 BOARD

7-4-1. No Superimpose

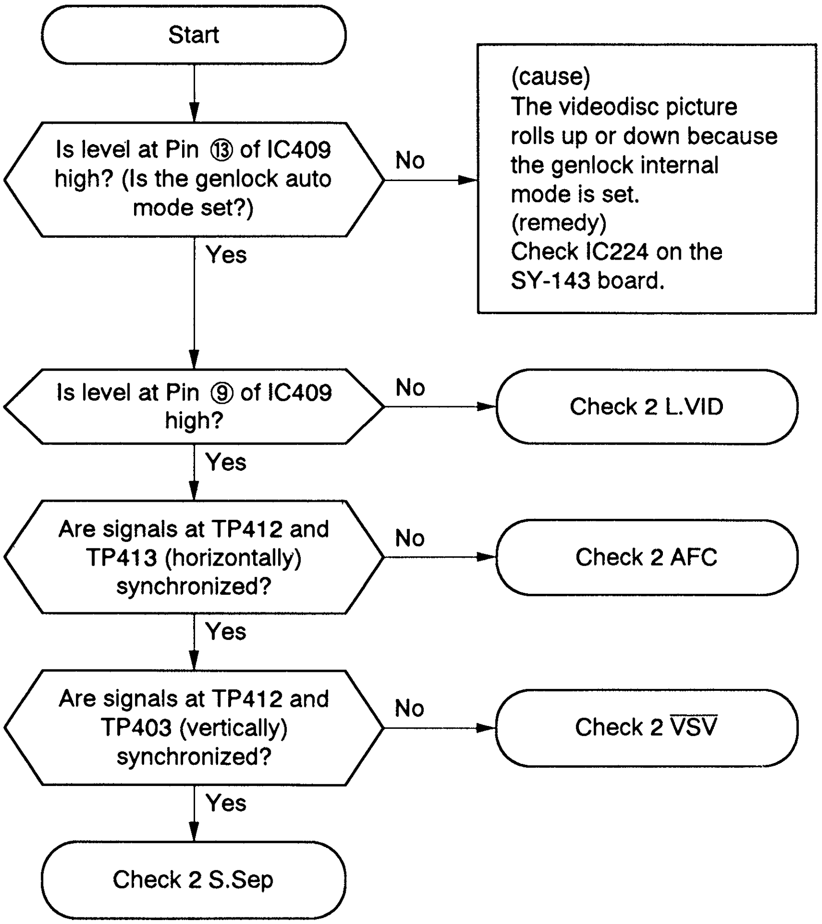

Start
Are both computer and video pictures missing?
Yes
No
Is the monitor cable properly connected?
No
Connect it.
Yes
Is only the computer picture missing?
No
Yes
SY-143 board trouble (software setting, etc.)
VS-39 board trouble
Is the videodisc picture missing?
Yes
Check 1
No
The videodisc picture is not synchronized to the computer picture
Check 2

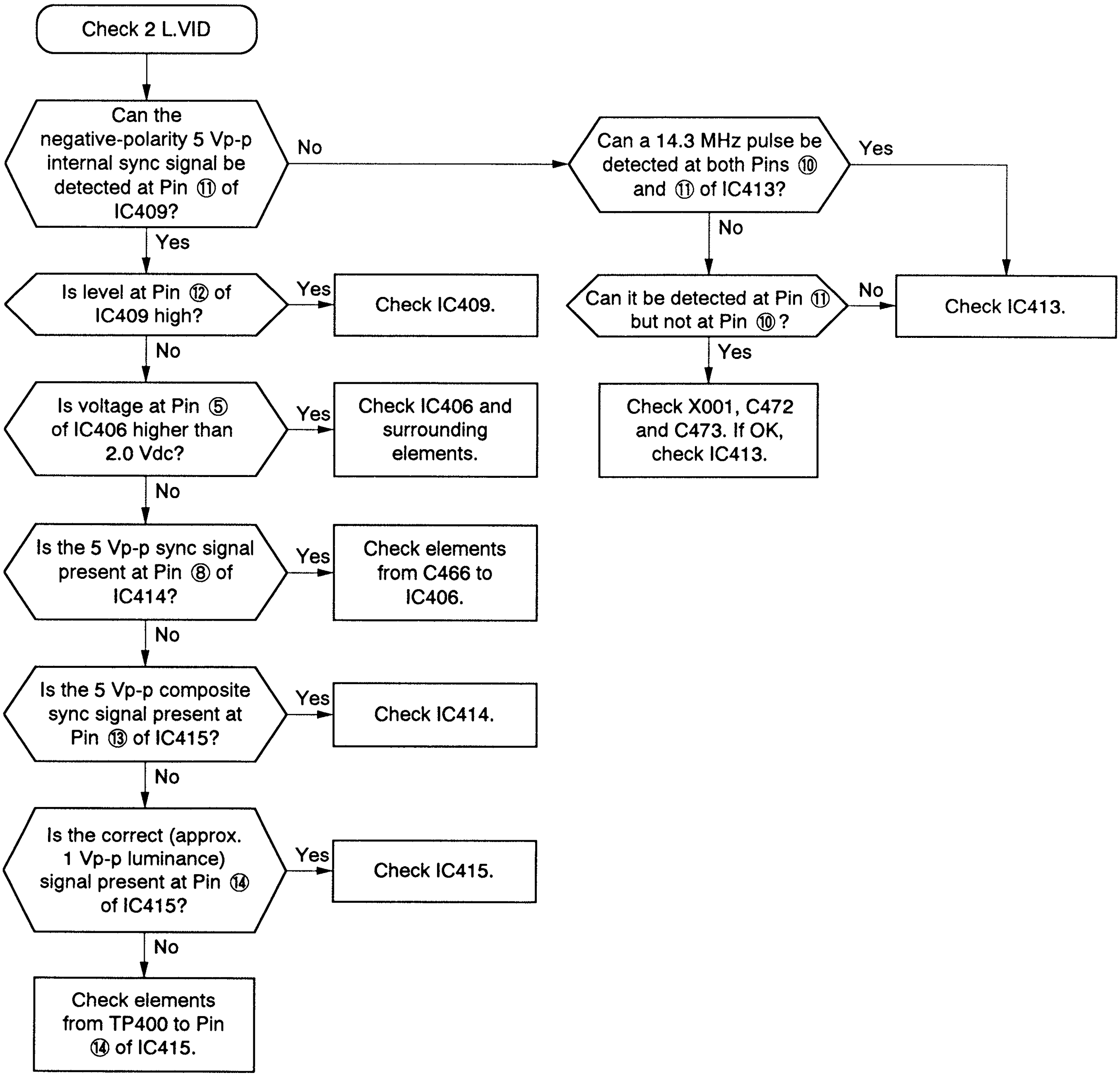
7-4-1-1. Check 1

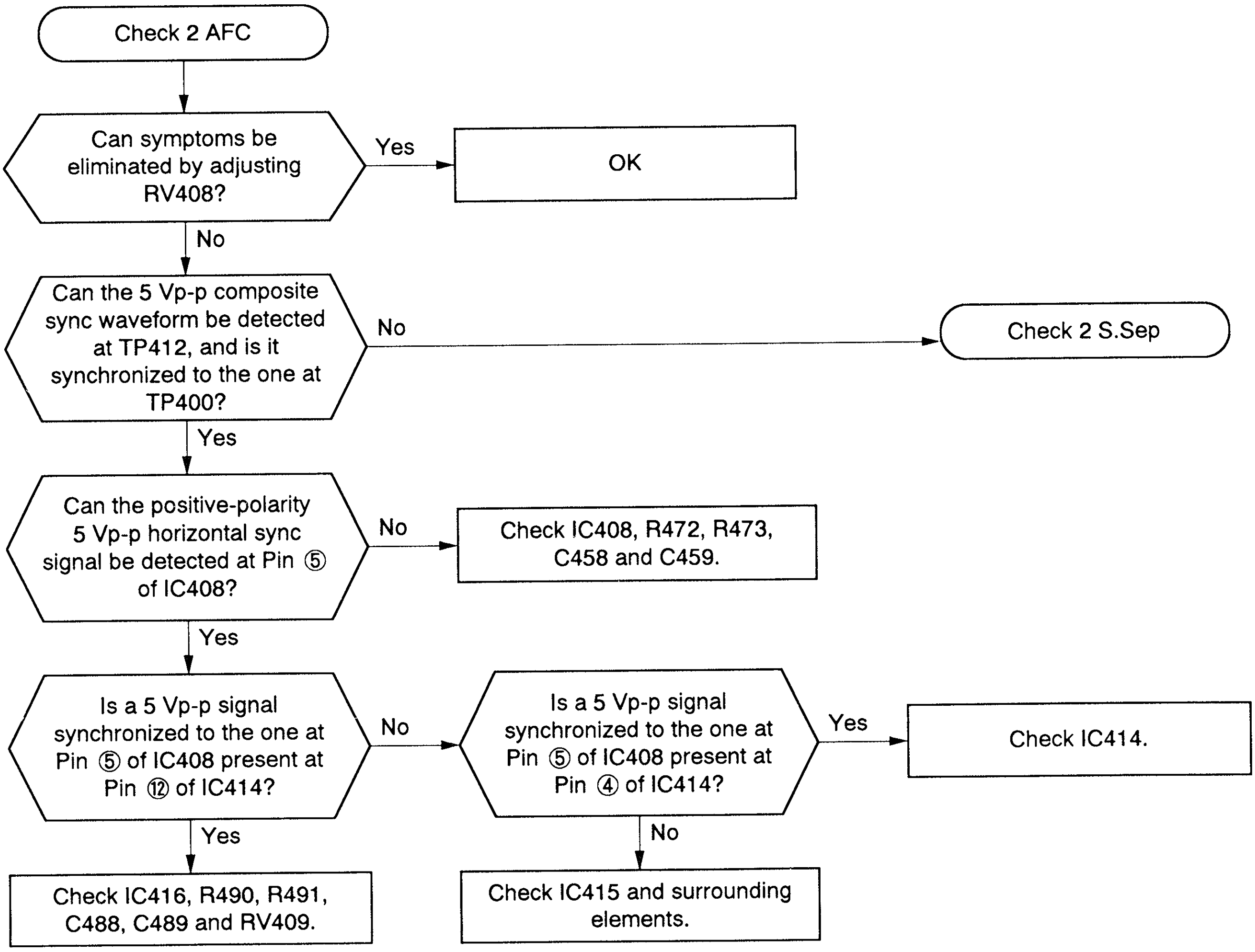

Start
Is output normal at Pins ① to ⑥ of IC402, IC403 and IC404 (5 Vp-p pulse)?
Yes
Check the SY-143 board.
No
Is input to Pin ⑫ of IC402, IC403 and IC404 normal? Signal leve...Approx. 0.7 Vp-p Clamping level...2.5 Vdc
Yes
Is a 14 MHz, 5 Vp-p clock pulse being input to Pin ⑦ of IC402, IC403 and IC404?
No
Check the ADCLK line.
Yes
Is voltage at Pins ⑪ and ⑬ of IC402, IC403 and IC404 normal? Pin ⑪...3.2 Vdc Pin ⑬...2.5 Vdc
No
Check IC401 and its surroundings.
Yes
Check IC402, IC403 and IC404.
No
Is output from the emitters of Q412, Q413 and Q414 normal? Signal level...Approx. 0.7 Vp-p Clamping level...2.5 Vdc
Yes
Perform pattern check from R453, R455 and R457 to Pin ⑫ of IC402, IC403 and IC404.
No
Is the waveform from the base of Q412, Q413 and Q414 normal? Signal level...Approx. 0.7 Vp-p Clamping level...3.1 Vdc
Yes
Check Q412, Q413 and Q414.
No
Is a waveform present at the base of Q412, Q413 and Q414?
Yes
Is voltage at Pins ④, ⑭ and ⑮ of IC405 3.1 Vdc?
No
Check R461 and Q415.
Yes
Is a (positive polarity) BF signal present at Pins ⑨, ⑩ and ⑪ of IC405?
No
Check BF.
Yes
Check IC405.
No
Is a signal present at Pins ⑯, ⑰ and ⑱ of IC400?
No
Is Y & C input to Pins ㉔ and ㉗ of IC400 normal?
No
Check the circuit from the video input to Q405 and Q411. *3
Yes
Check C432, C433 and C434.
Yes
Check IC400 and surrounding elements.

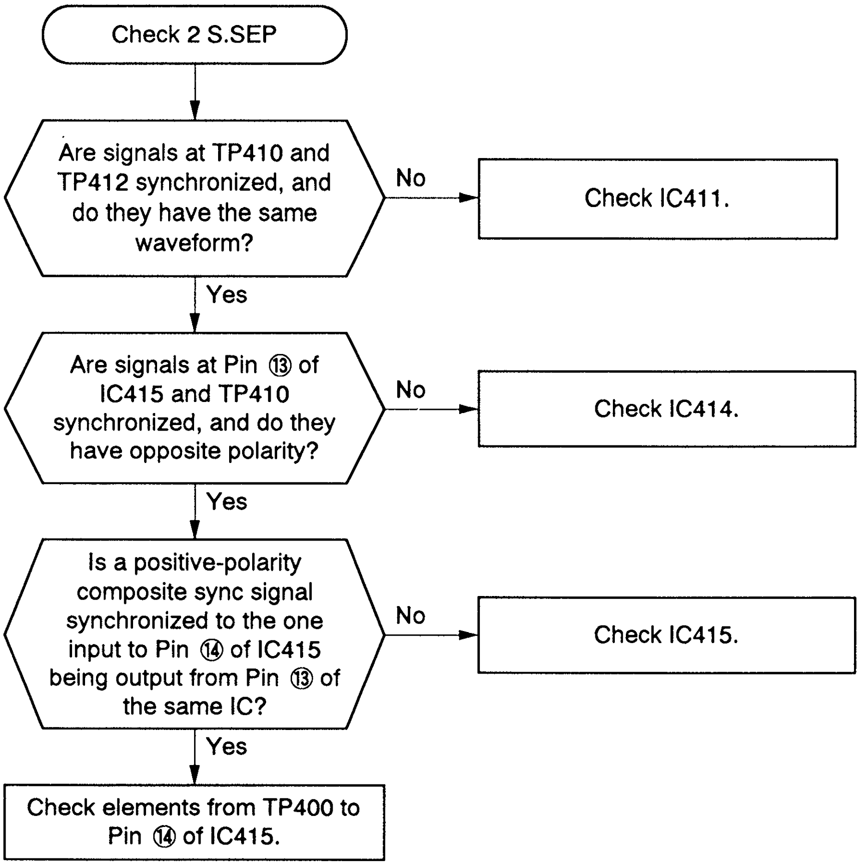

BF Check
Is a (negative polarity) BF signal present at Pin ① of IC411?
No
Check R440, RV402 and IC400.
Yes
Is level at Pin ② of IC411 high?
No
Check 2 L.VID
Yes
Check IC411.

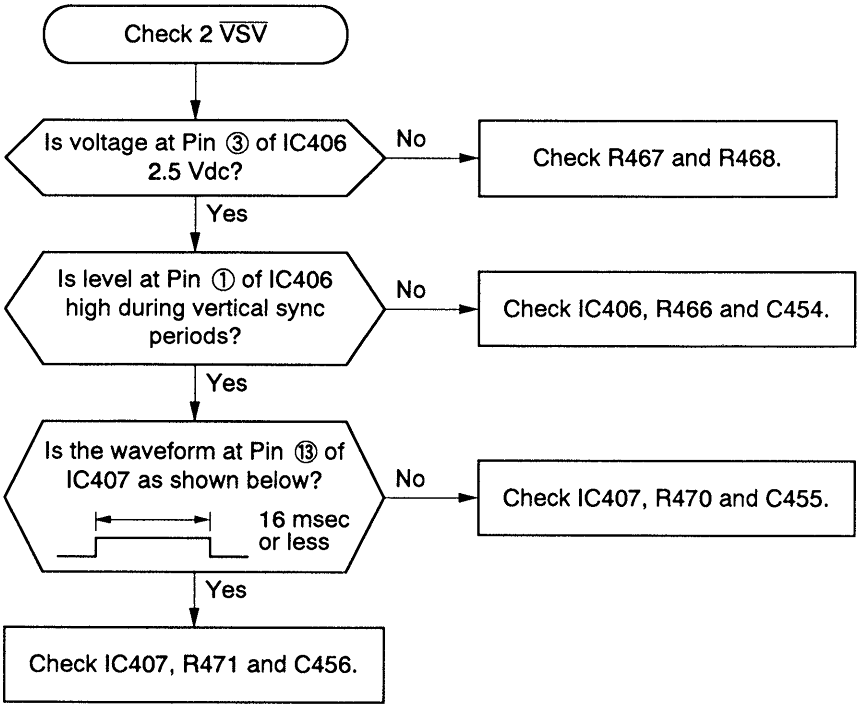
7-4-1-2. **Check 2**


Start
Is level at Pin ⑬ of IC409 high? (Is the genlock auto mode set?)
No
(cause)
The videodisc picture rolls up or down because the genlock internal mode is set.
(remedy)
Check IC224 on the SY-143 board.
Yes
Is level at Pin ⑨ of IC409 high?
No
Check 2 L.VID
Yes
Are signals at TP412 and TP413 (horizontally) synchronized?
No
Check 2 AFC
Yes
Are signals at TP412 and TP403 (vertically) synchronized?
No
Check 2 $\overline{\text{VSV}}$
Yes
Check 2 S.Sep


Check 2 L.VID
Can the negative-polarity 5 Vp-p internal sync signal be detected at Pin ⑪ of IC409?
No
Can a 14.3 MHz pulse be detected at both Pins ⑩ and ⑪ of IC413?
Yes
No
Can it be detected at Pin ⑪ but not at Pin ⑩?
No
Check IC413.
Yes
Check X001, C472 and C473. If OK, check IC413.
Yes
Is level at Pin ⑫ of IC409 high?
Yes
Check IC409.
No
Is voltage at Pin ⑤ of IC406 higher than 2.0 Vdc?
Yes
Check IC406 and surrounding elements.
No
Is the 5 Vp-p sync signal present at Pin ⑧ of IC414?
Yes
Check elements from C466 to IC406.
No
Is the 5 Vp-p composite sync signal present at Pin ⑬ of IC415?
Yes
Check IC414.
No
Is the correct (approx. 1 Vp-p luminance) signal present at Pin ⑭ of IC415?
Yes
Check IC415.
No
Check elements from TP400 to Pin ⑭ of IC415.


Check 2 AFC
Can symptoms be eliminated by adjusting RV408?
Yes
OK
No
Can the 5 Vp-p composite sync waveform be detected at TP412, and is it synchronized to the one at TP400?
No
Check 2 S.Sep
Yes
Can the positive-polarity 5 Vp-p horizontal sync signal be detected at Pin ⑤ of IC408?
No
Check IC408, R472, R473, C458 and C459.
Yes
Is a 5 Vp-p signal synchronized to the one at Pin ⑤ of IC408 present at Pin ⑫ of IC414?
No
Is a 5 Vp-p signal synchronized to the one at Pin ⑤ of IC408 present at Pin ④ of IC414?
Yes
Check IC414.
Yes
Check IC416, R490, R491, C488, C489 and RV409.
No
Check IC415 and surrounding elements.

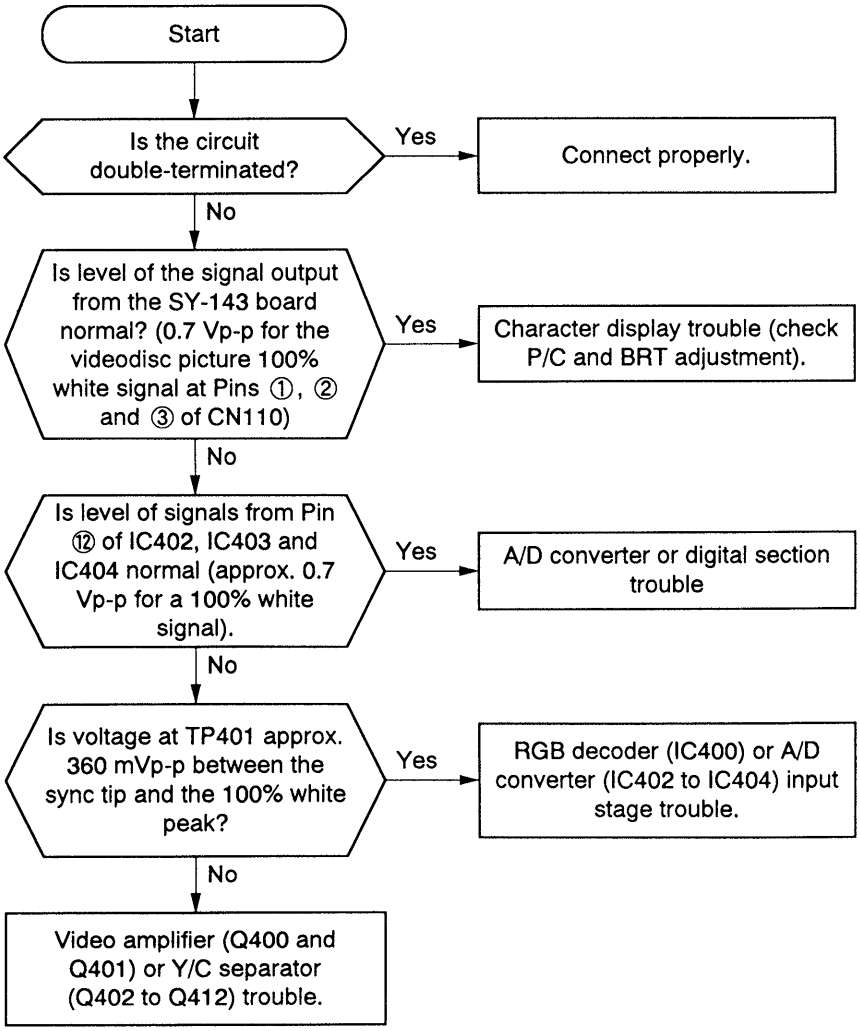

Check 2 S.SEP
Are signals at TP410 and TP412 synchronized, and do they have the same waveform?
No
Check IC411.
Yes
Are signals at Pin ⑬ of IC415 and TP410 synchronized, and do they have opposite polarity?
No
Check IC414.
Yes
Is a positive-polarity composite sync signal synchronized to the one input to Pin ⑭ of IC415 being output from Pin ⑬ of the same IC?
No
Check IC415.
Yes
Check elements from TP400 to Pin ⑭ of IC415.


Check 2 $\overline{\text{VSV}}$
Is voltage at Pin ③ of IC406 2.5 Vdc?
No
Check R467 and R468.
Yes
Is level at Pin ① of IC406 high during vertical sync periods?
No
Check IC406, R466 and C454.
Yes
Is the waveform at Pin ⑬ of IC407 as shown below?
16 msec or less
No
Check IC407, R470 and C455.
Yes
Check IC407, R471 and C456.

7-4-1-3. Check 3

a. Videodisc picture is dark.
b. Videodisc picture is slightly bluish/reddish.
c. Color of the videodisc picture is noticeably wrong.
d. No color in the videodisc picture.
e. Bright spots in the videodisc picture are blurred.

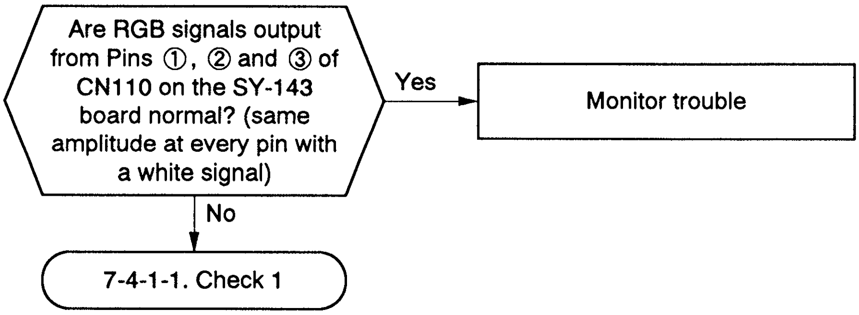
a. Videodisc picture is dark


Start
Is the circuit double-terminated?
Yes
Connect properly.
No
Is level of the signal output from the SY-143 board normal? (0.7 Vp-p for the videodisc picture 100% white signal at Pins ①, ② and ③ of CN110)
Yes
Character display trouble (check P/C and BRT adjustment).
No
Is level of signals from Pin ⑫ of IC402, IC403 and IC404 normal (approx. 0.7 Vp-p for a 100% white signal).
Yes
A/D converter or digital section trouble
No
Is voltage at TP401 approx. 360 mVp-p between the sync tip and the 100% white peak?
Yes
RGB decoder (IC400) or A/D converter (IC402 to IC404) input stage trouble.
No
Video amplifier (Q400 and Q401) or Y/C separator (Q402 to Q412) trouble.

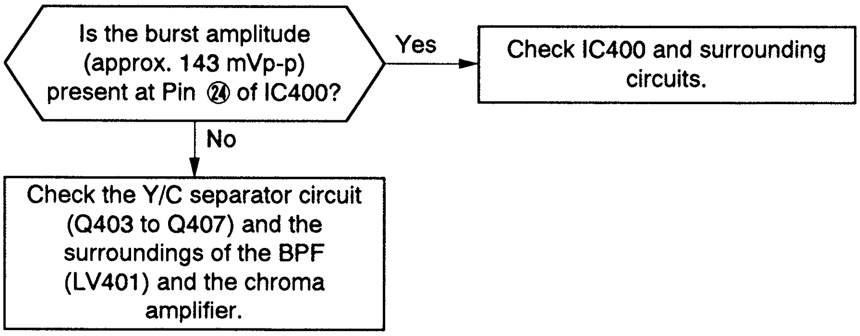
b. Videodisc picture is slightly bluish/reddish.

Try changing the rear panel hue selection switch (SW301 on the SY-143 board) position.

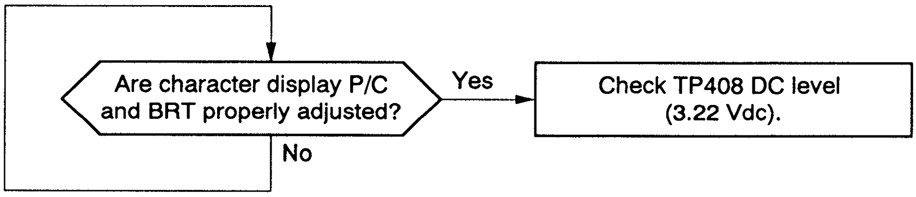
c. Color of the videodisc picture is noticeably wrong (one or two of RGB colors missing)


Are RGB signals output from Pins ①, ② and ③ of CN110 on the SY-143 board normal? (same amplitude at every pin with a white signal)
Yes
Monitor trouble
No
7-4-1-1. Check 1

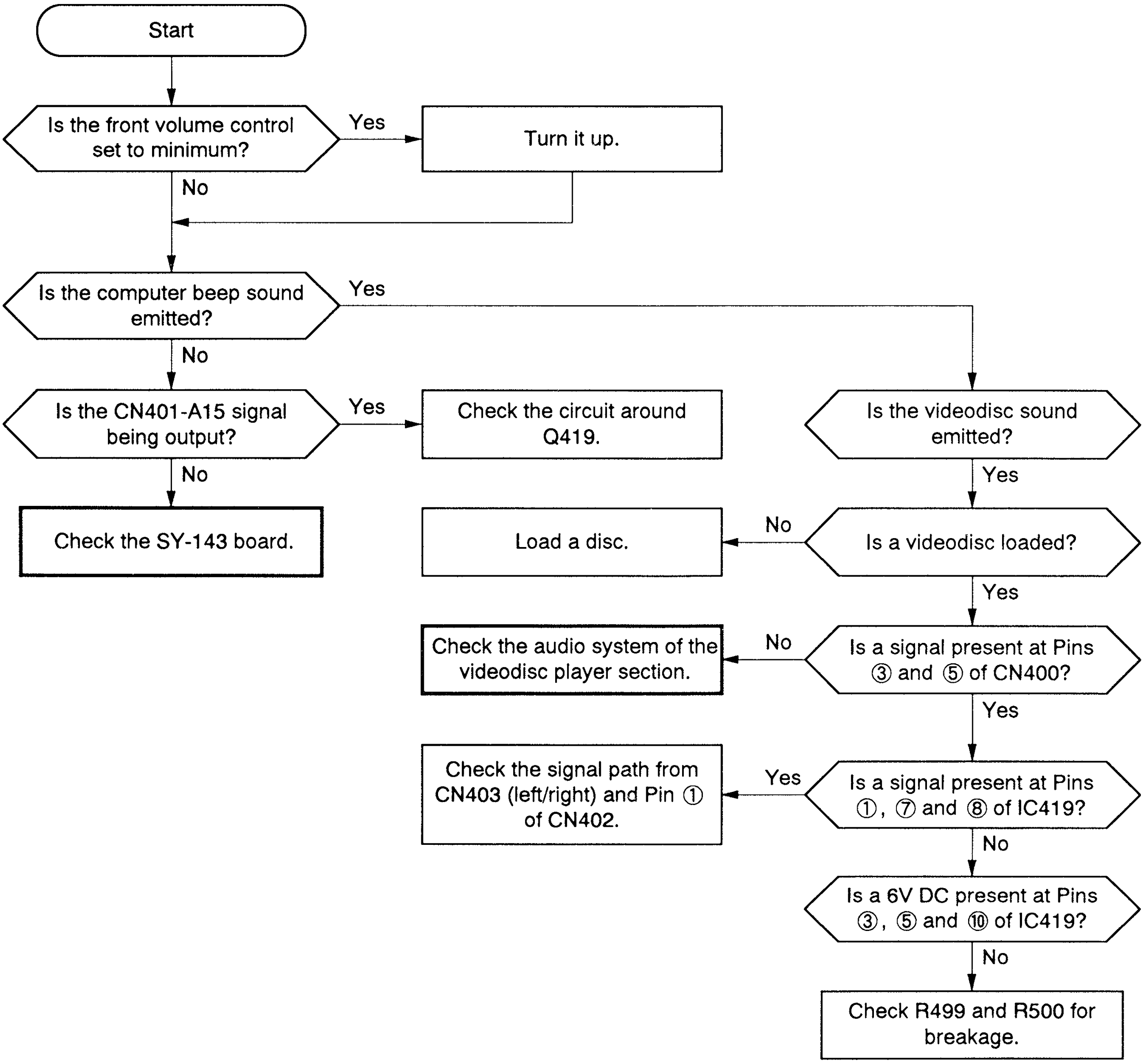
d. No color in the videodisc picture.


Is the burst amplitude (approx. 143 mVp-p) present at Pin ㉔ of IC400?
Yes
Check IC400 and surrounding circuits.
No
Check the Y/C separator circuit (Q403 to Q407) and the surroundings of the BPF (LV401) and the chroma amplifier.

e. Bright spots in the videodisc picture are blurred


Are character display P/C and BRT properly adjusted?
Yes
Check TP408 DC level (3.22 Vdc).
No

7-4-2. No Sound


Start
Is the front volume control set to minimum?
Yes
Turn it up.
No
Is the computer beep sound emitted?
Yes
No
Is the CN401-A15 signal being output?
Yes
Check the circuit around Q419.
No
Check the SY-143 board.
Is the videodisc sound emitted?
Yes
Is a videodisc loaded?
No
Load a disc.
Yes
Is a signal present at Pins ③ and ⑤ of CN400?
No
Check the audio system of the videodisc player section.
Yes
Is a signal present at Pins ①, ⑦ and ⑧ of IC419?
Yes
Check the signal path from CN403 (left/right) and Pin ① of CN402.
No
Is a 6V DC present at Pins ③, ⑤ and ⑩ of IC419?
No
Check R499 and R500 for breakage.

CHAPTER 8
ADJUSTMENT

There is a LDP-1200-type videodisc player mounted on the computer block. Disconnect it as explained in Chapter 2 before adjustment.

8-1. TOOLS LIST

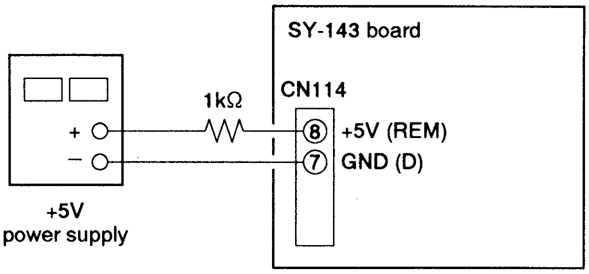
In general, adjustment of this unit requires the following equipments:

1. Monitor (CPD-1302 etc.) and Monitor cable
2. SMW-5001 (MS-DOS)
3. Accessories floppydisk
4. Frequency counter
5. Oscilloscope (refer to section 8-2-3)
6. EIA color-bar signal generator (refer to section 8-2-4)
7. VS-39 extension board: P/N ~~J-6093- -A~~ J-6082-093-A
8. VS-39 extension cable: P/N J-6082-092- A
9. DC regulated power supply
10. Screwdrivers for adjustment
11. Soldering iron and solder

8-2. PREPARATION

8-2-1. Connections for Performing Adjustments without Connecting the Videodisc Player Section

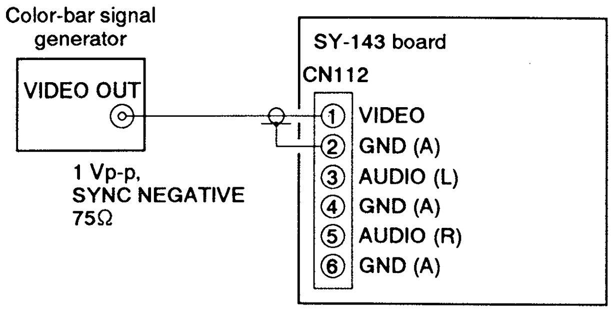
1. Connection for turning the power on
   Apply a +5V voltage to Pin ⑧ of CN114 on the SY-143 board through a 1 kΩ resistor.



SY-143 board
CN114
1kΩ
+
−
⑧ +5V (REM)
⑦ GND (D)
+5V
power supply

Fig. 8-1.

2. Connection required to input the video signal



Color-bar signal generator
VIDEO OUT
1 Vp-p,
SYNC NEGATIVE
75Ω
SY-143 board
CN112
① VIDEO
② GND (A)
③ AUDIO (L)
④ GND (A)
⑤ AUDIO (R)
⑥ GND (A)

Fig. 8-2.

8-2-2. Setting the VS-39 Board Upright

The VS-39 board must be set upright in order to perform adjustments.

1. Unplug the following two connectors and detach the VS-39 board from the SY-143 board.
   1. CN400 (VS-39 board)
   2. CN401 (VS-39 board)
2. Connect CN115 (SY-143 board) to CN401 (VS-39 board) with the VS-39 extension board (J-6082-093 -A).
3. Connect CN113 (SY-143 board) to CN400 (VS-39 board) with the VS-39 extension cable (J-6082 -092 -A).

8-2-3. About Oscilloscope

An oscilloscope capable of following three or more waveforms (or two, if it has an external trigger input terminal) and provided with a TV sync (field, line) separator is required for adjustment of the computer block.

- Band width limit
  This function restraints high-frequency components to make the waveform easier to observe. However, adjustment is also possible without this function.
- TV-LINE and TV-FLD
  Shows the TV sync separator trigger mode.

8-2-4. About Video Signal

EIA standard color-bar signal (NTSC, setup 0%, white level 100%, 1 Vp-p) is used as the video signal for the adjustment.
While adjust the computer block, must always give this signal to the computer block.

8-2-5. Initial Setting

- VS-39 board
  SL400 ....Short by the solder
  SL401 ....Open
- SY-143 board
  SW301 ....3 side (at right, seen from the rear)
  TP201 ....0 side (33CH to 33FH side)
  JP204, JP205 } .... Short-circuit with shorting plugs if not equipped with SMI-5051 (graphics memory expansion).

8-3. RUN SYSTEM

Operation 1: Power on, the monitor. Also, the oscilloscope and signal generator.

Operation 2: Insert system disk (SMW-5001) of MS-DOS in drive A and power on the computer block.

Operation 3: When the main menu appears on the monitor, select "Exit to MS-DOS".

Operation 4: At the "A>" prompt, type in the following to start the diagnostic program.
CD \DIAG ENTRY
DIAG ENTRY

Operation 5: Select the diagnostic program 2.2.2 Video/Monitor diagnostic manual mode.

Operation 6: Set modes as follows:
Display mode: 12
Genlock mode: Automatic
Superimpose mode: Superimpose

8-4. VS-39 BOARD

8-4-1. H AFC Adjustment

Confirmation 1: Applied the solder on the pattern jumper SL401 (Pin ③ of IC415 — GND)
Measuring equipment: Oscilloscope
Vertical mode: CHOP
Trigger channel: ch-2
Trigger slope: Up edge
Trigger coupling: AC
Measuring point ch-1: TP413 (coupling: DC)
Measuring point ch-2: TP412 (coupling: DC)

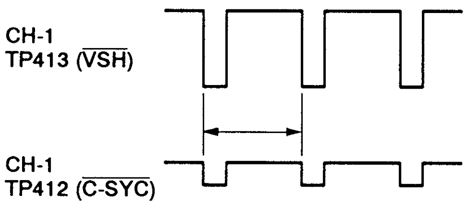


Fig. 8-3. TP413, TP412

Specification: T=63.5 ± 0.5 µsec
Adjustment: RV408
Adjust the RV408 so that waveform of ch-1 drifts slowest.

Note: Set oscilloscope to 2V/DIV and 20 µsec/DIV.

Operation 1: Power off, the computer
Operation 2: Remove the solder from the pattern jumper SL401.
Operation 3: Power on, the computer.
Operation 4: Run system (refer to section 8-3)
Confirmation 2: Monitor screen and waveform of ch-1 are stable.

8-4-2. APC Adjustment

Operation 1: Power off, the computer
Operation 2: Remove the solder from the pattern jumper SL400.
Operation 3: Power on, the computer
Operation 4: Run system (refer to section 8-3)
Measuring equipment: Monitor

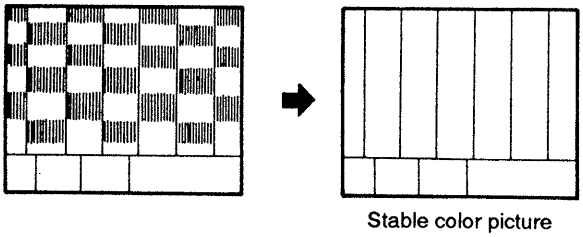


Fig. 8-4. Monitor screen

Specification: Color-sync is stable. See Fig. 8-4.
Adjustment: RV403

Operation 5: Power off, the computer
Operation 6: Apply the solder on the pattern jumper SL400.
Operation 7: Power on, the computer
Operation 8: Run system (refer to section 8-3)
Confirmation: Color-sync is stable. See Fig. 8-4.

8-4-3. Output RGB Level Adjustment

Measuring equipment: Oscilloscope
Vertical mode: ch-1
Trigger channel: ch-2
Trigger slope: Up edge
Trigger coupling: AC
Measuring point ch-1: TP404 (coupling:DC)
Operation 1: Undo all connections between the oscilloscope and other devices (including the VIEW-5000). If the oscilloscope and the VIEW-5000 are left grounded, IC401 on the VS-39 board will break.
Operation 2: Connect the ground clip of the oscilloscope channel-1 probe to TP408, and the channel-1 probe to TP404.

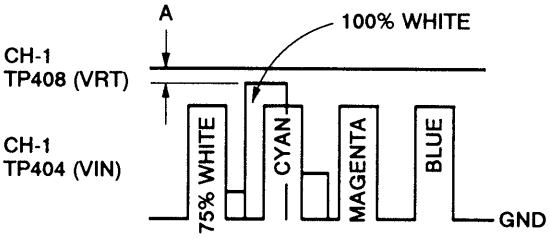


Fig. 8-5. TP408, TP404

Specification: A=40 ± 10 mV
Adjustment: RV401

Note: Set oscilloscope to 50 mV/DIV and 20 µsec/DIV.

8-4-4. Carrier Leak Level Adjustment

- Measuring equipment: Oscilloscope
  - Vertical mode: ch-1
  - Trigger channel: ch-2
  - Trigger slope: Up edge
  - Trigger coupling: AC
- Measuring point ch-1: TP401 (coupling: AC)
- Measuring point ch-2: TP412 (coupling: AC)

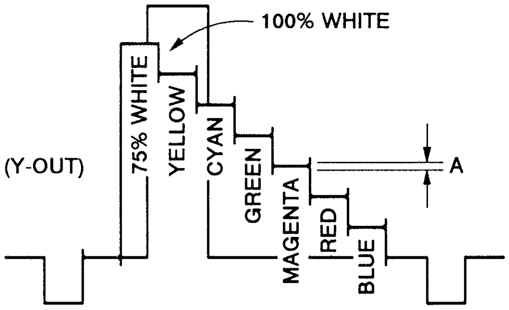


Fig. 8-6. TP412

Specification: A ≦ 10 mVp-p

Adjustment: RV400, LV400 (alternately adjust)

Note: Set oscilloscope to 50 mV/DIV and 10 μsec/DIV adjust with the level of the magenta color bar.

8-4-5. Burst Flag Position Adjustment

- Measuring equipment: Oscilloscope
  - Vertical mode: ALT
  - Trigger channel: ch-2
  - Trigger slope: Up edge
  - Trigger coupling: AC
- Measuring point ch-1: TP401 (coupling:AC)
- Measuring point ch-2: TP407 (coupling:AC)

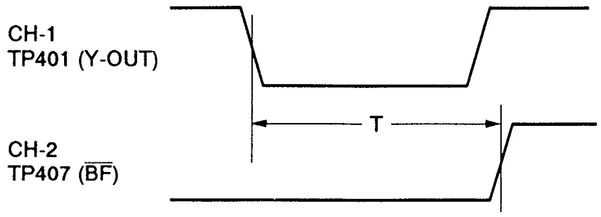


Fig. 8-7. TP401, TP407

Specification: T=5.3 ± 0.1 μsec

Adjustment: RV402

Note: Set oscilloscope to 1 μsec/DIV, 0.1 mV/DIV at ch-1, and 5V/DIV at ch-2.

8-4-6. Hue and Color Adjustment

- Measuring equipment: Oscilloscope
  - Vertical mode: ch-1
  - Trigger channel: ch-2
  - Trigger slope: Up edge
  - Trigger coupling: TV-LINE
- Measuring point ch-1: TP404 (coupling:AC)
- Measuring point ch-2: TP413 (coupling:AC)

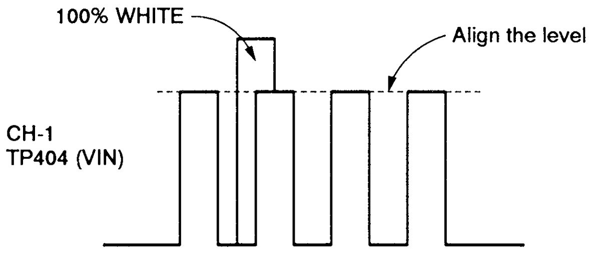


Fig. 8-8. TP404

Specification: Refer to Fig. 8-8.

Adjustment: RV404, RV410 (alternately adjust)

Note: Set oscilloscope to 0.2V/DIV and 20 μsec/DIV.

8-4-7. Vertical Reset Timing Adjustment

Confirmation: Confirm that the superimpose mode is set (refer to section 8-3).

- Measuring equipment: Oscilloscope
  - Vertical mode: CHOP
  - Trigger channel: ch-3
  - Trigger slope: Up edge
  - Trigger coupling: TV-FLD
- Measuring point ch-1: TP411 (coupling: DC)
- Measuring point ch-2: TP410 (coupling: DC)
- Measuring point ch-3: TP409

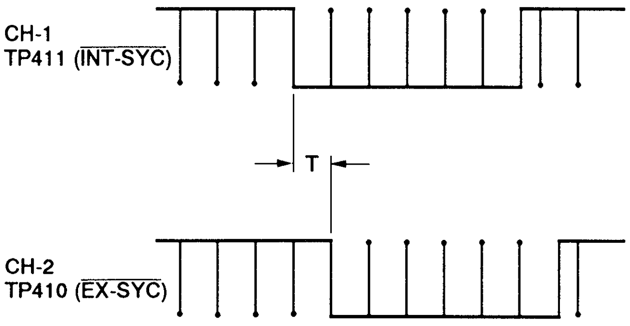


Fig. 8-9. TP411, TP410

Specification: T= ± 0.5H

Adjustment: RV407

Note: Set oscilloscope to 50 μsec/DIV.

8-4-8. H Position Adjustment

Measuring equipment: Oscilloscope
  Vertical mode: ALT, Band with limit (20 MHz)
  Trigger channel: ch-2
  Trigger slope: Down edge
  Trigger coupling: DC
Measuring point ch-1: TP401 (coupling: AC)
Measuring point ch-2: TP413 (coupling: DC)

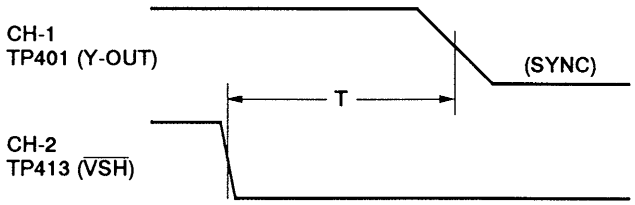


Fig. 8-10. TP401, TP413

Specification: T=670 ± 20 μsec
Adjustment: RV409

Note: Set oscilloscope to 20 nsec/DIV, 0.1V/DIV at ch-1, and 2V/DIV at ch-2.

8-4-9. Vertical Blanking Adjustment

Measuring equipment: Oscilloscope
  Vertical mode: ch-1
  Trigger channel: ch-1
  Trigger slope: DOWN edge
  Trigger coupling: DC
Measuring point ch-1: Pin ④ of IC410 (coupling:DC)

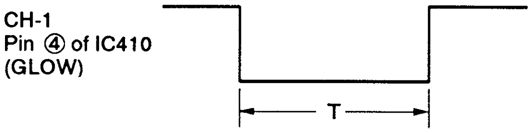


Fig. 8-11. Pin ④ of IC410

Specification: T=965 ± 20 μsec
Adjustment: RV406

8-5. SY-143 BOARD

8-5-1. P RAM Latch Timing Adjustment

Measuring equipment: Oscilloscope
  Vertical mode: CHOP
  Trigger channel: ch-2
  Trigger source: Up edge
  Trigger coupling: DC
Measuring point ch-1: TP206 (coupling: DC)
Measuring point ch-2: TP202 (coupling: DC)
Operation: Match the middle level of channels 1 and 2, so that A=B and C=D.

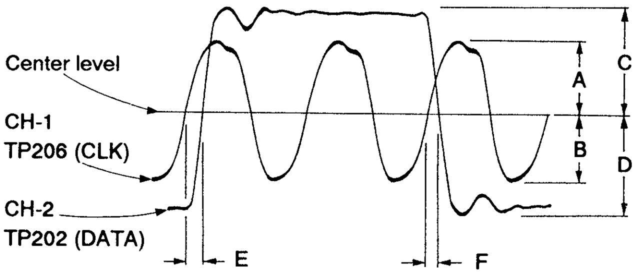


Fig. 8-12. TP206, TP202

Specification: E=0 ± 5 nsec
F=0 ± 5 nsec
Adjustment: JP202
Set the JP202 jumper to the position that minimizes E and F.

Note: Set oscilloscope to 10 nsec/DIV, 1V/DIV at ch-1, 1V/DIV at ch-2.

8-5-2. VCO Adjustment

Confirmation: Confirm that the superimpose mode is set (refer to section 8-3).
Measuring equipment: Oscilloscope
  Vertical mode: ch-1
  Trigger channel: ch-1
  Trigger slope: Up edge
  Trigger coupling: AC
Measuring point ch-1: TP201 (coupling: DC)

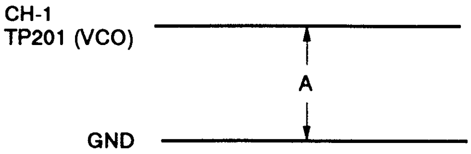


Fig. 8-13. TP201

Specification: A=3.0 ± 0.1V
Adjustment: L307

8-5-3. Setting In After Adjustment

- VS-39 board
  SL400 ············Short by the solder
  SL401 ············Open
- SY-143 board
  SW301 ···········3 side (at right, seen from the rear)
  TP201 ············0 side (33CH to 33FH side)
  JP204 } ······· Short-circuit with shorting plugs if not equipped
  JP205 } with SMI5051 (graphics memory expansion).

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Home Video Group

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VIW-5000

SERVICE MANUAL

SUPPLEMENT-2

This supplement-2 is added THEORY OF OPERATION and BLOCK DIAGRAM.

Refer to the service manual for OPERATION, SERVICE INFORMATION, SCHEMATIC DIAGRAM and REPAIR PARTS AND FIXTURES.

Refer to the supplement-1 for SELF-DIAGNOSTICS, TROUBLESHOOTING and ADJUSTMENT.

Sony VIEW System

SONY®

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CHAPTER 3
THEORY OF OPERATION

3-1. SYSTEM CONTROL BLOCK

3-1-1. General

The SY-143 board consists of a system control block and a graphic control block.
The system control block of the SY-143 board consists of a CPU, an AT chip set block, a BIOS ROM, a main memory block, a peripheral block and an AT-Bus block as shown in Fig. 3-1.
These blocks are connected from such address buses as A-Bus, ADDR-Bus, LADDR-Bus and RAMADR-Bus, and such data-Buses as D-Bus, DATA-Bus, EDATA-Bus and MDATA-Bus, to perform the function of the system control block.

a) CPU
The 16 bit CPU 80286 clock frequency is 10 MHz.

b) AT chip set block
This block consists of FE3001, FE3010B, FE3021 and FE3031. FE3001 is an AT control logic, FE3010B is an AT peripheral control logic block, FE3021 is an AT address buffer and memory controller, and FE3031 is an AT data buffer.

c) BIOS ROM
This is a 128-byte (16 bit × 64 Kbit) type ROM using two 512 Kbit PROMs. The BIOS ROM makes use of a genuine Phoenix ROM so that it is compatible with IBM PC/AT. Incidentally, the graphic control VGA BIOS is also incorporated this ROM.

d) Main memory block
This block is a 2-bank type consisting of bank 0 and bank 1. There are 640 Kbyte including parity. The bank 0 is configured with 512 Kbyte (four 256 Kbit × 4 DRAMs and two 256 Kbit × 1 DRAMs), and the bank 1 with 128 Kbyte (four 64 Kbit × 4 DRAMs and two 256 Kbit × 1 DRAMs). The EMS memory can be used by adding two 1 Mbit DRAM × 9 modules (SMI-5050) to the socket as a bank 2.

e) Peripheral block
This block consists of i8742, DS1287 and VL16C452. i8742 is a single chip microcomputer for keyboard control using a 1-time PROM. The firmware for keyboard control uses Phoenix's genuine ROM, just as in the case of the BIOS and is therefore compatible with IBM PC/AT. DS1287 is a real time clock. It contains an oscillator circuit and a x'tal oscillator and the battery, and is guaranteed for a period of five years. VL16C452 is a controller with two channels of RS232C and one channel of printer I/O.

f) AT-bus block
This block consists of an AT-Bus connector, a HDD interface and 37C65B. Just as in the case of the conventional AT-Bus hitherto available, the AT-Bus connector provides an interface with address data and control signals which are compatible with it. The HDD interface is an interface with the HDD controller HDD built-in type HDD for compatibility with the IBM PC/AT. 37C65B is a floppy disk controller. Incidentally, the PVGA1A (VGA controller) of the graphic control block is also included in the AT-Bus block.

g) Address bus
A-Bus (A0 to A23): CPU ↔ AT Chip Set Block
ADDR-Bus (ADDR0 to ADDR19):
AT Chip Set Block → BIOS ROM
AT Chip Set Block ↔ AT-Bus Block
AT Chip Set Block → Peripheral Block
LADDR-Bus (LADDR17 to LADDR23):
AT Chip Set Block ↔ AT-Bus Block
RAMADR-Bus (RAMADR0 to RAMADR9):
AT Chip Set Block → Main Memory Block

(h) Data Bus
D-Bus (D0 to D15): CPU ↔ AT Chip Set Block
DATA-Bus (DATA0 to DATA15):
AT Chip Set ↔ AT-Bus Block
EDATA-Bus (EDATA0 to EDATA7):
AT Chip Set ↔ Peripheral Block
MDATA-Bus (MDATA0 to MDATA15):
AT Chip Set ↔ Main Memory
AT Chip Set ← BIOS ROM

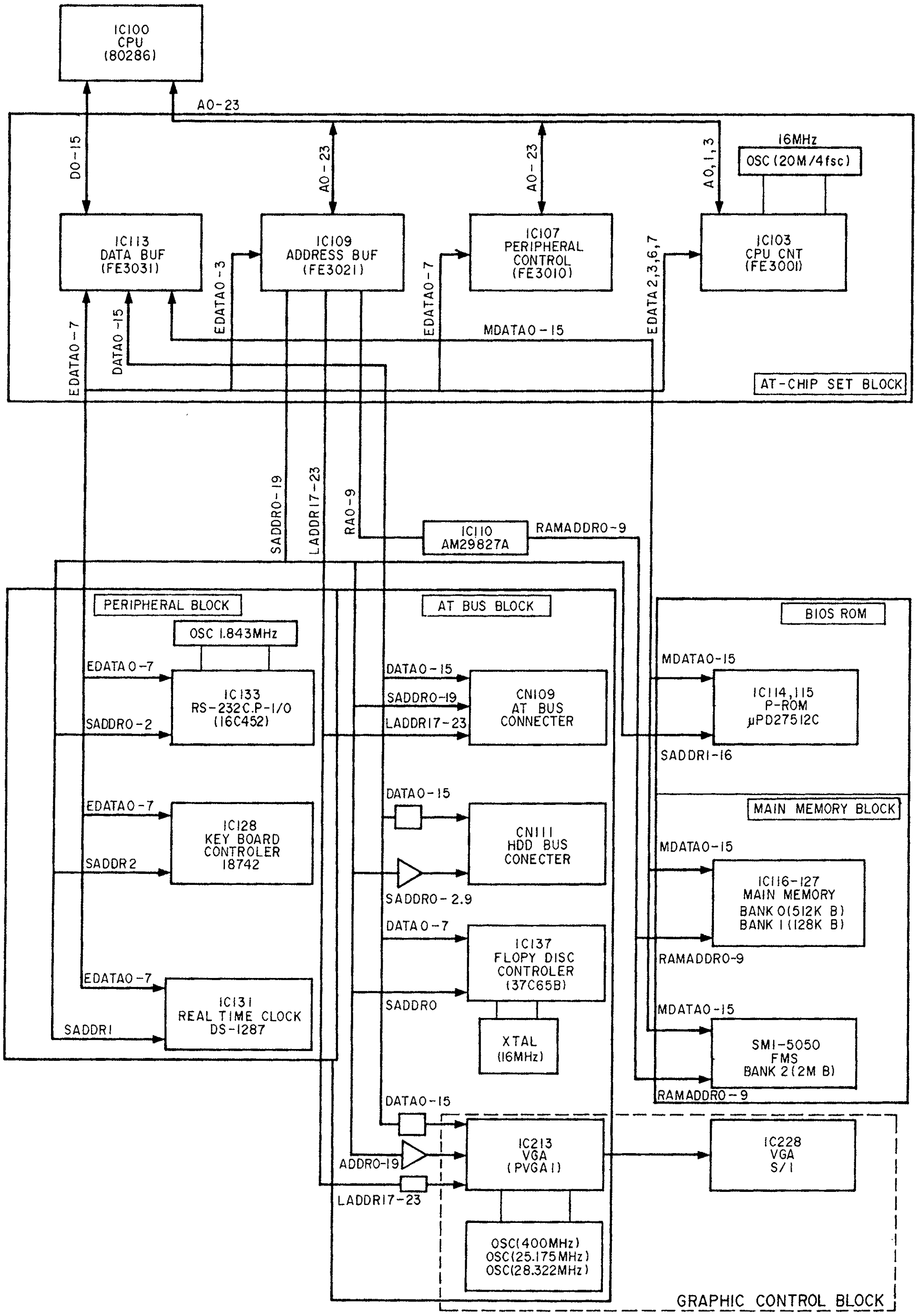

IC100
CPU
(80286)
A0-23
D0-15
A0-23
A0-23
A0,1,3
16MHz
OSC (20M/4fsc)
IC113
DATA BUF
(FE3031)
IC109
ADDRESS BUF
(FE3021)
IC107
PERIPHERAL
CONTROL
(FE3010)
IC103
CPU CNT
(FE3001)
EDATA0-3
EDATA0-7
EDATA2,3,6,7
MDATA0-15
EDATA0-7
DATA0-15
AT-CHIP SET BLOCK
SADDR0-19
LADDR17-23
RA0-9
IC110
AM29827A
RAMADDR0-9
PERIPHERAL BLOCK
OSC 1.843MHz
EDATA0-7
IC133
RS-232C.P-I/O
(16C452)
SADDR0-2
EDATA0-7
IC128
KEY BOARD
CONTROLER
18742
SADDR2
EDATA0-7
IC131
REAL TIME CLOCK
DS-1287
SADDR1
AT BUS BLOCK
DATA0-15
SADDR0-19
LADDR17-23
CN109
AT BUS
CONNECTER
DATA0-15
CN111
HDD BUS
CONECTER
SADDR0-2.9
DATA0-7
IC137
FLOPY DISC
CONTROLER
(37C65B)
SADDR0
XTAL
(16MHz)
DATA0-15
ADDR0-19
LADDR17-23
IC213
VGA
(PVGA1)
OSC(400MHz)
OSC(25.175MHz)
OSC(28.322MHz)
IC228
VGA
S/I
GRAPHIC CONTROL BLOCK
BIOS ROM
MDATA0-15
IC114,115
P-ROM
μPD27512C
SADDR1-16
MAIN MEMORY BLOCK
MDATA0-15
IC116-127
MAIN MEMORY
BANK 0(512K B)
BANK 1(128K B)
RAMADDR0-9
MDATA0-15
SMI-5050
FMS
BANK 2(2M B)
RAMADDR0-9

Fig. 3-1. System control block diagram

3-1-2. AT-Chip Set Block

3-1-2-1. FE3001: AT control logic (IC103)

FE3001 is an interface logic for interface with the programmable CPU, clock generator of DMA, system clock generator, programmable bus timing and wait-state generator, refresh controller, DMA controller, NMI generator, parity error circuit, reset circuit, and CPU 80286.

a) Clock generator

The clock generator generates clocks of CPU, DMA, 8742 (keyboard controller), and 80287 (numeric processor). The CPU clock permits a switchover between the high speed and low speed with software. The DMA clock allows a switchover to be made between 4 MHz and 8 MHz with software. The 80287 clock is fixed to the low speed of the CPU clock. Incidentally, 80287 is unused on the SY-143 board so that the 80287 clock is not required. There are three clock inputs are available, namely, CLK16 (pin 84), CLKHS (pin 1), and CLK14 (pin 83). To the CLK16, the 16 MHz clock of OSC103 is fed. It is used as a clock for 8 MHz operation (low speed) of the CPU. To the CLKLHS, the 20 MHz clock of OSC 100 is fed. It is used as a clock for 10 MHz operation (high speed) of the CPU. To CLK14, the 14.31818 MHz clock of OSC101 is fed after it has been buffered to LS125 (IC102) to generate the 8742 clock (pins 17 and 18) and the timer clock (pin 20) of FE3010B. The 8742 clock is fixed at 7.16 MHz, and the timer clock at 1.19 MHz.

b) Command control

From the inputs of NS0 (pin 82), NS1 (pin 81), and MNIO (pin 80), FE3001 generates signals such as I/O read (pin 43), I/O write (pin 45), memory read (pin 41), memory write (pin 42), ALE (pin 25), and BALE (pin 26). FE3001 also controls the wait-state of each cycle of the CPU.

c) A0, BHE generator

ADR0 (pin 47), NABHE (pin 37) and NEBHE (pin 46) are generated from A0 (pin 69) and NBHE (pin 48) applied from 80286, and also from DACK2 (pin 79) applied from the DMA controller of FE3010B. At the CPU cycle, A0 from 80286 is latched by ALE to generate ADR0. During the 16 bit DMA and the interrupt acknowledge cycle, ADR0 is brought to "L" to make the low byte of the data bus active. In other states in which the CPU remains held, ADR0 is placed in the try state. During a CPU cycle, NAEHE is generated by latching NBHE from 80286 with the ALE. NEBHE is generated by latching NABHE with the ALE. During the 16 bit DMA, NABHE is "L" to make the low byte of data bus active. During the 8 bit DMA, ADR0 coming from the DMA controller is inverted to become NABHE. In other states in which the CPU is held, the NEBHE is put into the tri-state.

d) Others

FE3001 generates a hold request to the CPU according to the hold request of the DMA controller and the refresh timer. In response to the refresh request, a refresh cycle control signal is generated. During the DMA cycle, HLDA1 (pin 9) is generated. The DMA RDY signal indicates the completion of the DMA cycle. FE3001 generates an NMI to 80286 when a parity error or system bus error is occurred. The functions of the parity error, system bus error and NMI can be switched between enable/disable by software. RESCPU (pin 56) transmits a power on reset signal and a CPU reset signal coming from the keyboard controller to 80286. A system reset signal is similarly generated as NRESET (pin 3).

e) Register

FE3001 has the error control register, speed select register, NMI enable register, command control registers and command register pointer. The write and read operations of these can be made by software.

- The error control register enables and disables both signals of parity error and I/O channel check. Address is I/O port 061H.
- The speed select register makes speed control of the CPU and the DMA. This register has the function of setting the CPU into the sleep mode and that of locking and unlocking the speed select register and the command control register. Address is I/O port 063H.
- The NMI enable register enables and disables the NMI. Address is I/O port 070H.
- The command control register controls the number of the BALE, NYMEMR, NYMEMW, NYIOR, NYIOW and WAIT to be output to the AT-Bus. Address is I/O port 073H.
- The command register pointer is for selecting one out of eleven registers in 073H. Address is 072H of I/O port.

PIN No.	SIGNAL	I/O	DESCRIPTION
1	CLKHS	I	High speed clock input (40 MHz max.). This provides the high speed clock when selected. When CLK16 (pin 84) is pulled high, this input (divided by two) is used as the low speed clock.
2	Vss1		Ground.
3	NRESET	O	Reset to the system.
4	NONBRDL	O	NONBRD input latched by ALE internally.
5	CPURES	O	Reset to 80286.
6	RTCALE	O	Real Time Clock Address Latch Enable (I/O address 70H).
7	HOLDRQ	O	Hold request to 80286 for DMA or Refresh.
8	NERFSH	O	Enable refresh address signal to FE3010. Puts refresh address on address bus.
9	HLDA1	O	DMA hold acknowledge signal to FE3010.
10	NINTA	O	Interrupt acknowledge to FE3010.
11	RST287	O	Reset to 80287 (Write to I/O address F1H or system reset).
12	Vss2		Ground.
13	NBZ286	O	80287 busy signal to 80286.
14	NIRQ13	O	Interrupt request 13 for 80287 error to FE3010.
15	NMI	O	Non-Maskable Interrupt to 80286. Generated in response to a parity error or bus IOCHCK.
16	NNPCS	O	80287 Co-processor chip select (F8).
17	PCLK	O	7.16 MHz clock for keyboard controller.
18	NPCLK	O	Inverted PCLK.
19	VDD1		+5V VDD.
20	TMRCLK	O	1.19 MHz timer clock to FE3010.
21	DMACLK	O	Software selectable clock for DMA to FE3010.
22	SYSCLK	O	System clock needed for bus timing. See description in synchronization section.
23	Vss3		Ground.
24	PROCLK	O	Software selectable 80286 clock.
25	ALE	O	Local Address Latch Enable. 3.
26	BALE	O	Bus Address Latch Enable. (Programmable)
27	CLK287	O	Clock for 80287. See clock section for details.
28	DTR	O	Data direction to data buffers.
29	NDEN0	O	Low byte data enable to data buffers.
30	NDEN1	O	High byte data enable to data buffers.
31	SDTR	O	Byte swap data direction to data buffers.
32	NSDEN	O	Byte swap data enable to data buffers.
33	SCYCLE	O	Latch low byte during byte swap read.
34	ACK	O	DMA Acknowledge signal to the PC/AT bus.
35	NREADY	O	Ready to CPU.
36	DMARDY	O	End DMA cycle to FE3010.
37	NABHE	O	High byte enable for devices on local bus.
38	Vss4		Ground.
39	NREFRESH	I/O	Refresh cycle. Generated from timer OUT1 or externally from the bus.
40	NDLYWR	I/O	NYIOW delayed to the FE3010, active edge delayed one PROCLK. Input from FE3010 in during DMA to generate NYIOW.
41	NYMEMR	I/O	Memory read. Input during Master cycle.
42	NYMEMW	I/O	Memory write. Input during HLDA cycle.
43	NYIOR	I/O	I/O read. Input during HLDA cycle.
44	VSS5	I/O	Ground.
45	NYIOW	I/O	I/O write. Input during Master cycle.
46	NEBHE	I/O	High byte enable to expansion bus.
47	ADR0	I/O	Low byte enable. During a CPU cycle. A0 is latched with ALE.

Table 3-1 (1/2). FE3001 pin assign

PIN No.	SIGNAL	I/O	DESCRIPTION
48	NBHE	I/O	High byte enable from the 80286. Output during MASTER and DMA cycles for memory control use.
49	D6	I/O	Peripheral data bus bit 6.
50	D7	I/O	Peripheral data bus bit 7.
51	VDD2		+5V VDD.
52	D2	I	Peripheral data bus bit 2.
53	D3	I	Peripheral data bus bit 3.
54	NDMAMR	I	DMA memory read from DMA controller.
55	NRESIN	I	System reset input.
56	NRESCPU	I	CPU reset input from keyboard controller.
57	NMEMCS16	I	16 bit memory transfer on the PC/AT bus.
58	NIOCS16	I	16 bit I/O transfer on the PC/AT bus.
59	NZEROWS	I	Zero wait state bus cycle. See description for more details.
60	NONBRD	I	16 bit On Board DRAM memory or I/O device. Implies local memory on memory cycles and fast I/O bus timing for I/O cycles.
61	NMASTER	I	Master on PC bus has control of the bus.
62	IOCHRDY	I	Current bus cycle may complete. May be used to extend CPU. DMA, or refresh cycles.
63	NBUSY	I	80287 co-processor busy.
64	NERROR	I	Error from 80287.
65	Vss6		Ground.
66	HRO1	I	Hold request from DMA controller in FE3010B.
67	OUT1	I	Refresh timer input from FE3010.
68	HLDA	I	Hold acknowledge from 80286.
69	A0	I	Local 80286 address bus 0.
70	A1	I	Local 80286 address bus 1.
71	A3	I	Local 80286 address bus 3.
72	NCS287	I	80287 select decode (0FXH).
73	PTYERR	I	On board RAM parity error.
74	VDD3		+5V VDD.
75	NIOCHCK	I	Error from PC/AT bus.
76	NNMICS	I	NMI port enable decode (07XH). Also used for programming bus control registers.
77	NPBCS	I	Port B chip select decode (061H, 063H). See register description for decode definitions.
78	AEN	I	DMA cycle enable from FE3010.
79	DACK2	I	16 bit DMA acknowledge from FE3010B.
80	MNIO	I	80286 memory I/O select. High indicates memory cycle, low indicates I/O cycle.
81	NS1	I	80286 Status 1.
82	NS0	I	80286 Status 0.
83	CLK14	I	14.318 MHz clock input used to derive TMRCLK, PCLK and NPCLK.
84	CLK16	I	16 MHz clock input. This provides the low speed CPU clock for 8 MHz operation. When this pin is pulled high, CLKHS 2 is used as the low speed clock.

Table 3-1 (2/2). FE3001 pin assign

3-1-2-2. FE3010B: AT Peripheral Control Logic (IC107)

FE3010B has the functions of a DMA controller, an interrupt controller and a timer.

a) DMA controller
FE3010B has two DMA controllers which are compatible with 8237. The I/O address of the DMA controller #1 is 000 to 00FH. The DMA controller #1 is used for 8-bit DMA transfer. The I/O address of the DMA controller #2 is 0C0 to 0DEH. The DMA controller #2 is used for 16-bit DMA transfer. Channel 0 of the DMA controller #2 is used for cascade connection of the DMA controller #1.

b) Interrupt controller
FE3010B has two interrupt controllers which are compatible with 8259. The I/O address of the interrupt controller #1 is 020 to 021H. The I/O address of the interrupt controller #2 is 0A0 to 0A1. The interrupt 2 of the interrupt controller #1 is used for cascade connection of the interrupt controller #2.

System Interrupt	Interrupt Controller	Use
0	#1 Level 0	Timer
1	#1 Level 1	Keyboard
2	#1 Level 2	Cascade
3–7	#1 Level 3–7	AT Bus
8	#2 Level 0	R.T.C.
9–12	#2 Level 1–4	AT Bus
13	#2 Level 5	Co-Processor

Table 3-2.

c) Timer
FE3010B has a timer compatible with 8254. The 8254 has three independent counters, and the timer operates on a 1.19 MHz clock. The I/O address of the timer is 040 to 043H, that indicates the function of each channel and address.

Timer Channel	Use
0	Time of Day (Interrupt)
1	Refresh Request
2	Speaker

Table 3-3.

I/O Address	Use	Read/Write
040	Timer 0 Count/Status	Read/Write
041	Timer 1 Count/Status	Read/Write
042	Timer 2 Count/Status	Read/Write
043	Control Word	Write

Table 3-4.

d) PIO
FE3010B has ports for controlling the speaker and the timer channel. Also, FE3010B has a circuit for detecting whether the refresh function is operating. These are used to make software compatible with the IBM PC/AT. Port B (PIO) is a register for both the 8 bit control and status, and 0 to 5 bits are determined by FE3010B, but 6 and 7 bits are generated from FE3031.

PIN No.	SIGNAL	I/O	FUNCTION
1	Vss		GROUND.
2	DATA (0)	I/O	DATA BIT 0.
3	DATA (1)	I/O	DATA BIT 1.
4	DATA (2)	I/O	DATA BIT 2.
5	DATA (3)	I/O	DATA BIT 3.
6	DATA (4)	I/O	DATA BIT 4.
7	DATA (5)	I/O	DATA BIT 5.
8	DATA (6)	I/O	DATA BIT 6.
9	DATA (7)	I/O	DATA BIT 7.
10	HLDA	I	HOLD ACKNOWLEDGE. Active high. Acknowledge from the CPU (80286) for a request for the bus from the DMA controller.
11	DMARDY	I	DMA READY. Active high. Signal to indicate that the DMA may complete its current cycle.
12	DMACLK	I	DMA CLOCK. System clock/DMACLK. 6 MHz/3 or 6 MHz. 8 MHz/4 or 8 MHz. 10 MHz/5 MHz
13	NMASTER	I	BUS MASTER. Active low. Signal indicating a master on the expansion bus has bus control.
14	KBINT	I	KEYBOARD INTERRUPT. Active high.
15	IRQ3	I	INTERRUPT REQUEST 3. Active high.
16	IRQ4	I	INTERRUPT REQUEST 4. Active high.
17	IRQ5	I	INTERRUPT REQUEST 5. Active high.
18	IRQ6	I	INTERRUPT REQUEST 6. Active high.
19	IRQ7	I	INTERRUPT REQUEST 7. Active high.
20	INTR	O	INTERRUPT REQUEST TO CPU (80286). Active high.
21	OUT1	O	TIMER CHANNEL 1 OUTPUT.
22	Vss		GROUND.
23	TCLK	I	TIMER CLOCK (1.19 MHz clock for timer).
24	SPKR	O	SPEAKER DATA.
25	NTRQ8	I	INTERRUPT REQUEST 8. Active low.
26	IRQ9	I	INTERRUPT REQUEST 9. Active high.
27	IRQ10	I	INTERRUPT REQUEST 10. Active high.
28	IRQ11	I	INTERRUPT REQUEST 11. Active high.
29	IRQ12	I	INTERRUPT REQUEST 12. Active high.
30 to 39	AL (0 − 9)	I/O	ADDRESS BIT 0 − 9[NOTE].
40	AH (0)	O	ADDRESS BIT 10.
41	AH (1)	O	ADDRESS BIT 11.
42	Vss		GROUND.
43	VDD		+5 VOLTS SUPPLY.
44	AH (2)	O	ADDRESS BIT 12.
45	AH (3)	O	ADDRESS BIT 13.
46	AH (4)	O	ADDRESS BIT 14.
47	AH (5)	O	ADDRESS BIT 15.
48	AH (6)	O	ADDRESS BIT 16.
49	AH (7)	O	ADDRESS BIT 17.
50	AH (8)	O	ADDRESS BIT 18.
51	AH (9)	O	ADDRESS BIT 19.
52	AH (10)	O	ADDRESS BIT 20.
53	AH (11)	O	ADDRESS BIT 21.
54	AH (12)	O	ADDRESS BIT 22.
55	AH (13)	O	ADDRESS BIT 23.

NOTE

All addresses going in the FE3010B during CPU cycles are latched with ALE except for A0. This allows compatibility for 16-bit writes to the FE3010B, although 8-bit accesses are preferred.

Table 3-5 (1/2). FE3010B pin assign

PIN No.	SIGNAL	I/O	FUNCTION	
56	NRFSH	I	REFRESH ADDRESS. Signal to enable the refresh address to the address bus during a RAM refresh cycle.	Active low.
57	ALE	I	ADDRESS LATCH ENABLE.	Active high.
58	NRTCCS	O	REAL TIME CLOCK.	
59	NINTA	I	INTERRUPT ACKNOWLEDGE FROM CPU (80286). Interrupt acknowledge to the interrupt controllers.	Active low.
60	IRQ15	I	INTERRUPT REQUEST 15.	Active high.
61	IRQ14	I	INTERRUPT REQUEST 14.	Active high.
62	NIRQ13	I	INTERRUPT REQUEST 13. Error interrupt from (80287).	Active low.
63	NCLEAR	I	SYSTEM CLEAR.	Active low.
64	Vss		GROUND.	
65	DACK2	O	DMA ACKNOWLEDGE BIT 2.	
66	DACK1	O	DMA ACKNOWLEDGE BIT 1.	
67	DACK0	O	DMA ACKNOWLEDGE BIT 0.	
68	NDACKEN	O	DMA ACKNOWLEDGE ENABLE. Signal to enable DACK0, DACK1, and DACK2 decode.	Active low.
69	HRQ	O	DMA REQUEST TO CPU (80286).	Active high.
70	TC	O	DMA END OF OPERATION. Signal to indicate the DMA controller has finished its cycle.	Active high.
71	AEN	O	DMA AEN. Signal to indicate that the current bus is a DMA cycle.	Active high.
72	DRQ7	I	CHANNEL 7 DMA REQUEST.	Active high.
73	DRQ6	I	CHANNEL 6 DMA REQUEST.	Active high.
74	DRQ5	I	CHANNEL 5 DMA REQUEST.	Active high.
75	DRQ3	I	CHANNEL 3 DMA REQUEST.	Active high.
76	DRQ2	I	CHANNEL 2 DMA REQUEST.	Active high.
77	DRQ1	I	CHANNEL 1 DMA REQUEST.	Active high.
78	DRQ0	I	CHANNEL 0 DMA REQUEST.	Active high.
79	SYSALE	O	SYSTEM ALE. Signal to latch the address in the address latch.	Active high.
80	NIOR	I/O	I/O READ COMMAND.	Active low.
81	NIOW	I/O	I/O WRITE COMMAND.	Active low.
82	NMEMR	O	MEMORY READ COMMAND.	Active low.
83	NMEMW	O	MEMORY WRITE COMMAND.	Active low.
84	VDD		+5 VOLTS SUPPLY.	

DACK2	DACK1	DACK0	DMA Channel Acknowledge
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	illegal
1	0	1	5
1	1	0	6
1	1	1	7

Table 3-5 (2/2). FE3010B pin assign

3-1-2-3. FE3021: address buffer and memory controller (IC109)

FE3021 consists of a RAS/CAS generator for DRAM, an address multiplexer, a LIM 4.0 EMS expand memory circuit, a chip select generator for floppydisk drive controller/8742/BIOS ROM/NMI, a chip select generator for hard disk drive controller, printer I/O, RS232C (×2), an address/control signal buffer for driving the AT-Bus.

a) Memory control

There are four RAS, namely, RAS0 (pin 128), RAS1 (pin 129), RAS2 (pin 130) and RAS3 (pin 132). With them, four 16-bit memory banks can be controlled. CAS is available for both low byte and the other for high byte. CASL0 (pin 125), CASL1 (pin 125), CASL2 (pin 2) and CASL3 (pin 3) are for low byte applications, and CASH0 (pin 4), CASH1 (pin 5), CASH2 (pin 6) and CASH3 (pin 131) are for high byte applications.

During the refresh cycle, all RAS are made active, but CAS are not active. RAS and CAS lines can directly drive DRAM. It is bank 0 memory that is controlled by RAS0, CASL0, and CASH0. Similarly, bank 1 memory, bank 2 memory and bank 3 memory can be controlled, as shown in Table 3-6.

PIN No.	MNEMONIC	I/O	FUNCTION
128	RAS0–	O	RAS SIGNAL FOR DRAM MEMORY BANK 0
129	RAS1–	O	RAS SIGNAL FOR DRAM MEMORY BANK 1
130	RAS2–	O	RAS SIGNAL FOR DRAM MEMORY BANK 2
132	RAS3–	O	RAS SIGNAL FOR DRAM MEMORY BANK 3
125	CASL0–	O	CAS SIGNAL FOR DRAM MEMORY BANK 0. LOW BYTE
126	CASL1–	O	CAS SIGNAL FOR DRAM MEMORY BANK 1. LOW BYTE
2	CASL2–	O	CAS SIGNAL FOR DRAM MEMORY BANK 2. LOW BYTE
3	CASL3–	O	CAS SIGNAL FOR DRAM MEMORY BANK 3. LOW BYTE
4	CASH0–	O	CAS SIGNAL FOR DRAM MEMORY BANK 0. HIGH BYTE
5	CASH1–	O	CAS SIGNAL FOR DRAM MEMORY BANK 1. HIGH BYTE
6	CASH2–	O	CAS SIGNAL FOR DRAM MEMORY BANK 2. HIGH BYTE
131	CASH3–	O	CAS SIGNAL FOR DRAM MEMORY BANK 3. HIGH BYTE
18	REFR–	I	MEMORY REFRESH SIGNAL
43	CSPROM–	O	BIOS PROM SELECT
26	TAP2–	I	SECOND TAP OUTPUT OF RAS DELAY LINE
44	TAP1–	I	FIRST TAP OUTPUT OF RAS DELAY LINE
58	RAS–	O	TO RAS DELAY LINE INPUT
23	DBLE–	O	TO FE3031 MEMORY DATA BUS LATCH ENABLE
24	ADR0	I	FROM FE3001 BYTE CONVERSION

Table 3-6.

b) Memory address multiplexer

The memory address multiplexer generates a row address and column address for DRAM. This output requires the use of an external driver for driving the DRAM. IC110 (AM29827A) is an external driver for this purpose.

The memory address multiplexer is capable of supporting 64K, 256K, and 1M DRAMs. So, DRAMs of each capacity indicated above can be mixedly used for each bank. A switchover is done by software, and there is no need for jumpering the hardware section.

PIN No.	MNEMONIC	I/O	FUNCTION
31	RA0	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 0 (LSB)
32	RA1	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 1
33	RA2	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 2
34	RA3	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 3
35	RA4	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 4
36	RA5	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 5
37	RA6	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 6
38	RA7	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 7
39	RA8	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 8
41	RA9	O	MEMORY ADDRESS MULTIPLEXER OUTPUT BIT 9 (MSB)

Table 3-7.

c) I/O chip select generator

FE3021 outputs CS8042 (pin 60) for 8742 keyboard control, CSF (pin 49) for floppy disk controller, CSNMI (pin 20) for NMI, and CSPTB (pin 22) for port B. In addition, there are CS0 (pin 48), CS1 (pin 47), CS2 (pin 46) and CS3 (pin 45) as programmable chip select generators. On the SY-143 board, CS0 is set for selecting the channel 0 of RS232C, CS1 for the channel 1 of RS232C, CS2 for printer input and output, and CS3 for selecting the hard disk drive controller.

When CS3 is designed as a chip select generator for the hard disk driver controller, the operation register select (LDOR) generator for the floppy disk drive controller, configuration register select (LDCR) generator, floppy disk drive chip select (FCS) generator are created from CSF (pin 49) and CS3 (pin 45). The 1/3, 2/3 and 3/3 of IC111 (74ALS10) are the circuits for generating FCS (pin 12), LDCR (pin 6) and LDOR (pin 8).

PIN No.	MNEMONIC	I/O	FUNCTION
48	CS0–	O	PROGRAMMABLE CHIP SELECT 0
47	CS1–	O	PROGRAMMABLE CHIP SELECT 1
46	CS2–	O	PROGRAMMABLE CHIP SELECT 2
45	CS3–	O	PROGRAMMABLE CHIP SELECT 3 OR H.D.CONT. CHIP SELECT
49	CSF	O	FLOPPY DISK CONTROLLER CHIP SELECT OR OPERATION OR CONFIG. REGISTER SELECT
60	CS8042–	O	8042 KEYBOARD CONT. SELECT
56	CS287–	O	80287 COPROCESSOR SELECT
20	CSNMI–	O	NMI LOGIC CHIP SELECT
22	CSPTB–	O	MEMORY PARITY AND I/O CHECK CONTROL CHIP SELECT

Table 3-8.

OUTPUT SIGNAL	INPUT SIGNAL			
	CSF	$\overline{\text{CS3}}$	ADDR1	ADDR2
$\overline{\text{LDOR}}$	HIGH	HIGH	HIGH	X
$\overline{\text{LDCR}}$	HIGH	LOW	X	X
$\overline{\text{FCS}}$	HIGH	HIGH	X	HIGH

Table 3-9.

d) EMS memory

The EMS (Expanded Memory Specification) is the specification for the expanded memory to remove the restriction that the memory space controlled by MS-DOS is 640 Kbytes. FE3021 contains an EMS configuration register, an EMS control register and an EMS page register. So, the EMS memory can be used when a register is set from the EMS driver with the software, without any change or addition of an external circuit excepting the memory. On the SY-143 board, a 2 M-bytes memory can be additionally provided by an optional SMI5050, it is possible to use the EMS memory up to 2 Mbytes besides the 640 Kbyte main memory.

e) I/O control

FE3021 generates a control signal of I/O bus.

PIN No.	MNEMONIC	I/O	FUNCTION
127	IORDY	O	READY LINE, MODIFIED OPEN DRAIN
40	SELDA–	O	DIRECTION OF DATA TRANSCEIVER-DATA TO EDATA BUS
8	IOR–	I/O	SYSTEM I/O READ COMMAND SIGNAL, DRIVES EXPANSION BUS. AN INPUT IN MASTER MODE.
9	IOW–	I/O	SYSTEM I/O WRITE COMMAND SIGNAL, DRIVES EXPANSION BUS. AN INPUT IN MASTER MODE.
10	YMEMR–	I	UNGATED SYSTEM MEMORY READ COMMAND SIGNAL FROM FE3001
11	YMEMW–	I	UNGATED SYSTEM MEMORY WRITE COMMAND SIGNAL FROM FE3001
53	ADSTB	I	ADDRESS STROBE FROM FE3001 & FE3010B
12	YIOR–	I/O	UNGATED I/O READ STROBE FROM FE3001. AN OUTPUT IN MASTER MODE.
13	YIOW–	I/O	UNGATED I/O WRITE STROBE FROM FE3001. OUTPUT IN MASTER MODE.
19	FRES–	I/O	"HOT" RESET OUTPUT
25	LOMEG–	O	TO FE3031 MEMORY STROBE GATING
28	RESET–	I	MASTER RESET FOR FE3021
52	MASTER–	I	BUS MASTER SIGNAL FROM AT BUS
54	A20GT	I	FROM 8042. WHEN HIGH, A20IS UNGATED
57	ONBD–	O	TO FE3001. INDICATES HIGH SPEED ON-BOARD ACCESS
59	ADDR19	O	AT BUS SA19
61	ADDR18	O	AT BUS SA18
62	ADDR17	O	AT BUS SA17
64	ADDR16	I/O	AT BUS SA16
65	ADDR15	I/O	AT BUS SA15
66	ADDR14	I/O	AT BUS SA14
68	ADDR13	I/O	AT BUS SA13
69	ADDR12	I/O	AT BUS SA12
72	ADDR11	I/O	AT BUS SA11
73	ADDR10	I/O	AT BUS SA10
75	ADDR9	I/O	AT BUS SA9
94	ADDR8	I/O	AT BUS SA8
96	ADDR7	I/O	AT BUS SA7
97	ADDR6	I/O	AT BUS SA6
98	ADDR5	I/O	AT BUS SA5
100	ADDR4	I/O	AT BUS SA4
101	ADDR3	I/O	AT BUS SA3
104	ADDR2	I/O	AT BUS SA2
106	ADDR1	I/O	AT BUS SA1
105	ADDR0	I/O	AT BUS SA0
63	LA23	I/O	AT BUS LA23
70	LA22	I/O	AT BUS LA22
71	LA21	I/O	AT BUS LA21
93	LA20	I/O	AT BUS LA20
95	LA19	I/O	AT BUS LA19
102	LA18	I/O	AT BUS LA18
103	LA17	I/O	AT BUS LA17

Table 3-10.

3-1-2-4. FE3031: AT data buffer (IC103)

FE3031 has functions such as the peripheral data bus buffer, memory data bus buffer, PC/AT data bus buffer, and parity generator/checker of memory.

a) Data buffer and control

The EDATA Bus (peripheral data bus) is used for 8 bit data transfer between core logic ICs such as CPU and main memory and other peripheral chips (8742 keyboard controller, D1287 real time clock and VL16C452 serial/parallel I/O controller) on the SY-143 board.

The DATA Bus (PC/AT data bus) is used for 16 bit data transfer between core logics and chips (37C65B floppy disk controller, PVGA1A, VGA controller, and I/O for hard disk drive controller) linked with the AT-Bus on the SY-143, and the external card connected to AT-Bus connectors (CN108 and IC109). The MDATA Bus (memory data bus) is used for 16 bit data transfer between the main memory and the BIOS ROM and other chips on the SY-143 board.

b) Memory parity generator/checker

FE3031 has a parity generator/checker which compatible with 74280. The PLO (pin 55) and PHI (pin 56) are low byte and high byte inputs of 74280, respectively, and POLO (pin 20) and POHI (pin 100) are low byte and high byte outputs of 74280, respectively. PERROR (pin 79) is the Ram parity error output of 74280.

PIN No.	SIGNAL	I/O	FUNCTION
1 to 4	D (0:15)	I/O	80286 Local Data Bus.
6 to 9			
11 to 14			
16 to 19			
5, 15	Vss		Ground.
26, 36			
60, 65			
74, 83			
94			
10, 21	VDD		+5V VDD.
31, 41			
70, 78			
89, 99			
20	POLO	O	Low byte parity bit to the DRAMs.
22 to 25	DATA (0:15)	I/O	PC/AT Data Bus.
27 to 30			
32 to 35			
37 to 40			
42	DTR	I	Data direction for DATA buffers.
43	NDEN0	I	Low byte data enable to DATA buffers.
44	NDEN1	I	High byte data enable to DATA buffers.
45	ADR0	I	Address bit 0 for MDATA buffers and byte swap.
46	SCYCLE	I	Latch low byte during byte swap read.
47	NSDEN	I	Byte swap data buffer enable.
48	SDTR	I	Byte swap data direction to swap buffer.
49	ACK	I	DMA Acknowleadge signal to the PC/AT bus.
50	NSELDATA	I	EDATA bus enable.
51	NINTA	I	Interrupt scknowledge.
52	NABHE	I	High byte enable for MDATA bus.
53	NBUFDIS	I	Disable Buffers when low.
54	NDLE	I	Latch MDATA bus during a read.
55	PLO	I	Low byte parity bit from DRAMs.
56	PHI	I	High byte parity bit from DRAMs.
57	NONBRD16	I	NONBRD indicates a local DRAM operation.
58	NLOWMEG	I	NLOWMEG indicates access of low MB of memory.
59	NMASTER	I	Mster on PC bus has control of the bus.

Table 3-11 (1/2). FE3031 pin assign

PIN No.	SIGNAL	I/O	FUNCTION
61 to 64 66 to 69	EDATA (0:7)	I/O	Peripheral Data Bus for FE3001, FE3010B, RTC and Keyboard controller.
71	NSMEMR	O	Low 1 MB Memory Read to PC bus.
72	NSMEMW	O	Low 1 MB Memory Write to PC bus.
73	NMEMR	I/O	Memory read to/from AT bus.
75	NMEMW	I/O	Memory read to/from AT bus.
76	NYMEMR	I/O	Memory read to/from FE3001.
77	NYMEMW	I/O	Memory write to/from FE3001.
79	PERROR	O	RAM parity error.
80 to 82 84 to 88 90 to 93 95 to 98	MDATA (0:15)	I/O	Memory Data bus.
100	POHI	O	High byte parity bit to the DRAMs.

Table 3-11 (2/2). FE3031 pin assign

3-1-3. Main Memory Block (IC116 to IC127, CN116)

The main memory has bank 0 of 128 Kbytes and bank 1 of 512 Kbytes, or a total of 640 Kbyte capacity. Bank 0 consists of four 64-Kbit × 4 DRAMs (MB81464-15PSZ). IC122, IC123 forms a low byte memory of bank 0, and IC126 is a low byte parity memory. IC124, IC125 consist of high byte memory of bank 0. IC127 is a high byte parity memory. Bank 1 consists of four 256-Kbit × 4 DRAMs (MB81C4256-15 PSZ). IC116, IC117 forms a low byte memory of bank 1, and IC120 is a low byte parity memory. IC118, IC119 forms a high byte memory of bank 1, and IC121 is a high byte parity memory. In parity memory blocks IC120, IC121, IC126 and IC127, a 256-Kbit × 1 DRAM (MB81256-10PSZ) is used. To bank 2, a socket (CN116-1, CN116-2) is connected, so as to use it as 2 Mbyte EMS memory with an optional SMI-5050 mounted in. CN116-1 is a socket for low byte memory + parity bit of bank 2, and CN116-2 is a socket for high byte memory + parity bit of bank 2.

3-1-4. BIOS ROM (IC144, IC145)

The BIOS ROM consists of two μPD27C512-15 for 16 bit operation. The μPD27C512 is a 32K × 8 bits. So, the memory capacity is that of 64 Kbytes. In the case of the SY-143, system BIOS for system control block and VGA BIOS for VGA controller of the graphic control block, are written in it.

Address		
000000 07FFFF	Main Memory	Bank 1 (512 Kbyte)
080000 09FFFF	Main Memory	Bank 0 (128 Kbyte)
0A0000 0BFFFF	Video RAM	VGA RAM 64 Kbyte × 4 Bank (128 Kbyte × 4 Bank)
0C0000 0DFFFF		
0E0000 0EFFFF	VGA BIOS	PROM (128 Kbyte)
0F0000 0FFFFF	System BIOS	

Table 3-12. Memory address map

3-1-5. AT-Bus Block

In the IBM PC/AT, an FDD controller, an HDD controller and a graphic controller are supplied to each AT-Bus connector as an external card. In this equipment, however, an FDD controller and a graphic controller are incorporated in the SY-143 board for the purpose of cost reduction. Also, for labor-saving and cost reduction, a type having a built-in HDD controller is used in the HDD, and the SY-143 board has HDD I/O only.

1) 37C65B (IC137)
   37C65B contains a formatter/controller, a data separator, a write pre-compensation, a data rate selector, a clock generator, etc. to have all necessary functions between the bus of the host CPU and the FDD connector.

PIN No.	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	$\overline{\text{RD}}$	$\overline{\text{READ}}$	I	Control signal for transfer of data of status onto the data bus by the WD37C65.
2	$\overline{\text{WR}}$	$\overline{\text{WRITE}}$	I	Control signal for latching data from the bus into the WD37C65 Buffer Register.
3	$\overline{\text{CS}}$	$\overline{\text{CHIP SELECT}}$	I	Selected when 0 (low) allowing $\overline{\text{RD}}$ or $\overline{\text{WR}}$ operation from the host.
4	A0	ADDRESS LINE	I	Address line selecting data (–1) or status (–0) information. (A0-logic 0 during $\overline{\text{WR}}$ is illegal).
5	$\overline{\text{DACK}}$	$\overline{\text{DMA ACKNOWLEDGE}}$	I	Used by the DMA controller to transfer data from the WD37C65 onto the bus. Logical equivalent to $\overline{\text{CS}}$ and A0-1. In Special or PC AT mode, this signal is qualified by DMAEN from the Operations Register.
6	TC	TERMINAL COUNT	I	This signal indicates to WD37C65 that data transfer is complete. If DMA operational mode is selected for command execution, TC will be qualified by $\overline{\text{DACK}}$, but not in the programmed I/O execution. In PC AT or Special mode, qualification by $\overline{\text{DACK}}$ requires the Operations Register signal DMAEN to be logically true. Note also that in PC AT mode, TC will be qualified by $\overline{\text{DACK}}$, whether in DMA or non-DMA host operation. Programmed I/O in PC AT mode will cause an abnormal termination error at the completion of a command.
7-14	DB0 thru DB7	DATA BUS 0 thru DATA BUS 7	I/O	8-Bit, bi-directional, tri-state, data bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB).
15	DMA	DIRECT MEMORY ACCESS	O	DMA request for byte transfers of data. In special or PC AT mode, this pin is tri-state, enabled by the DMAEN signal from the Operations Register. This pin is driven in the Base mode.
16	IRQ	INTERRUPT	O	Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in base mode. In Special or PC AT mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register.
17	DCHGEN			Not connected.
18	$\overline{\text{LDOR}}$	$\overline{\text{LOAD OPERATIONS REGISTER}}$	I	Address decode which enables the loading of the Operations Register. Internally gated with $\overline{\text{WR}}$ creates the strobe which latches the data bus into the Operations Register.
19	$\overline{\text{LDCR}}$	$\overline{\text{LOAD CONTROL REGISTER}}$	I	Address decode which enables loading of the Control Register. Internally gated with $\overline{\text{WR}}$ creates the strobe which latches the two LSBs from the data bus into the Control Register.
20	RST	RESET	I	Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base mode, not PC AT or Special mode.
21	$\overline{\text{RDD}}$	$\overline{\text{READ DISK DATA}}$	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
22	$\overline{\text{XT2}}$	$\overline{\text{XTAL2}}$	O	XTAL oscillator drive output for 44 pin PLCC, Should be left floating it TTL inputs used at pin 23.
23	XT2	XTAL2	I	XTAL oscillator input used for non-standard data rates. It may be driven with a TTL level signal.
24	DRV	DRIVE TYPE	I	Drive type input indicates to the device that a two-speed spindle motor is used if logic is 0. In that case, the second clock input will never be selected and must be grounded.
25	$\overline{\text{XT1}}$	$\overline{\text{XTAL1}}$	O	XTAL oscillator drive output. Should be left floating it TTL inputs used at pin 26.
26	XT1	XTAL1	I	XTAL oscillator input requiring 16 MHz crystal. This oscillator is used for all standard data rates, and may be driven with a TTL level signal.

Table 3-13 (1/2). 37C65B pin descriptions

PIN No.	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
27	PCVAL	PRECOMPENSATION VALUE	I	PRECOMPENSATION VALUE select input. This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1–125 ns, Logic 0–187 ns.
28	HS	HEAD SELECT	O	High current drive (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic 1–side 0. Logic 0–side 1.
29	WE	WRITE ENABLE	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
30	WD	WRITE DATA	O	this HCD output is WRITE DATA. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
31	DIRC	DIRECTION	O	This HCD output determines the direction of the head stepper motor. Logic 1–outward motion. Logic 0–inward motion.
32	STEP	STEP PULSE	O	This HCD output issues an active low pulse for each track to track movement of the head.
33	DS1	DRIVE SELECT 1	O	This HCD output, when active low, is DRIVE SELECT 1 in PC AT mode, enables the interface in this disk drive. This signal comes from the Operations Register. In Base, or Special mode, this output is #1 of the four decoded Unit Selects, as specified in the device command syntax.
34	Vss	GROUND		Ground.
35	DS2	DRIVE SELECT 2	O	This HCD output, when active low, is DRIVE SELECT 2 in PC AT mode, enables the interface in this disk drive. This signal comes from the Operations Register. In Base or the Special mode, this output is #2 of the four decoded Unit Selects as specified in the device command syntax.
36	MO1, DS3	MOTOR ON 1, DRIVE SELECT 3	O	This HCD output, when active low, is MOTOR ON enable for disk drive #1, in PC AT mode. This signal comes from the Operations Register. In the Base or Special mode, this output is #3 of the four decoded Unit Selects as specified in the device command syntax.
37	MO2, DS4	MOTOR ON 2, DRIVE SELECT 4	O	This HCD output, when active low, is MOTOR ON enable for disk drive #2, in PC AT mode. This signal comes from the Operations Register. In the Base or Special mode, this output is #4 of the four decoded Unit Selects as specified in the device command syntax.
38	HDL	HEAD LOADED	O	This HCD output, when active low, causes the head to be loaded against the media in the selected drive.
39	RWC, RPM	REDUCED WRITE CURRENT, REVOLUTIONS PER MINUTE	O	This HCD output, when active low, causes a REDUCED WRITE CURRENT when bit density is increased toward the inner tracks, becoming active when tracks > 28 are accessed. This condition is valid for Base or Special mode, and is indicative of when write precompensation is necessary. In the PC AT mode, this signal will be active when CR0–1.
40	DCCHG	DCHG		Not connected.
41	WP	WRITE PROTECTED	I	This Schmidt Trigger (ST) input senses status from the disk drive, indicating active low when a diskette is WRITE PROTECTED.
42	TR00	TRACK 00	I	This ST input senses status from disk drive, indicating active low when the head is positioned over the outermost track, TRACK 00.
43	IDX	INDEX	I	This ST input senses status from the disk drive, indicating active low when the head is positioned over the beginning of a track marked by an index hole.
44	Vcc	+5 VDC		Input power supply.

Table 3-13 (2/2). 37C65B pin descriptions

2) HDD controller I/O (IC138 to IC142)

The HDD controller I/O consists of a 16 bits data buffer (IC138, IC139: 74LS245), address 0 to 2, HDD controller CS0, CS1, IOR, and IOW buffers (IC140: 74LS244). IC141 is a gate array for generating CE (pin 19 of IC138, IC139) and DIR (pin 1 of IC138, IC139) of the 16 bits data buffer for HDD controller CS0 and CS1 from ADDR 0 to 2, LADDR17 to 23, IOR, IOW and CSHD.

IC141 contains a logic circuit for generating CE (pin 19 of IC211, IC212) and DIR (pin 1 of IC211, IC212) of the 16 bits data buffer for the VGA controller from ADDR 0 to 2, LADDER 17 to 23, SMEMR, SMEMW, EBHE, and EDBUF.

PIN	SIGNAL NAME	DIR	DESCRIPTION
01	–HOST RESET	O	Reset signal from the Host system which is active low during power up and inactive thereafter.
02	GND	O	Ground between the drive and the Host.
03–18	+HOST DATA	I/O	16 bit bi-directional data bus between the host and the drive. The lower 8 bits, HD0–HD7, are used for register & ECC access. All 16 bits are used for data transfers.
19	GND	O	Ground between the drive and the Host.
20	KEY	N/C	An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable.
21	RSVD	N/C	A pin reserved for future use.
22	GND	O	Ground between the drive and the host.
23	–HOST IOW	O	Write strobe, the rising edge of which clocks data from the host data bus, HD0 through HD15, into a register or the data register of the drive.
24	GND	O	Ground between the drive and the host.
25	–HOST IOR	O	Read strobe, which when low enables data from a register or the data register of the drive onto the host data bus, HD0 through HD15. The rising edge of –HOST IOR latches data from the drive at the host.
26	GND	O	Ground between the drive and the host.
27	RSVD	N/C	A pin reserved for future use.
28	+HOST ALE	O	Host Address Latch Enable. A signal used to qualify the address lines. This signal is presently not used by the drive.
29	RSVD	N/C	A pin reserved for future use.
30	GND	O	Ground between the drive and the host.
31	–HOST IRQ14	I	Interrupt to the Host system, enabled only when the drive is selected, and the host activates the –IEN bit in the Digital Output register. When the –IEN bit is inactive high, or the drive is not selected, this output in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a Host read of the Status register or a write to the command register. This signal is a tri-state line with 10 ma drive capacity.
32	+HOST IO16	I	Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word. This line is tri-state line with 20 ma drive capacity.
34	+HOST PDIAG	I	Passed diagnostic. Output by the drive if it is strapped in the slave mode. EI not jumpered. Input to the drive if it is jumpered in the master mode EI. This low true signal indicates to a master that the slave has passed its internal diagnostic command. This line is only inactive high during execution of the diagnostic command. This line is a tri state line with 10 ma drive capability.
35, 33, 36	+HOST A0, A1, A2	O	Bit binary coded address used to select the individual registers in the task file.
37	–HOST CS0	O	Chip select decoded from the host address bus. Used to select some of the Host accessible registers.
38	–HOST CS1	O	Chip select decoded from the Host address bus. Used three of the registers in the Task File.
39	–HOST SLV/ACT	I	Signal from the drive used either to drive an active LED whenever the disk is being accessed or as an indication of a second drive present. (See the Customer Options section for further information.) When jumpered as –ACTIVE, this signal is active low when the drive is busy and has a drive capability of 20 ma. When jumpered as –SLAVE PRESENT signal, it is an indication of the presence of a second drive when low. In this state, it has a drive capability of 10 ma.
40	GND	O	Ground between the drive and the host.

Table 3-14. CN111 HDD interface pin assign

3-1-6. Peripheral Block

1) VL16C452 (IC133)
   VL16C452 has two channels of asynchronous serial I/O (RS232C) and one channel of Centronics type printer I/O. Channel 0 of RS232C is connected with the video disk player through CN114 to control of the play/search operations of this player.

   Channel 1 of RS232C is externally output through the line receiver of MC1489AM (IC134, IC135) and that of MC1488M (IC136), driver, and CN105. The design is so made that to CN105, the mouth is normally connected with BIOS in the started state when the power of the SY-143 board has been turned on.

Pin Number	Signal Name	Signal Description
37	–IOR	Input/Output Read Strobe: This is an active low input which causes the selected channel to output data to the data bus (DB0–DB7). The data output depends upon the register selected by the address inputs A0, A1, A2. chip select 0 (–CS0) selects UART #1, chip select 1 (–CS1) selects UART #2, and chip select 2 (–CS2) selects the line printer port.
36	–IOW	Input/Output Write Strobe: This is an active low input which causes data from the data bus (DB0–DB7) to be input to either UART or to the parallel port. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs (–CS0, –CS1, and –CS2) enable UART #1, UART #2, and the parallel port (respectively).
14 to 21	DB0 to DB7	Data Bits DB0–DB7: The Data Bus provides eight, three-state I/O lines for the transfer of data, control and status information between the VL 16C452 and the CPU. These lines are normally in a high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
35, 34, 33	A0, A1, A2	Address Lines A0–A2: The address lines select the internal registers during CPU bus operations.
4	CLK	Clock Input: The external clock input.
26, 10	SOUT0, SOUT1	Serial Data Outputs: These lines are the serial data outputs from the UARTs' transmitter circuitry. A mark (1) is a logic "one" (high) and space (0) is a logic "zero" (low). Each SOUT is held in the mark condition when the transmitter is disabled, Reset is true, the Transmitter Register is empty, or when in the Loop Mode.
28, 13	–CTS0, –CTS1	Clear to Send Inputs: The logical state of each-CTS pin is reflected in the CTS bit of the (MSR) Modem Status Register [CTS is bit 4 of the MSR, written MSR (4)] of each UART. A change of state in either CTS pin since the previous reading of the associated MSR causes the setting of DCTS [MSR (0)] of each Modem Status Register. When a CTS pin is active (low), the modem is indicating that data on the associated SOUT can be transmitted.
31, 5	DSR0, DSR1	Data Set Ready Inputs: The logical state of the DSR pins is reflected in MSR (5) of its associated Modem Status Register. DDSR [MSR (1)] indicates whether the associated DSR pin has changed state since the previous reading of the MSR. When a DSR pin is low, its modem is indicating that it is ready to exchange data with the associated UART.
25, 11	DTR0, DTR1	Data Terminal Ready Lines: Each DTR pin can be set (low) by writing a logic 1 to MCR (0), Modem Control Register bit 0 of its associated UART. This signal is cleared (high) by writing a logic 0 to the DTR bit [MCR (0)] or whenever a reset occurs. When active (low), the DTR pin indicates to the DCE that its UART is ready to receive data.
24, 12	–RTS0, –RTS1	Request to Send Outputs: The –RTS signal is an output on each UART used to enable the modem. An –RTS pin is set low by writing a logic 1 to MCR (1) bit 1 of its UARTs Modem Control Register. Both –RTS pins are reset high by Reset. When active, an –RTS pin indicates to the DCE that its UART has data ready to transmit. In half duplex operations, –RTS is used to control the direction of the line.

Table 3-15 (1/3). VL16C452 signal descriptions

Pin Number	Signal Name	Signal Description
30, 6	–RI0, –RI1	Ring Indicator Inputs: When low, –RI indicates that a telephone ringing signal has been received by the modem or data set. The –RI signal is a modem control input whose condition is tested by reading MSR (6) (RI) of each UART. The Modem Status Register output TERI [MSR (2)] indicates whether the RI input has changed from high to low since the previous reading of the MSR. If the interrupt is enabled [IER (3)=1] and RI changes from a high to low, an interrupt is generated.
1	–LPTOE	Line Printer Output Enable: This input signal enables the parallel line printer when it is low. When this signal is high, the pins of the line printer are held in a high-impedance state. This line may be tied to ground for normal line printer operation.
23, 40, 64	VCC	Power Supply: 5V ± 5%.
2, 7, 9, 22, 27, 42, 43, 54, 61	GND	Ground (0V): All pins must be tied to ground for proper operation.
29, 8	–RLSD0, –RLSD1	Receive Line Signal Detect: When active (low), –RLSD indicates that the data carrier has been detected by the modem or data set. –RLSD is a modem input whose condition can be tested by the CPU by reading MSR (7) (RLSD) of the Modem Status Register. MSR (3) (DRLSD) of the Modem Status Register indicates whether the –RLSD input has changed since the previous reading of the MSR. –RLSD has no effect on the receiver. If the –RLSD changes state with the modem status interrupt enabled, an interrupt is generated.
39	–RESET	Reset: When low, the reset input forces the VL 16C452 into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities.
45, 60	INT0, INT1	Serial Channel Interrupts: Each serial channel interrupt goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the interrupt Enable Register of its associated channel: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The interrupt is reset low upon appropriate service or a reset operation.
41, 62	SIN0, SIN1	Serial Data Inputs: The serial data inputs move information from the communication line or modem to the VL16C452 receiver circuits. A mark (1) is high, and a space (0) is low. Data on serial data inputs is disabled when operating in the loop mode.
32, 3, 38	–CS0, –CS1, –CS2	Chip Selects: Each Chip Select input acts as an enable for the write and read signals for the serial channels 0 (–CS0) and 1 (–CS1), –CS2 enables the the signals to the line printer port.
44	BDO	Bus Buffer Output: This active high output is asserted when either serial channel or the parallel port is selected as an output. This output can be used to control the system bus driver device (74LS245).
53 to 46	PD0 to PD7	Parallel Data Bits (0 to 7): These eight lines provide a byte-wide input or output port to the system. The eight lines are held in a high-impedance state when the port is not selected (–CS2 is high).
55	–STB	Line Printer Strobe: This I/O line provides communication between the VL16C452 and the line printer. When it is active low, it provides the line printer with a signal to latch the data currently on the parallel port.
56	–AFD	Line Printer Autofeed: This I/O line provides the line printer with an active low signal when continuous form paper is to be autofed to the printer.
57	–INIT	Line Printer Initialize: This I/O line provides the line printer with a signal that allows the line printer initialization routine to be started.

Table 3-15 (2/3). VL16C452 signal descriptions

Pin Number	Signal Name	Signal Description
58	–SLIN	Line Printer Select: This I/O line selects the printer when it is active low.
59	INT2	Interrupt Printer Port: This signal is an input line from the line printer that goes active high when an error signal is received. The interrupt is reset low upon a reset operation.
63	–ERROR	Line Printer Error: This is an input line from the line printer. The line printer reports an error by holding this line low during the error condition. This causes INT2 to be asserted high.
65	SLCT	Line Printer Selected: This is an input line from the line printer that goes high when the line printer has been selected.
66	BUSY	Line Printer Busy: This is an input line from the line printer that goes high when the line printer has a local operation in progress.
67	PE	Line Printer Paper Empty: This is an input line from the line printer that goes high when the printer runs out of paper, and causes INT2 to be asserted high.
68	–ACK	Line Printer Acknowledge: This input goes low to indicate a successful data transfer has taken place.

Table 3-15 (3/3). VL16C452 signal descriptions

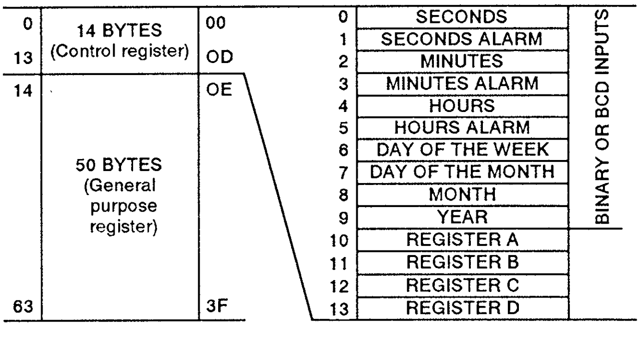
2) DS1287 (IC131)

DS1287 is a real time clock containing a lithium battery, a crystal oscillator, and a support circuit. It counts the seconds, minutes, hours, day, week, month, and year and makes non-volatile operation for about ten years without an external power supply. It also has a 64 bytes SRAM so that 14 bytes can be used for the clock control register and that 50 bytes for the general-purpose register.

PIN No.	Name	Description
4 to 11	AD0 to AD7	Multiplexed Address/Data Bus
2, 3, 16, 20 to 22	N.C.	No Connection
1	MOT	Bus Type Selection
13	$\overline{CS}$	Chip Select
14	AS	Address Strobe
15	R/$\overline{W}$	Read/Write Input
17	DS	Data Strobe
18	$\overline{RESET}$	Reset Input
19	$\overline{IRQ}$	Interrupt Request Output
23	SQW	Square Wave Output
24	Vcc	+5 Volt Supply
12	GND	Ground

Table 3-16. DS1287 pin assign

When MOT (pin 1) is connected to Vcc, it becomes the Motorola bus timing or when GND or open, it becomes the Intel bus timing. AD0 to AD7 (pins 4 to 11) are multiplexed bidirectional address/data bus, and address is given at the 1st part of the bus cycle, and data given at the 2nd part. At the rising edge of AS (Address Strobe:pin 14), the bus is demultiplexed; at the falling edge of the AS, address is latched to DS1287. As the CPU is Intel 80286 on the SY-143 board, it becomes the Intel bus. In the Intel bus, DS (pin 17) is called $\overline{RD}$, and operates as output enable, and the R/W (pin 15) is called $\overline{WR}$, and operates as write enable. $\overline{CS}$ (pin 13) is a chip select. It requires to keep $\overline{CS}$ active while $\overline{RD}$ and $\overline{WR}$ are active. $\overline{IRQ}$ (pin 19) is an output for requesting the CPU for an interrupt, and $\overline{RESET}$ (pin 18) an input for resetting plugs associated with the interrupt. RESET does not affect the clock, calendar, and SRAM.



0 13	14 BYTES (Control register)	00 OD
14 63	50 BYTES (General purpose register)	OE 3F

0	SECONDS	BINARY OR BCD INPUTS
1	SECONDS ALARM	
2	MINUTES	
3	MINUTES ALARM	
4	HOURS	
5	HOURS ALARM	
6	DAY OF THE WEEK	
7	DAY OF THE MONTH	
8	MONTH	
9	YEAR	
10	REGISTER A	
11	REGISTER B	
12	REGISTER C	
13	REGISTER D	

Table 3-17. address map DS1287

3-2. GRAPHIC CONTROL BLOCK

3-2-1. General

The graphic control block is mounted in the SY-143 board. This block can be divided into the VGA (Video Graphics Array) block and the VGA S/I (superimpose) block. Although VRAM on the VGA block is a memory with 256 Kbyte, it is possible to extend to 512 Kbyte by using an optional board.

- Flow of Video Signal

  The video signal fed from the video disk player section to the VS-39 board is separated into Y and C and decoded into R, G, and B signal components. Each signal is A/D converted into 6 bits and input into IC221, IC222, IC223 line memory. Write in the line memory is made at half the frequency of the dot clock, the double speed conversion is made by reading at the dot clock frequency. As a result, one and the same line is read twice consecutively, and the signal becomes 1 field 525 raster fH = 31.5 kHz. In this way, the video signal is made the same format as the signal of computer graphics. This signal is superimposed by a switchover with the CG picture using the selector mounted in IC228.

- Flow of CG Signal

  The CR controller mounted in IC213 (PVGA1A) creates the CG picture display timing based on the clock input to VCLKO (or VCLK1, VCLK2). Data read from IC201 to 208 VRAM is converted into the address* of the color palette RAM by a graphic controller and an attribute controller in IC213. The color palette RAM is a memory with 6 bits each of R, G, and B, or a total of 18 bits × 256. A maximum of 256 color data can be derived by reading the 18 bits color information written in advance.

  (Note: This corresponds to PIX address in the block diagram.)

  The CG (computer graphics) signals and video signals are superimposed one on the other by selecting this data and the video signal from the VS-39 board in IC228 with the key signal. The R, G, and B signals with 6 bits each, which are the outputs of the selector, are converted into analog signals by a D/A converter consisting of IC233, IC234, and IC235 for output to the monitor screen.

- Superimpose Key Signal

  There are two methods available for generating a key signal necessary for superimposition. One is the method of generating a key signal by specifying in advance the address of the CG color palette RAM desired to be made transparent and making the data that coincides with the PIX address fed from the VGA card transparent. The other is the method of making the data (from which this bit is output) transparent with the key bit (1 bit) written in the color palette RAM in advance together with the color data. As described above, the superimposing method is either that based on the coincidence of PIX address or that using the key bit, but in addition there is another mode in which it is based on the video only display or on the computer only display. Also, in the superimposition by PIX address, colors 0 to 1 out of a maximum of 256 colors can be made transparent, and in the superimposition by key bit, 0 to N (256 max.) colors out of those being displayed can be made transparent. The selector in IC228 selects a video signal when the key signal is output, and then outputs it to the D/A converter.

- Genlock Block

  To superimpose the video picture and CG picture, it is necessary to synchronize them. The video signal from the video disk player is separated into H sync ($\overline{\text{VSH}}$) and V sync ($\overline{\text{VSV}}$) by the sync separator circuit on the VS-39 board. The H sync is then stabilized through the AFC (Auto Frequency Control) circuit and fed to the SY-143 board via CN115. In IC224, a PLL (Phase Locked Loop) circuit is incorporated.

  In IC224, therefore, phase of the video V. sync/video H. sync are compared with the video V. sync/H. sync created by IC213 (PVGA1A), and an error detected by an IC220 phase detector is passed through a low-pass filter, and voltage is applied to the VCO (Voltage Controlled Oscillator) to generate a dot clock.

  In the genlock mode, the video CLK of IC213 (PVGA1A) selects VCLK2, inputs DOT clock received from the VCO, to generate H sync, V sync, and PIX address in synchronization with it.

- Monitor

  Analog R, G, and B signals, and H sync and V sync are output from CN110. As a monitor set, CPD-1303 (or CPD-1302), which is a multi-scan monitor set capable of accepting the input of analog R, G, and B signals can be used. (The cable used is a mini D-sub 15 pin ↔ D-sub 9 pin cable: Type CTG-PSII)

  Note: When using CPD-1303 (or CPD-1302), set the switch at the rear to ANALOG position. If it kept set to DIGITAL position, no image display is made.

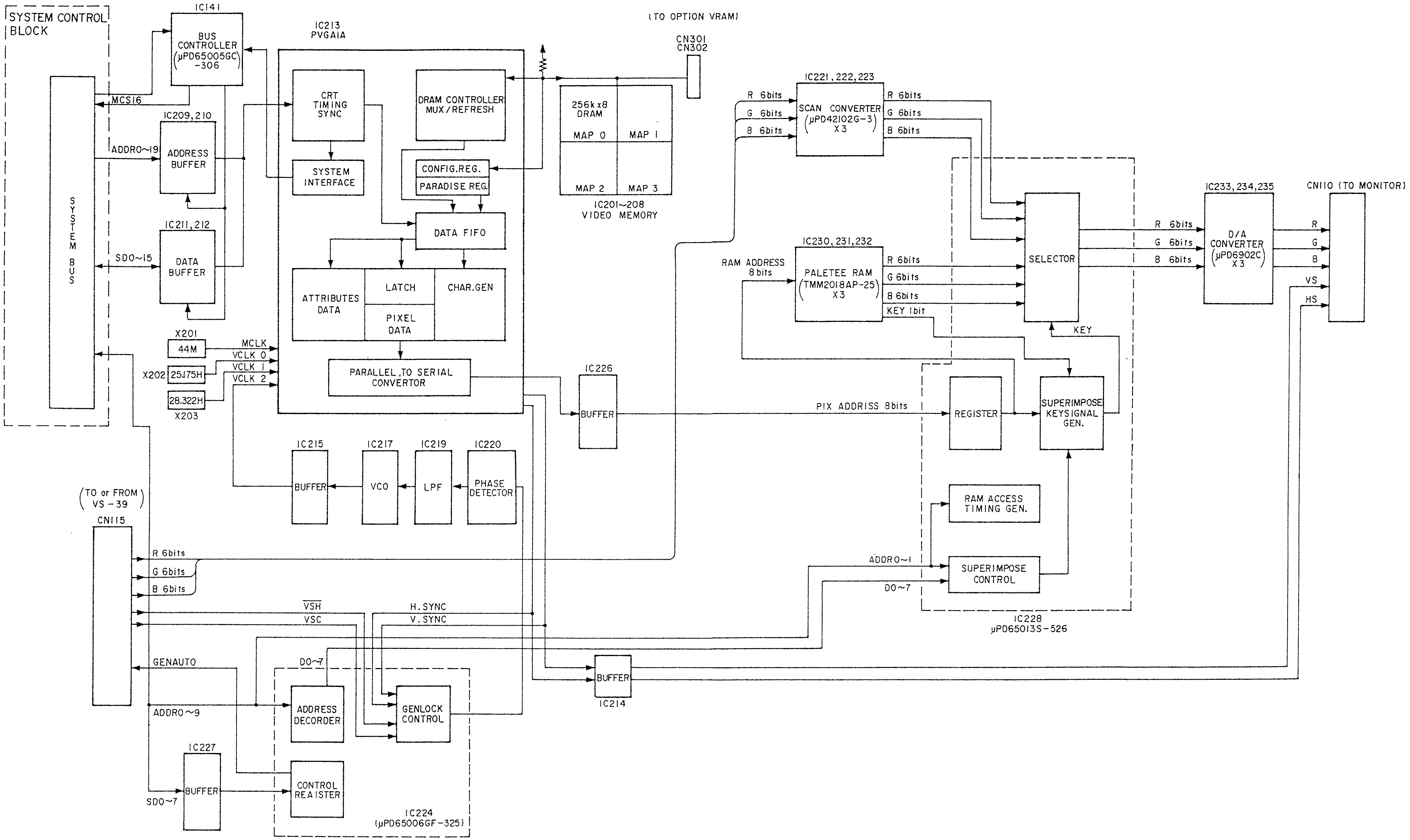

SYSTEM CONTROL BLOCK
SYSTEM BUS
MCS16
ADDR0~19
SD0~15
IC141
BUS CONTROLLER (μPD65005GC -306)
IC209, 210
ADDRESS BUFFER
IC211, 212
DATA BUFFER
X201
44M
X202
25.175H
28.322H
X203
MCLK
VCLK 0
VCLK 1
VCLK 2
IC213
PVGA1A
CRT TIMING SYNC
DRAM CONTROLLER MUX/REFRESH
SYSTEM INTERFACE
CONFIG.REG.
PARADISE REG.
DATA FIFO
ATTRIBUTES DATA
LATCH
CHAR.GEN
PIXEL DATA
PARALLEL TO SERIAL CONVERTOR
(TO OPTION VRAM)
CN301
CN302
256k x 8 DRAM
MAP 0
MAP 1
MAP 2
MAP 3
IC201~208
VIDEO MEMORY
IC226
BUFFER
IC215
BUFFER
IC217
VCO
IC219
LPF
IC220
PHASE DETECTOR
(TO or FROM VS-39)
CN115
R 6bits
G 6bits
B 6bits
VSH
VSC
H.SYNC
V.SYNC
GENAUTO
D0~7
ADDR0~9
ADDRESS DECORDER
GENLOCK CONTROL
IC227
BUFFER
SD0~7
CONTROL REAISTER
IC224
(μPD65006GF-325)
IC214
BUFFER
IC221, 222, 223
R 6bits
G 6bits
B 6bits
SCAN CONVERTER (μPD42102G-3) X3
R 6bits
G 6bits
B 6bits
RAM ADDRESS 8bits
IC230, 231, 232
PALETEE RAM (TMM2018AP-25) X3
R 6bits
G 6bits
B 6bits
KEY 1bit
SELECTOR
KEY
PIX ADDRISS 8bits
REGISTER
SUPERIMPOSE KEYSIGNAL GEN.
RAM ACCESS TIMING GEN.
ADDR0~1
D0~7
SUPERIMPOSE CONTROL
IC228
μPD65013S-526
R 6bits
G 6bits
B 6bits
IC233, 234, 235
D/A CONVERTER (μPD6902C) X3
CN110 (TO MONITOR)
R
G
B
VS
HS

Fig. 3-2. Graphics control block diagram

3-2-2. VGA Block

3-2-2-1. VGA (Video Graphics Array) IC: PVGA1A (IC213)

a) VGA

VGA is adopted by IBM Corp. in Model 50/60/80 of Personal System/2 (PS/2) as a display for personal computers. It consists of several custom LSI on the system board (mother board). In VIW-5000, VGA compatible chip PVGA1A manufactured by Paradise Systems, Inc. is used. Comparison between IBM VGA and PVGA1A is given in the accompanying table below.

Item		IBM VGA	PVGA1A
Compatibility	VGA	Register level	Register level
	MCGA	BIOS level	BIOS level
	EGA	BIOS level	BIOS level
	CGA	Register level	Register level
	Hercules	Not provided	Register level
Data bus • Interface	16 bits	Provided	Provided
	8 bits	Provided	Provided
Expansion color • Graphics	640 × 480 pixels/256 colors	Not provided	Provided
Number of chips		1	1
Clock (max.)		28 MHz	44.5 MHz

Table 3-18. Comparison between IBM VGA and PVGA1A

b) Package

100-pin PLCC (Plastic Leadless Chip Carrier) package.

c) PVGA1A pin descriptions

No.	Pin Name	I/O	Description	
1	VSS	—	GND	
2	MD4	I/O	Display memory data or PR5 register*[2] bit 4 upon power up	
3	MD3	I/O	Display memory data or configuration register*[2] bit 3 upon power up	
4	MD2	I/O	Display memory data or configuration register*[2] bit 2 upon power up	
5	MD1	I/O	Display memory data or PR1 register*[2] bit 1 upon power up	
6	MD0	I/O	Display memory data or PR1 register*[2] bit 0 upon power up	
7	EBROMN	O	Enable BIOS ROM.	Active low*[1]
8	DS16N	O	Programmable enable 16 bit word transfer.	Active low
9	BHEN	I	Bus high byte enable.	Active low
10	ROM16N	O	Card select feedback during memory or I/O access.	Active low.
11	EABUFN	O	Enable processor data buffer.	Active low.
12	DA8	I/O	Multiplexed data/address bus bit 8	
13	DA9	I/O	Multiplexed data/address bus bit 9	
14	DA10	I/O	Multiplexed data/address bus bit 10	
15	VSS	—	GND	
16	DA11	I/O	Multiplexed data/address bus bit 11	
17	DA12	I/O	Multiplexed data/address bus bit 12	
18	DA13	I/O	Multiplexed data/address bus bit 13	
19	DA14	I/O	Multiplexed data/address bus bit 14	
20	DA15	I/O	Multiplexed data bit 15 with Monitor type input	
21	EMEM	I	Enable display memory.	Active high*[1]
22	A15	I	Address bus bit 15	
23	A16	I	Address bus bit 16	
24	A17	I	Address bus bit 17	
25	VDD	—	+5 Vdc	

Table 3-19 (1/3).

No.	Pin Name	I/O	Description
26	VSS	—	GND.
27	A18	I	Address bus bit 18.
28	A19	I	Address bus bit 19.
29	IORN	I	I/O Read Strobe. Active low.
30	IOWN	I	I/O write strobe. Active low.
31	MRDN	I	Display memory read strobe. Active low.
32	MWRN	I	Display memory write strobe. Active low.
33	EION	I	Programmable enable. I/O. Active low or high^{*2}.
34	IORDY	O	A tri-state active high ready output to signal processor that memory access is available.
35	IRQ	O	Programmable processor interrupt request. Active low or high with tri-state.
36	RSET	I	Active high signal from external circuit during power up.
37	DIR	O	Directional control for processor data bus. Bits 0 through 15 high for read cycles.
38	EDBUFN	O	Enable processor data buffer. Active low.
39	DA0	I/O	Multiplexed data/address bus bit 0.
40	DA1	I/O	Multiplexed data/address bus bit 1.
41	DA2	I/O	Multiplexed data/address bus bit 2.
42	DA3	I/O	Multiplexed data/address bus bit 3.
43	DA4	I/O	Multiplexed data/address bus bit 4.
44	DA5	I/O	Multiplexed data/address bus bit 5.
45	DA6	I/O	Multiplexed data/address bus bit 6.
46	DA7	I/O	Multiplexed data/address bus bit 7.
47	RPLTN	O	0Read color look up palette. Active low (not used).
48	VID7	O	Video color look up table address bit 7.
49	VID6	O	Video color look up table address bit 6.
50	VID5	O	Video color look up table address bit 5.
51	VSS	—	GND.
52	VDD	—	+5 Vdc.
53	VID4	O	Video color look up table address bit 4.
54	VID3	O	Video color look up table address bit 3.
55	VID2	O	Video color look up table address bit 2.
56	VID1	O	Video color look up table address bit 1.
57	VID0	O	Video color look up table address bit 0.
58	WPLTN	O	Write color look up palette. Active low (not used).
59	PCLK	O	Pixel clock.
60	HSYNC	O	Color monitor horizontal synchronization pulse.
61	VSYNC	O	Color monitor vertical synchronization pulse.
62	BLNKN	O	Color monitor blank pulse. Active low.
63	MA8	O	Display memory multiplexed RAS/CAS address bit 8.
64	VSS	—	GND.
65	MA7	O	Display memory multiplexed RAS/CAS address bit 7.
66	MA6	O	Display memory multiplexed RAS/CAS address bit 6.
67	MA5	O	Display memory multiplexed RAS/CAS address bit 5.
68	MA4	O	Display memory multiplexed RAS/CAS address bit 4.
69	MA3	O	Display memory multiplexed RAS/CAS address bit 3.
70	MA2	O	Display memory multiplexed RAS/CAS address bit 2.
71	MA1	O	Display memory multiplexed RAS/CAS address bit 1.
72	MA0	O	Display memory multiplexed RAS/CAS address bit 0.
73	VCLK2	I/O	User defined external clock input.
74	VCLK1	I/O	28.322 MHz clock input.
75	VCLK0	I/O	25.175 MHz reference clock input.
76	MCLK	I	Up to 44.5 MHz for 100 ns DRAMS.
77	VSS	—	GND.
78	VDD	—	+5 Vdc.

Table 3-19 (2/3).

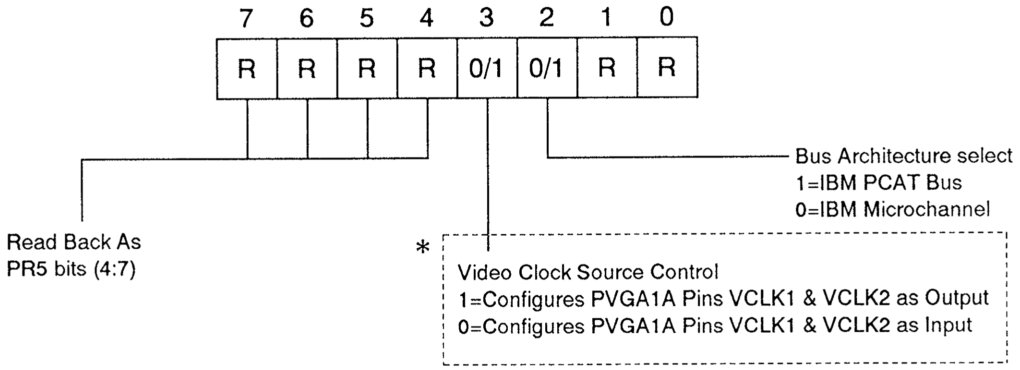
No.	Pin Name	I/O	Description
79	RAS10N	O	Row address strobe bank 0.(Memory Maps 1 & 0) Active low
80	CAS10N	O	Column address strobe bank 0. Active low
81	OE10N	O	Output enable bank 0. Active low
82	RAS32N	O	Row address strobe bank 1.(Memory Maps 3 & 2). Active low
83	CAS32N	O	Column address strobe bank 1. Active low
84	OE32N	O	Output enable bank 1. Active low
85	WE0N	O	Write enable bank 0 lower byte.(Memory map 0) Active low
86	WE1N	O	Write enable bank 0 upper byte.(Memory map 1) Active low
87	WE2N	O	Write enable bank 1 lower byte.(Memory map 2) Active low
88	WE3N	O	Write enable bank 1 upper byte.(Memory map 3) Active low
89	MD15	I/O	Display memory data bit 15.
90	MD14	I/O	Display memory data bit 14.
91	MD13	I/O	Display memory data bit 13.
92	MD12	I/O	Display memory data bit 12.
93	MD11	I/O	Display memory data bit 11.
94	MD10	I/O	Display memory data bit 10.
95	MD9	I/O	Display memory data bit 9.
96	MD8	I/O	Display memory data bit 8.
97	MD7	I/O	Display memory data or PR5*2 register bit 7 upon power up.
98	MD6	I/O	Display memory data or PR5*2 register bit 6 upon power up.
99	MD5	I/O	Display memory data or PR5*2 register bit 5 upon power up.
100	VDD	—	+5 Vdc.

Note: *1 EBROMN: In AT mode, addresses (C6000 to C67FF) are mapped out. Write strobe for I/O port $46E8 in AT mode.

*2 PR1=PARADISE REGISTER 1 MEMORY SIZE port 3CF 0B
PR5=PARADISE REGISTER 5 LOCK/STATUS port 3CF 0F
Configuration register=PVGA1A CONFIGURATION BITS CNF (2:3)
CNF (2:3) is a NON-READ/NON-WRITE PORT.
CNF (2:3), PR1 (0:1), and PR5 (4:7) are set by pull up or pull down of resistors (R304 to R311), which are connected to MD (0:7) (Pins 6 to 2, 99 to 97).

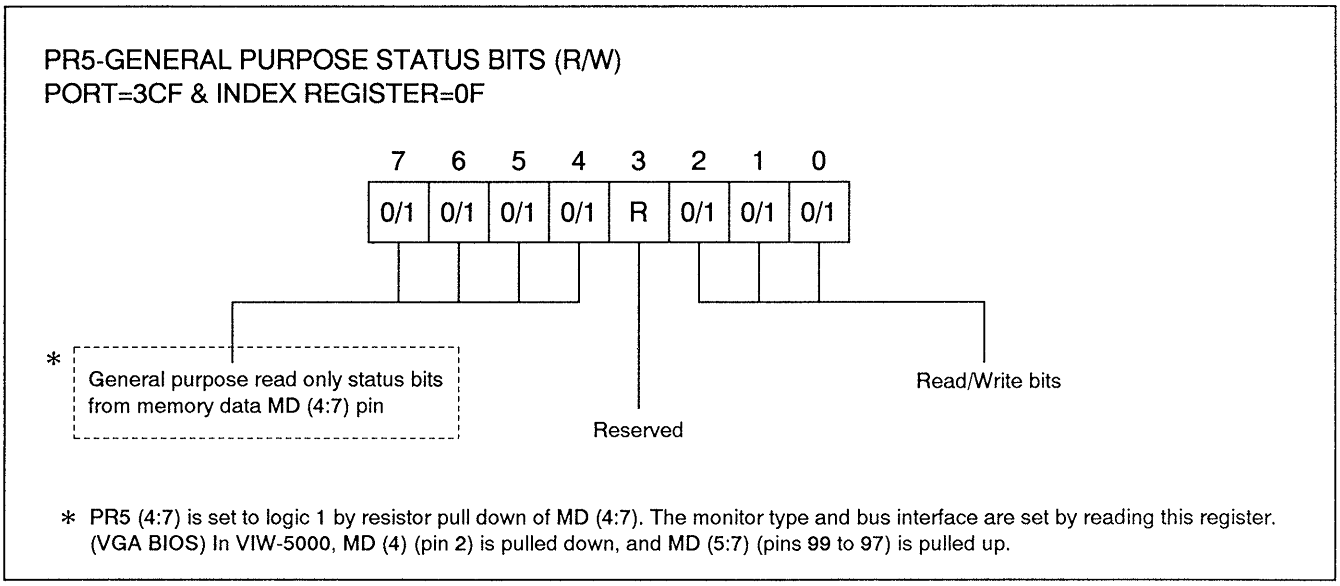
Table 3-19 (3/3).

PVGA1A CONFIGURATION REGISTER CNF (2:3)


7 6 5 4 3 2 1 0
R R R R 0/1 0/1 R R
Bus Architecture select
1=IBM PCAT Bus
0=IBM Microchannel
Read Back As
PR5 bits (4:7)
*
Video Clock Source Control
1=Configures PVGA1A Pins VCLK1 & VCLK2 as Output
0=Configures PVGA1A Pins VCLK1 & VCLK2 as Input

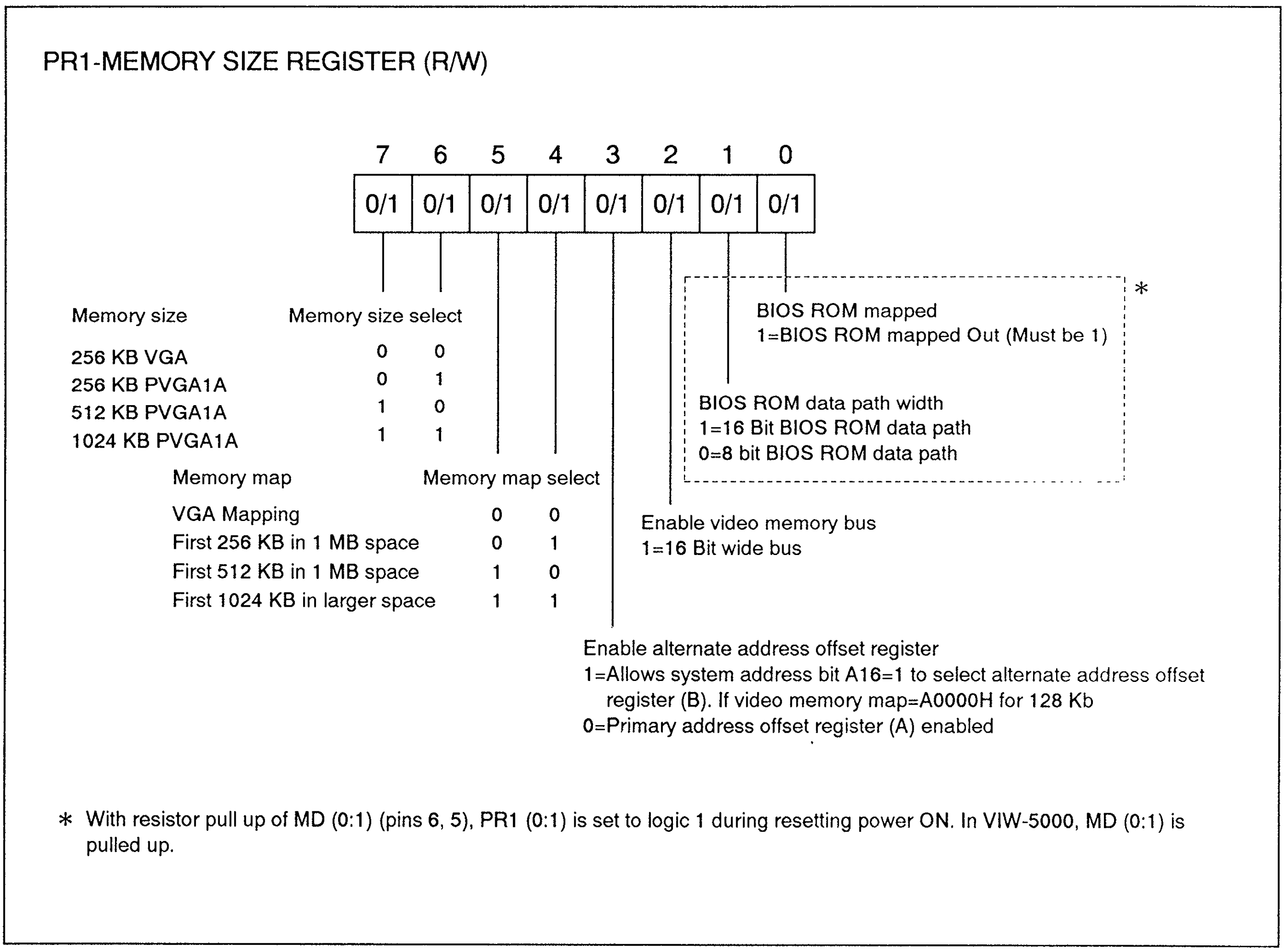
* CNF (2:3) internally latches MD (2:3) connected by pull up or pull down resistor at the time of power ON resetting. During pull up, it is set to logic 1. In VIW-5000, MD (2) is pulled up, and MD (3) is pulled down, being set to logic 0. Also when CNF (2:3) is latched after power ON, it cannot be subjected to read/write operations. But CNF (4:7) can be read by PR5 bits (4:7) even after power ON.

Fig. 3-3.


PR5-GENERAL PURPOSE STATUS BITS (R/W)
PORT=3CF & INDEX REGISTER=0F
7 6 5 4 3 2 1 0
0/1 0/1 0/1 0/1 R 0/1 0/1 0/1
*
General purpose read only status bits from memory data MD (4:7) pin
Reserved
Read/Write bits

* PR5 (4:7) is set to logic 1 by resistor pull down of MD (4:7). The monitor type and bus interface are set by reading this register. (VGA BIOS) In VIW-5000, MD (4) (pin 2) is pulled down, and MD (5:7) (pins 99 to 97) is pulled up.

Fig. 3-4.


PR1-MEMORY SIZE REGISTER (R/W)
7 6 5 4 3 2 1 0
0/1 0/1 0/1 0/1 0/1 0/1 0/1 0/1
*

Memory size	Memory size select	
256 KB VGA	0	0
256 KB PVGA1A	0	1
512 KB PVGA1A	1	0
1024 KB PVGA1A	1	1

Memory map	Memory map select	
VGA Mapping	0	0
First 256 KB in 1 MB space	0	1
First 512 KB in 1 MB space	1	0
First 1024 KB in larger space	1	1

BIOS ROM mapped
1=BIOS ROM mapped Out (Must be 1)

BIOS ROM data path width
1=16 Bit BIOS ROM data path
0=8 bit BIOS ROM data path

Enable video memory bus
1=16 Bit wide bus

Enable alternate address offset register
1=Allows system address bit A16=1 to select alternate address offset register (B). If video memory map=A0000H for 128 Kb
0=Primary address offset register (A) enabled

* With resistor pull up of MD (0:1) (pins 6, 5), PR1 (0:1) is set to logic 1 during resetting power ON. In VIW-5000, MD (0:1) is pulled up.

Fig. 3-5.

d) AT bus interface

PVGA1A is so designed that data bus and address bus are multiplexed (DA0 to 15). Therefore, it controls IC209/IC210 and IC211/IC212 with the EDBFN, EABFN and DIR signals, to prevent data bus and address bus from coming into contact with each other. Also, during VRAM read/write, it sends $\overline{\text{MEMCS16}}$ to the CPU to cause its cycle to be 1 wait, 16 bit memory cycle. The EDBFN ($\overline{\text{EDBUF}}$), DIR (VDIRR) and DS16N ($\overline{\text{DS16}}$) signals are gated with signals needed in IC141 gate array μPD65005GC-306-3B6, to generate $\overline{\text{EDBOF0}}$, $\overline{\text{EDBUF1}}$, VDIRW and $\overline{\text{MEMCS16}}$. The internal block diagram of IC141 is shown in Fig. 3-6.

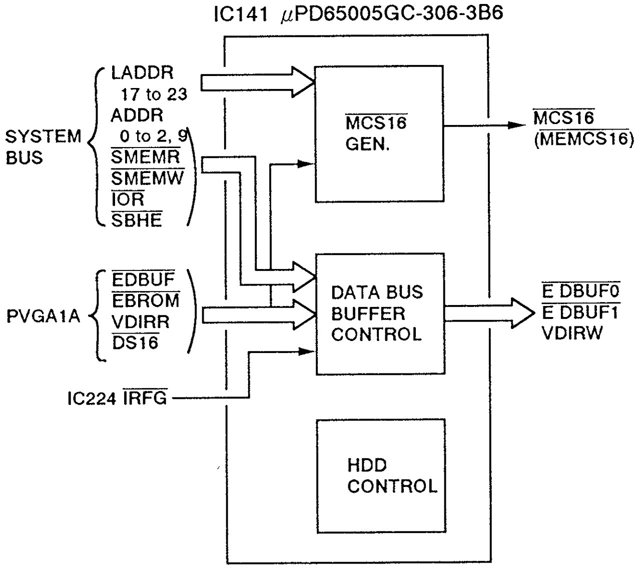


Fig. 3-6.

e) CLK selector

PVGA1A contains VCLK0, VCLK1 and VCLK2 as a video clock inputs. To VCLK0, a 25.175 MHz crystal oscillator is connected, and to VCLK1, a 28.322 MHz crystal oscillator is connected. Also, To VCLK2, a clock from IC217 is input. As the CLK from IC217 is synchronized with the external video signal, both the external video signal and VGA display can be genlocked. VCLK0 to 2 selection is made inside PVGA1A for control by bits 3. 2 of the I/O port 3C2 miscellaneous output register (R/W port).

bit3	Bit2	clock Select
0	0	25.175 MHz clock (640 Horizontal PELs)
0	1	28.322 MHz clock (720 Horizontal PELs)
1	0	VCO clock (from IC217 approx. 25.5 to 32.5 MHz
1	1	Reserved

Table 3-20. Clock select 3C2 (bit3, 2)

f) Monitor support

In VIW-5000, only the color mode of PVGA1A display modes is supported. Therefore, pin 8 of the address buffer IC210 is pulled up. This pin (DA15) is read by BIOS during power ON, and display mode 3+ is set.

g) Video memory

In VIW-5000, there are 64 Kbyte four planes, as provided by using eight of 64K × 4 bit DRAM (MBM81464), or a total capacity of 256 Kbytes. By further adding an expansion VRAM (optional), it can be expanded up to 512 Kbytes.

When the capacity is expanded to 512 KB, the display mode 5F (640 × 480 pixels, 256 colors) can be used.

The display memory is mapped in the 128 KB of host memory address space between A0000H to BFFFFH.

In the display mode 5F, 640 × 480=307,200 bytes are linearly used. But the CPU can handle only 64 Kbytes of address space. For this reason, in the display mode 5F, a bank switchover of a kind is made by using the Paradise register PROA (Address offset register A) and PROB (address offset register B) to make it possible to handle the video memory in the address space of 64 Kbytes.

Read from, and write to, VRAM from the CPU is made possible with 1 wait, 16 bit access by sending $\overline{\text{MEMCS16}}$ to the CPU.

h) Color palette RAM port

The color palette performs read/write of IC230 to IC232 TMM2018AP-25. In PVGA1A, the color palette read/write port is internally decoded to provide a data bus. But in VIW-5000, the color palette read/write is controlled by IC224. Therefore, IC211 and IC227 are caused to be open at the same time, and data bus SD0 to 7 collide when reading. Therefore, (ports 3C6 to 3C8 hex) prevents IC211 to be open by IC141 when reading from the color palette. ($\overline{\text{EDBUF0}}$ is disabled at time of $\overline{\text{IREG}}$ and $\overline{\text{IOR}}$.

i) VGA BIOS

VGA BIOS is mapped to E0000H to E7FFFH of the system ROM. (But E6000H to E67FFH are mapped out for prevention of collision from the IBM PGA board.)

j) Internal configuration of PVGA1A

PVGA1A has four major functions. These are ① CRT controller, ② Sequencer, ③ Graphics controller and ④ Attribute controller. Also, there are five major interfaces, namely, 1) CPU interface, 2) Clock interface, 3) DRAM (display memory) interface, 4) Video interface and 5) BIOS interface. PVGA1A provides interface between the system microprocessor and the video memory. When the system microprocessor writes data in the video memory, or when it reads data from the video memory, all data passes through PVGA1A. Also, PVGA1A controls access to the video memory with the system microprocessor and access to the video memory with the CRT controller mounted in PVGA1A. PVGA1A has FIFO for ruling out the possibility of a race between the CPU access cycle and the display refresh cycle during video display.

① CRT controller

The CRT controller creates the H sync, V sync and video display timing, cursor underline timing and address to DRAM.

② Sequencer

The sequencer creates a character clock for controlling the basic timing of DRAM and display data. The system microprocessor gains access to the memory during screen display with the system microprocessor memory cycle cyclically inserted into the display memory. It can prevent all memory maps from updating by the map master resister.

③ Graphics controller

The graphics controller operates as both a video memory and an attribute controller interface during a display period. In the process of video memory read/write, it operates as an interface with the video memory and the system microprocessor. During a display period, the graphics controller latches the memory data and sends it to the attribute controller. In the graphics mode, it makes parallel-to-serial conversion of data received from the memory, and in the text mode, it sends attribute data directly. While the system microprocessor either reads data from, or write it in, the video memory, the graphics controller logically handles memory data before it reaches the video memory or system microprocessor data bus. The logic work consists of four logical write modes and two logical read modes. With these features, expansion operations such as the color compare read mode, individual bit masking during the write mode, 32-bit writes in a single memory cycle, and writing to the display buffer on non-byte boundaries are possible.

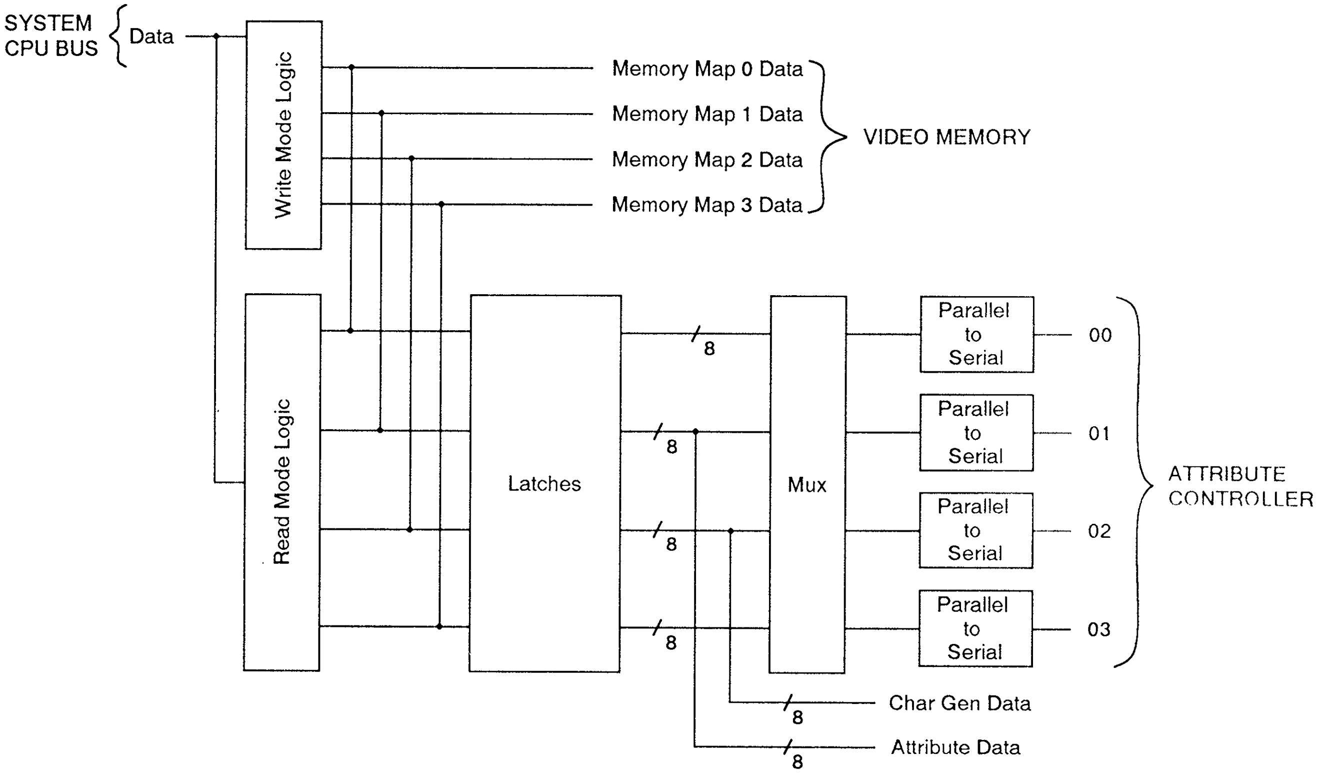
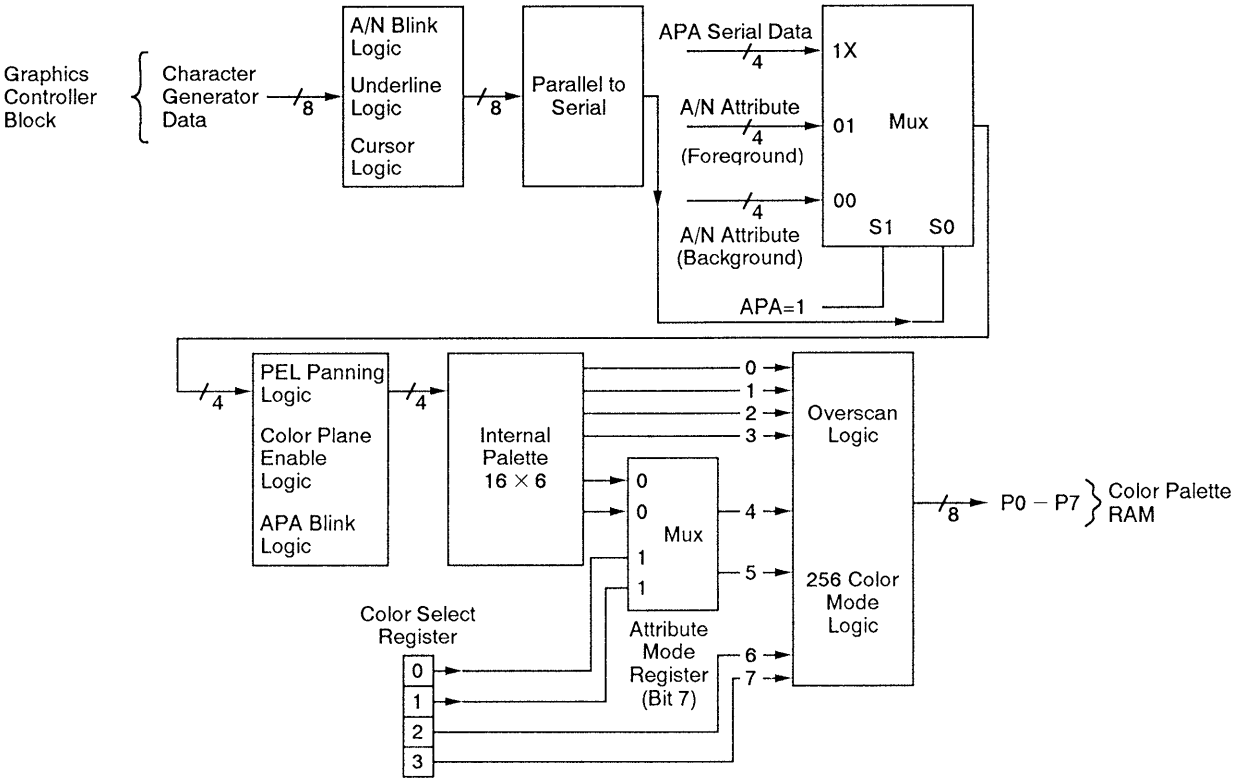

SYSTEM CPU BUS
Data
Write Mode Logic
Memory Map 0 Data
Memory Map 1 Data
Memory Map 2 Data
Memory Map 3 Data
VIDEO MEMORY
Read Mode Logic
Latches
8
8
8
8
Mux
Parallel to Serial
Parallel to Serial
Parallel to Serial
Parallel to Serial
00
01
02
03
ATTRIBUTE CONTROLLER
8
Char Gen Data
8
Attribute Data

Fig. 3-7. Graphics controller block diagram

④ Attribute controller

The attribute controller fetches data from the video memory via the graphics controller to format the data for showing it on the display screen. In the text mode, attribute data is changed into 8 bit PIX address and then output; in the graphics mode, bit plane data is changed into 8 bit PIX address and then output after parallel-to-serial conversion. Each PIX address is selected from 64 colors of internal color palette (excepting the 256 color mode). The PIX address to be output is a color palette RAM address. Blinking, underlining, cursor insertion and PEL panning are also controlled by the attribute controller.



Graphics Controller Block
Character Generator Data
8
A/N Blink Logic
Underline Logic
Cursor Logic
8
Parallel to Serial
APA Serial Data
4
A/N Attribute
4
(Foreground)
4
A/N Attribute (Background)
1X
01
00
Mux
S1
S0
APA=1
4
PEL Panning Logic
Color Plane Enable Logic
APA Blink Logic
4
Internal Palette 16 × 6
0
0
1
1
Mux
0
1
2
3
4
5
6
7
Overscan Logic
256 Color Mode Logic
8
P0 – P7
Color Palette RAM
Color Select Register
0
1
2
3
Attribute Mode Register (Bit 7)

Fig. 3-8. Attribute controller block diagram

k) Memory write operations

When the CPU is written into the video memory, the map is enabled by memory address decoding and the map mask register in the video mode. The flow of data during CPU write operation is shown in Fig. 3-9.

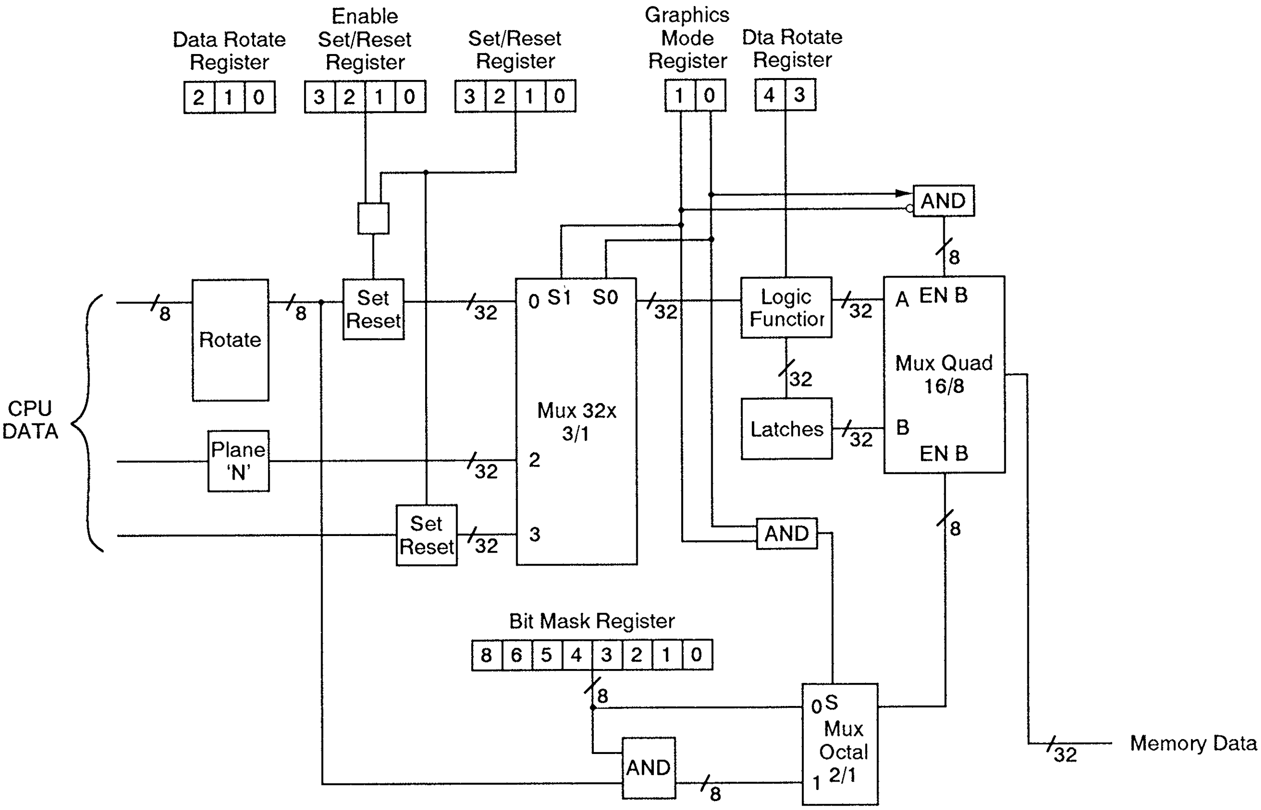

Data Rotate Register
2 1 0
Enable Set/Reset Register
3 2 1 0
Set/Reset Register
3 2 1 0
Graphics Mode Register
1 0
Dta Rotate Register
4 3
AND
8
CPU DATA
8
Rotate
8
Set Reset
32
0 S1 S0
32
Logic Functior
32
A EN B
Mux Quad 16/8
32
Latches
32
B
EN B
Mux 32x 3/1
Plane 'N'
32
2
Set Reset
32
3
AND
8
Bit Mask Register
8 6 5 4 3 2 1 0
8
0 S
Mux Octal 2/1
1
AND
8
32
Memory Data

Fig. 3-9. VGA memory write data flow

l) Video memory read operations

Two methods are available for reading the video memory.

1. When read type 0 is selected by the graphics mode register, the CPU decodes the memory address and reads the 8 bit value determined by the read map select register from the video memory.
2. When read type 1 is selected by the graphics mode register, the 8 bit value, which is the result of color compare operation controlled by the "color compare register" and the "color don't care register", is returned. The color compare operation is shown in Fig. 3-10.

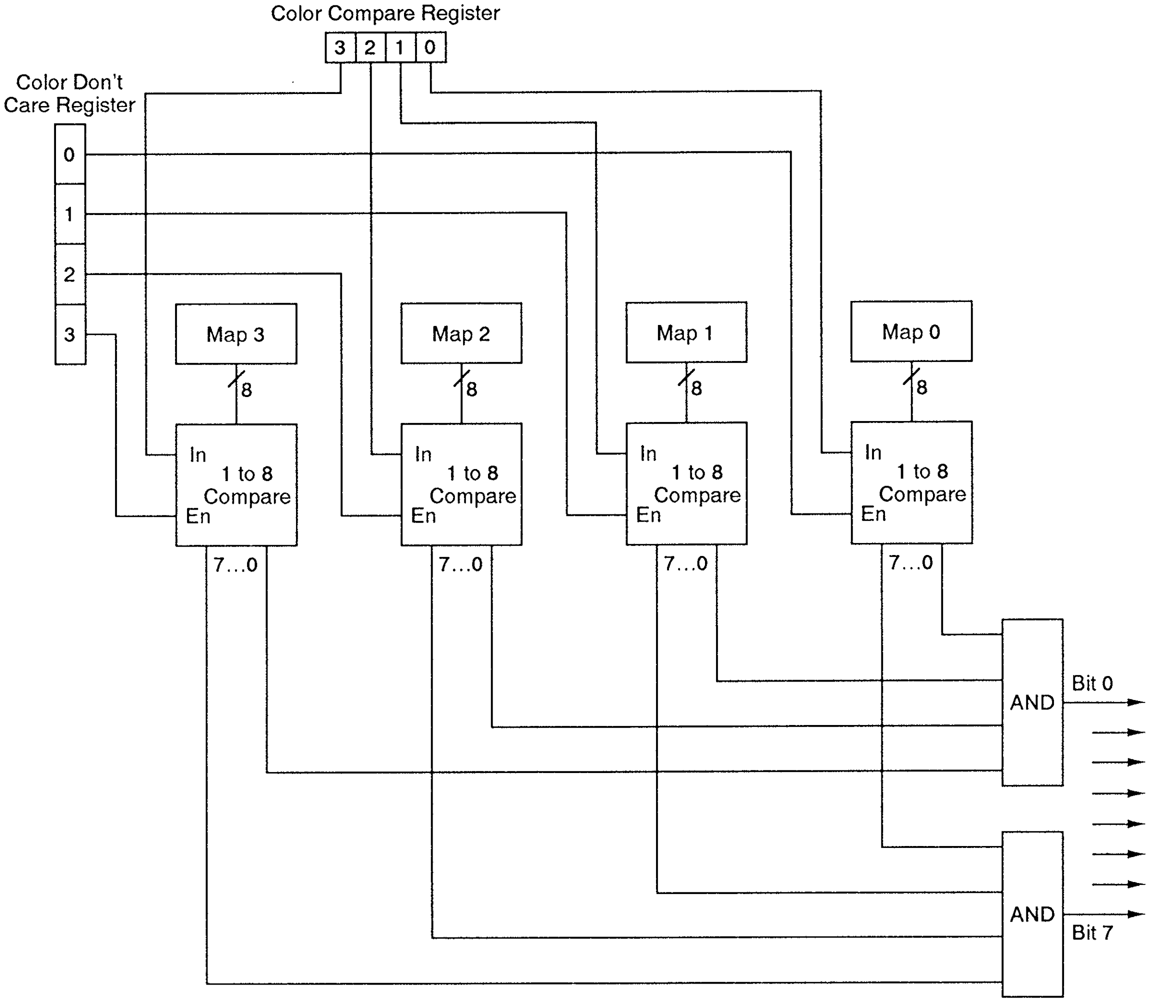

Color Compare Register
3
2
1
0
Color Don't Care Register
0
1
2
3
Map 3
Map 2
Map 1
Map 0
8
In
1 to 8 Compare
En
7...0
AND
Bit 0
Bit 7

Fig. 3-10. VGA color compare data flow

3-2-3. Superimpose Block

3-2-3-1. Gate array μPD65013S-526 (IC228)

a) General

This gate array is an IC designed specifically for the VGA superimposer. With a signal from the VGA IC PVGA1A (IC213), external palette SRAM (IC230 to IC232) is controlled and then superimposed with the video signal from the video disk player, to generate an output signal to the D/A converter.

b) Block diagram

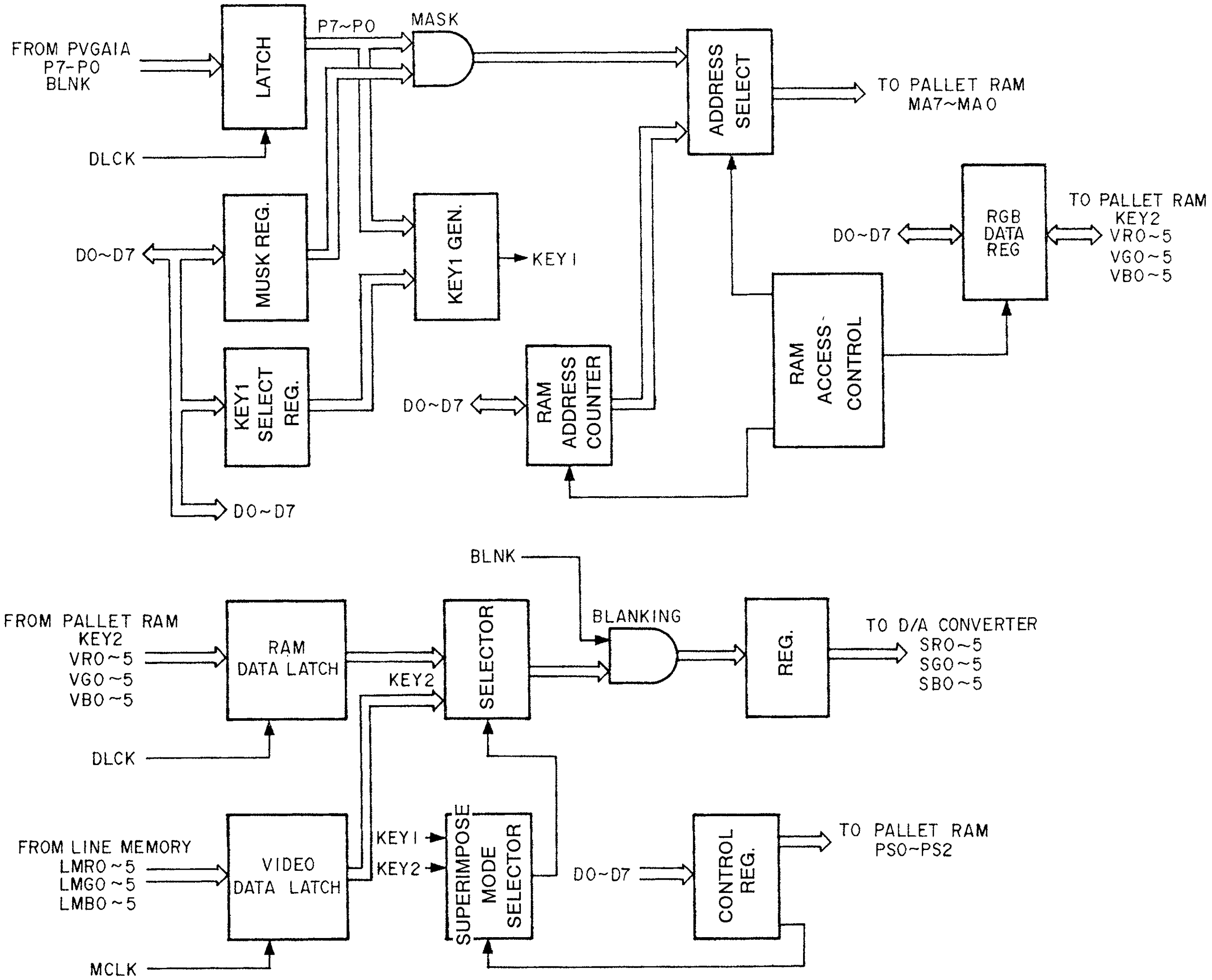

FROM PVGAIA
P7-PO
BLNK
LATCH
DLCK
P7~PO
MASK
ADDRESS SELECT
TO PALLET RAM
MA7~MA O
MUSK REG.
DO~D7
KEY1 GEN.
KEY I
KEY1 SELECT REG.
DO~D7
DO~D7
RAM ADDRESS COUNTER
RAM ACCESS CONTROL
DO~D7
RGB DATA REG
TO PALLET RAM
KEY2
VRO~5
VGO~5
VBO~5
BLNK
FROM PALLET RAM
KEY2
VRO~5
VGO~5
VBO~5
RAM DATA LATCH
DLCK
KEY2
SELECTOR
BLANKING
REG.
TO D/A CONVERTER
SRO~5
SGO~5
SBO~5
FROM LINE MEMORY
LMRO~5
LMGO~5
LMBO~5
VIDEO DATA LATCH
MCLK
KEY I
KEY2
SUPERIMPOSE MODE SELECTOR
DO~D7
CONTROL REG.
TO PALLET RAM
PSO~PS2

Fig. 3-11.

c) Outline of operation

Palette address P7 to P0 (VD7 to VD0) from PVGA1A (IC213) is once latched and masked by the mask register, following which it is output as an address signal (MA7 to MA0) of the palette RAM. Data VR0 to VR5, VG0 to VG5, VB0 to VB5, KEY2 of the palette RAM accessed by the address are latched by DLCK for superimposing the video disk signal by the selector, and then latched once again, after which it is input into the D/A converter.

On the other hand, video disk signal data LMR0 to LMR5, LMG0 to LMG5, LMB0 to LMB5 received from the line memory (IC221 to IC223) are latched by MCLK and then input into the selector for superimposing the computer pictures. The method of specifying the bit at which a video disk signal is output in the process of superimpose is available in two methods. One is the method by the palette address. In this method, latched P0 to P7 is compared with the contents of the KEY1 designated register and a KEY1 signal is sent out if coincided to switch it over to the video disk signal by the selector.

The RAM bit designation method is such that the video disk signal is switched by the selector based on the KEY2 signal read out from the palette RAM. In this method, a key bit can be inserted into all palette data. Transparent colors up to 256 can therefore be designated.

When reading and writing D0 to D7 in the palette RAM, the process is as given below. Address is written in the RAM address counter. Next, when 3 bytes are continuously written in from the data bus, each six bits of R, G and B, and KEY2 signal can be written in the data register. After writing the 3rd byte, address line of MA7 to MA0 is switched over to the contents of the RAM address counter, and the contents of R, G, B data register are written in. The RAM address counter is incremented by 1 (+1) as a result. After that, it is sequentially written into the palette RAM by writing 3 bytes at a time.

When reading, read start address is written in the RAM address counter from the data bus. After writing operation, MA7 to MA0 is switched over to the contents of the RAM address counter so that the contents of the palette RAM are fetched to the R, G, B data registers. (VP0 to VP5, VG0 to VG5, VB0 to VB5, KEY2)

Further, RAM address counter is incremented by 1 (+1).

After this, 6 bits each of R, G and B, and the KEY2 signal can be read by reading RGB data bus three times from the data bus. Following the B data read operation, next data is automatically fetched to the R, G, B data registers from the palette RAM.

d) Pin Description

PIN No.	SIGNAL		I/O	FUNCTION
1	NC		—	
2	NC		—	
3	VR4	R DATA	I/O	Data line for reading and writing the R signal in the palette RAM.
4	VR1			
5	VG4	G Data	I/O	Data line for reading and writing the G signal in the palette RAM.
6	VG1			
7	VB5	B Data	I/O	Data line for reading and writing the B signal in the palette RAM.
8	VB2			
9	D07	Data Bus	I/O	A data bus for reading and writing data in the internal register.
10	D04			
11	D03			
12	D02			
13	NC		—	
14	D01	Data Bus	I/O	A data bus for reading and writing data in the internal register.
15	$\overline{IOR}$		I	A signal for reading from the internal register.
16	A0		I	The internal port select signal. The port to be accessed depends upon a suitable combination of A0, A1, $\overline{IREG}$ and $\overline{SREG}$.
17	MCLK	Master Clock	I	This is an internally used master clock. It changes in a range from 25.7 MHz to 32.3 MHz depending upon the mode selected.
18	SB0	D/A B Data	O	A B data output for data input into the D/A converter. A CPU image and a video image are superimposed and then output.
19	SB1			
20	SB4			
21	SG0	D/A G Data	O	A G data output for data input into the D/A converter. A CPU image and a video image are superimposed and then output.
22	SG3			
23	SG4			
24	SG5			
25	NC		—	

Table 3-21 (1/3).

PIN NO.	SIGNAL		I/O	FUNCTION
26	SR0	S/A R Data	O	Input terminals of palette address applied from VGA IC (PVGA1A).Input terminals for the R signal from the line memory.Reset is made at "0".
27	SR1			
28	SR2			
29	P2	Palette Address	I	
30	P5			
31	P7			
32	LMR4		I	
33	LMR1			
34	$\overline{\text{RESET}}$	RESET	I	
35	LMG5		I	Input terminals for the G signal from the line memory.
36	LMG4			
37	NC		—	
38	LMG3		I	Input terminals for the G signal from the line memory.
39	LMG1			
40	LMB4		I	Input terminals for the B signal from the line memory.
41	LMB1			
42	$\overline{\text{MEMOE}}$	Memory Output Enable	O	The output enable signal of the palette RAM. Enable is made at "0".
43	PS0	Palette Select Signal	O	A signal for selecting eight palette RAMs.
44	MA7	RAM Address	O	Address output for accessing an external palette RAM.
45	MA4			
46	MA1			
47	MA0			
48	KEY2	Key 2 Bit	I/O	Line for reading and writing the key 2 signal in the palette RAM.
49	NC		—	
50	VR5	R DATA	I/O	Data line for reading and writing the R signal in the palette RAM.
51	VR2			
52	VG5	G Data	I/O	Data line for reading and writing the G signal in the palette RAM.
53	VG2			
54	VG0			
55	VB3	B Data	I/O	Data line for reading and writing the B signal in the palette RAM.
56	VB0			
57	D05	Data Bus	I/O	A data bus for reading and writing data in the internal register.
58	NC		—	
59	NC		—	
60	D00	Data Bus	I/O	A data bus for reading and writing data in the internal register.
61	A1		I	The internal port select signal. The port to be accessed depends upon a suitable combination of A0, A1, $\overline{\text{IREG}}$ and $\overline{\text{SREG}}$.
62	$\overline{\text{SREG}}$			
63	DLCK		I	A clock for latching the data from the palette RAM. A dot clock is externally generated for input in harmony with the RAM address output timing.
64	GND		—	
65	SB3	D/A B Data	O	A B data output for data input into the D/A converter. A CPU image and a video image are superimposed and then output.
66	SB5			
67	SG2	D/A G Data	O	A G data output for data input into the D/A converter. A CPU image and a video image are superimposed and then output.
68	NC		—	
69	NC		—	
70	SR1	D/A R Data	O	A R data output for data input into the D/A converter. A CPU image and a video image are superimposed and then output.
71	SR4			
72	P1	Palette Address	I	Input terminals of palette address applied from VGA IC (PVGA1A).
73	P4			
74	GND		—	

Table 3-21 (2/3).

PIN No.	SIGNAL		I/O	FUNCTION
75	LMR5		I	Input terminals for the R signal from the line memory.
76	LMR2			
77	LMR0			
78	NC		—	
79	NC		—	
80	LMG2		I	Input terminal for the G signal from the line memory.
81	LMB5		I	Input terminals for the B signal from the line memory.
82	LMB2			
83	$\overline{\text{MEMWE}}$	Memory Write Enable	O	The write control signal of the palette RAM.
84	GND		—	Write operation takes place at "0".
85	PS2	Palette Select Signal	O	A signal for selecting eight palette RAMs.
86	MA5	RAM Address	O	Address output for accessing an external palette RAM.
87	MA2			
88	NC		—	
89	NC		—	
90	VR3	R DATA	I/O	Data line for reading and writing the R signal in the palette RAM.
91	VR0			
92	VG3	G Data	I/O	Data line for reading and writing the G signal in the palette RAM.
93	GND		—	
94	VB4	B Data	I/O	Data line for reading and writing the B signal in the palette RAM.
95	VB1			
96	D06	Data Bus	I/O	A data bus for reading and writing data in the internal register.
97	NC		—	
98	$\overline{\text{IOW}}$		I	A signal for writing data in the internal register.
99	$\overline{\text{IREG}}$		I	The internal port select signal. The port to be accessed depends upon a suitable combination of A0, A1, $\overline{\text{IREG}}$ and $\overline{\text{SREG}}$.
100	CKD2		I	This signal is for internally generating a dot clock. In the horizontal 640 mode, "0" is input; in the horizontal 320 mode, half the frequency of MCLK is input.
101	+5V		—	
102	SB2	D/A B Data	O	A B data output for data input into the D/A converter. A CPU image and a video image are superimposed and then output.
103	GND		—	
104	SG1	D/A G Data	O	A G data output for data input into the D/A converter. A CPU image and a video image are superimposed and then output.
105	NC		—	
106	SR3	D/A R Data	O	A R data output for data input into the D/A converter. A CPU image and a video image are superimposed and then output.
107	P0	Palette Address	I	Input terminals of palette address applied from VGA IC (PVGA1A).
108	P3			
109	P6			
110	$\overline{\text{BLANK}}$	Blanking Input	I	Blanking is applied to both the video images and CPU images at "0".
111	LMR3		I	Input terminal for the R signal from the line memory.
112	NC		—	
113	NC		—	
114	LMG0		I	Input terminal for the G signal from the line memory.
115	LMB3		I	Input terminals for the B signal from the line memory.
116	LMB0			
117	+5V		—	
118	PS1	Palette Select Signal	O	A signal for selecting eight palette RAMs.
119	MA6	RAM Address	O	Address output for accessing an external palette RAM.
120	MA3			

Table 3-21 (3/3).

e) Internal ports

Internal port read and write operations can be made depending upon the combination of A0, A1, IREG and SREG input signals.

IREG	SREG	A1	A0	R/W	Register
0	1	0	0	R/W	Palette write address.
0	1	0	1	R/W	Palette data (IBM)
0	1	1	0	R/W	Mask (host) register
0	1	1	1	W	Palette read address
0	1	1	1	R	Status register
1	0	0	0	W	Control register
1	0	0	1	W	Board control port
1	0	1	0	R/W	Superimpose address
1	0	1	1	R/W	Palette data (Sony)

Table 3-22.

3-2-3-2. Gate array μPD65006GF-325-3B8 (IC224)

a) Functions and block diagram

The gate array μPD65006GF-325-3B8 has functions of address decoder (I/O port), superimpose control, line memory, A/D converter clock generator and genlock circuit, etc. The block diagram of the gate array is shown in Fig. 3-12.

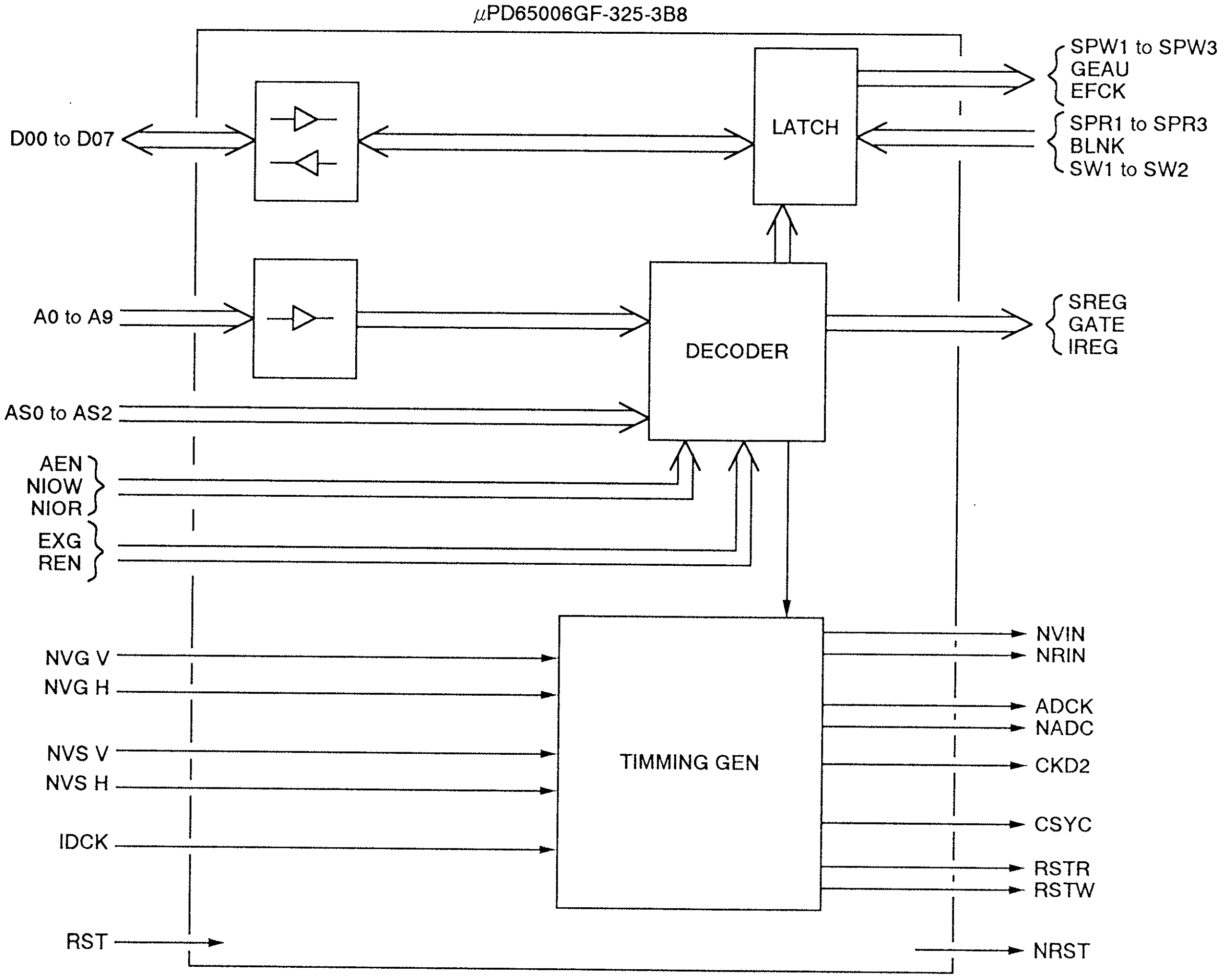

μPD65006GF-325-3B8
D00 to D07
A0 to A9
AS0 to AS2
AEN
NIOW
NIOR
EXG
REN
NVG V
NVG H
NVS V
NVS H
IDCK
RST
LATCH
DECODER
TIMMING GEN
SPW1 to SPW3
GEAU
EFCK
SPR1 to SPR3
BLNK
SW1 to SW2
SREG
GATE
IREG
NVIN
NRIN
ADCK
NADC
CKD2
CSYC
RSTR
RSTW
NRST

Fig. 3-12. Block diagram

b) Pin description

Pin No.	Pin Name	I/O	Description & Connection
1	N.C	—	
2	D02	I/O	IBM-AT bus SD2
3	D01	O	IBM-AT bus SD1
4	D00	I/O	IBM-AT bus SD0
5	GATE	O	IBM-AT bus SD0 to SD7 Enable signal for data bus buffer. Active low
6	RST	I	IBM-AT bus RESET DRV
7	AEN	I	IBM-AT bus AEN
8	NIOW	I	IBM-AT bus -IOW
9	NIOR	I	IBM-AT bus -IOR
10	A9	I	IBM-AT bus SA9
11	A8	I	IBM-AT bus SA8
12	A7	I	IBM-AT bus SA7
13	A6	I	IBM-AT bus SA6
14	A5	I	IBM-AT bus SA5
15	A4	I	IBM-AT bus SA4
16	A3	I	IBM-AT bus SA3
17	A2	I	IBM-AT bus SA2
18	A1	I	IBM-AT bus SA1
19	A0	I	IBM-AT bus SA0
20	NRST	O	Pin 6 RST negation
21	IREG	O	Decode signals of I/O address 3C6H, 3C7H, 3C8H and 3C9H on the IBM VGA board. Active low.
22	SREG	O	Decode signals of Sony's exclusive I/O address XXCH, XXDH, XXEH and XXFH*1. Active low.
23	CKD2	O	When "1" is written in I/O port XXDH D2 (in the horizontal 320 mode), a pulse of 2 frequency divided IDCK is output. When "0" is written in I/O port XXDH D2*1 (in the horizontal 640 mode), the output is low. This signal is used for latching the palette address data in the VGA superimpose IC (IC228) for generation of a dot clock.
24	EXG	I	5 gate control input terminal for input of +5V.
25	REN	I	5 gate control input terminal for controlling gate signal output when reading 3C6H to 3C9H. When +5V is input: when reading 3C6H to 3C9H, no gate signal is output. When 0V is input: when reading 3C6H to 3C9H, a gate signal is output. Connected to the GND.
26	GND	—	
27	VDD	—	+5V
28	SPR1	I	Read at XXCH (D3)*1
29	SPR2	I	Read at XXCH (D4)*1
30	SPR3	I	Read at XXCH (D5)*1
31	RSTW	O	Used as a reset write signal of the line memory (μPD41102G).
32	RSTR	O	Used as a reset read signal of the line memory (μPD41102G).
33	GEAU	O	A signal for controlling the genlock mode of the computer image and the video image. Write "0" in XXDH D0*1: Genlock auto Write "1" in XXDH D0*1: Genlock internal
34	NVSV	I	For input of V sync of external video signal. Negative.*2
35	NVSH	I	For input of H sync of external video signal. Negative.*2
36	SPW1	O	Written at XXDH (D3)*1.
37	SPW2	O	Written at XXDH (D4)*1.
38	SPW3	O	Written at XXDH (D5)*1.
39	N.C	—	
40	N.C	—	
41	GND	—	
42	N.C	—	
43	GND	—	

Table 3-23 (1/2).

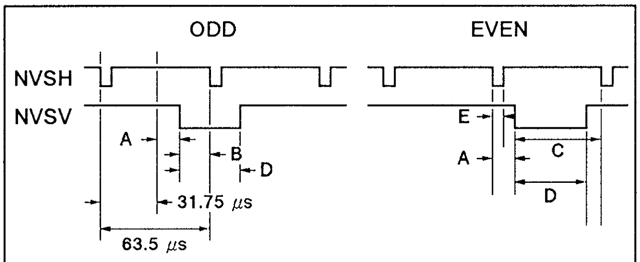
Pin No.	Pin Name	I/O	Description & Connection
44	ADCK	O	Used as a write clock of the line memory (μPD41102C). It frequency divides 50 IDCK to reset FF at the falling edge of NVSH.
45	NADC	O	Used as a clock of the A/D converter. It is a pin 44 ADCK inverted pulse.
46	BLNK	I I	This inputs blanking. Positive. It can be read at XXCH (D2). "1" indicates during blanking. Connected to GND.
47	NVGV	I	This inputs VOUT (V SYNC) from VGA IC (PVGA1A). It sets VGA to negative polarity.
48	NVGH	O	This inputs HOUT (H SYNC) from VGA IC (PVGA1A). It sets VGA to negative polarity.
49	EFCK	I	It is connected to the clock switchover IC (IC215). When 1, 0 are written in I/O ports 3C2H D3, D2, the voltage level is forced low. An external clock can be input to VGA superimpose IC (IC228).*4
50	IDCK	I	This inputs a dot clock.
51	AS0	I	Sony exclusive I/O port can be selected as below depending upon the input conditions of AS0 to AS2.
52	AS1	I	
53	AS2	I	
54	SW2	I	This can be read at XXCH (D1)*1. (Not used)
55	SW1	I	This can be read at XXCH (D0)*1. (Not used)
56	NRIN	O	This outputs the pulse frequency divided by FF at the falling edge of NVGH.*3 It is connected to pin 7 of the phase comparator CX-23065.
57	NVIN	O	This outputs NVSH.*3 It is connected to pin 6 of the phase comparator CX-23065.
58	GND	—	
59	CSYC	O	This is an open drain output for output of C SYNC. Negative polarity.
60	D07	O	IBM-AT bus. SD7
61	D06	O	IBM-AT bus. SD6
62	D05	I/O	IBM-AT bus. SD5.
63	D04	I/O	IBM-AT bus. SD4
64	D03	I/O	IBM-AT bus. SD3

Address	33X	34X	35X	25X	26X	28X	29X	2AX
AS0	L	H	L	H	L	H	L	H
AS1	L	L	H	H	L	L	H	H
AS2	L	L	L	L	H	H	H	H

Notes*:Input and outputs except for C sync at pin 59 are TTL level.

*1. XX is determined by the input conditions of pins 51 to 53 AS0 to AS2.

*2. Conditions of the pulse width of the NVSV and NVSH pulses.



	Contents (Conditions)	Time (sec.)
A	Time difference between NVSV and HVSH due to V sync separation.	Approx. 18 μ
B	Minimum value of NVSV pulse width. (B>D)	—
C	Maximum value of NVSV pulse width. (C<D)	—
D	Optimum value:D= (B+C) /2	Approx. 28 μ
E	NVSH pulse width. (E<A)	Approx. 4.4 μ

Fig. 3-13. Input conditions of NVSV and NVSH pulses

*3. If a phase shift between the falling edge of the NVSV pulse and the falling edge of the frequency-divided NVGV pulse is in excess of 1H, the NVSH or NVGH pulse is removed for V sync phase matching (genlock).

*4. EFCK is used as a select signal for selecting either PCLK (through mode) or the ACLK (genlock mode) as a clock for latching the palette address PD0 to PD7 from the VGA IC (PVGA1A).

Table 3-23 (2/2).

3-2-3-3. DCK circuit (PLL circuit)

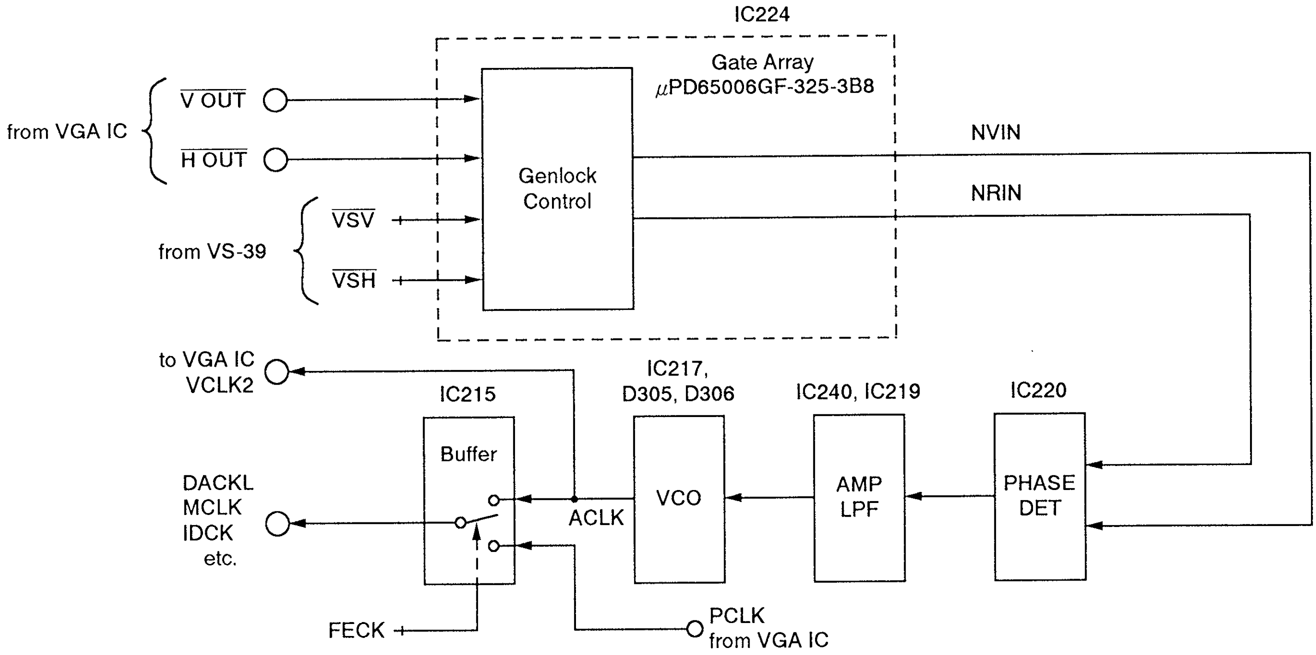

IC224
Gate Array
µPD65006GF-325-3B8
from VGA IC
V OUT
H OUT
Genlock
Control
NVIN
NRIN
from VS-39
VSV
VSH
to VGA IC
VCLK2
IC215
IC217,
D305, D306
IC240, IC219
IC220
Buffer
DACKL
MCLK
IDCK
etc.
VCO
AMP
LPF
PHASE
DET
ACLK
FECK
PCLK
from VGA IC

Fig. 3-14. Dot clock generator

When a CLK is fed to VGA IC (PVGA1A) from (either VCLK 0 or VCLK1, 2), sync signals (V OUT, H OUT) are output according to the VGA CRTC setting. The CLK (VCLK0 to VCLK2) select of VGA and the CLK select of IC215 are controlled by "D3", "D2" of I/O port 3C2H, and VCLK2 is input to VGA IC when it is "1", "0", respectively. As a result, a clock from VCO is supplied to make genlock possible.

VGA is normally set to vertical 70 Hz and horizontal 31.5 kHz. In this condition, it is not synchronized, and for this reason, genlock to the video signal is accomplished by setting the parameters of the CRTC to vertical 60 Hz and horizontal 31.5 kHz once again. Polarity is negative for both HOUT and V OUT.

The dot clock causes the error of the Phase DET (IC220) to be passed thorough the LPF AMP, thereby changing the applied voltage of D305 and D306 for synchronizing the oscillated frequency with $\overline{\text{VSH}}$ (external video signal). HOUT from the VGA IC is 31.5 kHz (in the gate array). Therefore, the flip-flop is triggered at the falling edge of it to create a 15.75 kHz pulse NRIN. This falling edge is compared with that of $\overline{\text{VSH}}$ for phase comparison by IC220.

In the gate array (IC224), VOUT from the VGA IC is phase compared with $\overline{\text{VSV}}$ of an external video signal. If a phase difference is in excess of 1H, an error is caused by forcedly removing either the falling edge NVIN or NRIN to the Phase DET, thereby matching the vertical phase. (See Fig. 3-16)

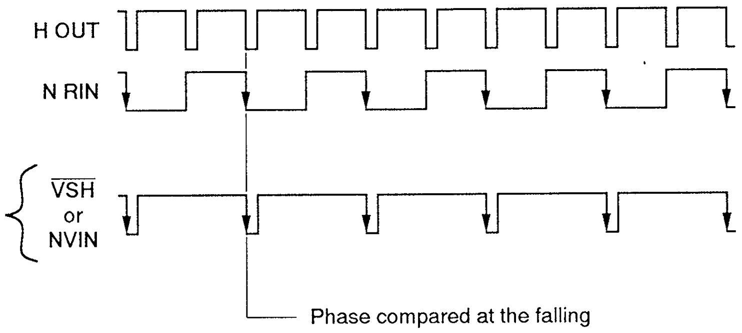
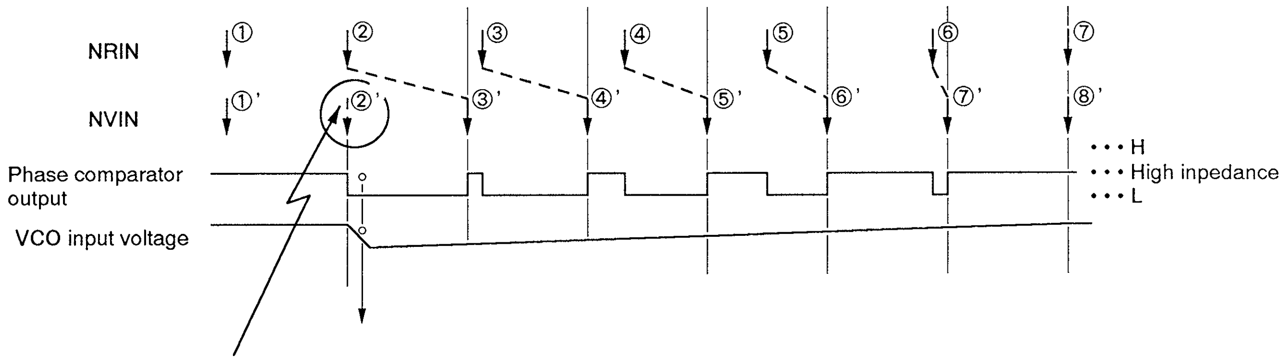

H OUT
N RIN
VSH
or
NVIN
Phase compared at the falling

Fig. 3-15. Genlock circuit descriptions inside IC224


NRIN
NVIN
Phase comparator output
VCO input voltage
①
②
③
④
⑤
⑥
⑦
①'
②'
③'
④'
⑤'
⑥'
⑦'
⑧'
• • • H
• • • High inpedance
• • • L

When this is removed → VCO input voltage drops → DCLK frequency drops → HOUT cycle extends.
(When removing ②' falling edge, it is locked so as to be watched, ⑦ and ⑧' phases)

Fig. 3-16. Genlock concept diagram

The gain of filter is switched over by the analog switch of IC240, and a pulse, which is brought low for a period of approx. 965 μ from the falling edge of the $\overline{VSV}$ (the vertical sync signal of an external video signal) by the monostable multivibrator in VS-39, is created. During this period, the gain of the filter is set somewhat high. This is for the reason that when making a track jump while the video disk player is still, the video signal is shifted in phase (approx. 130 μsec.) for every one frame for color framing. At a normal gain, image sway occurs at the upper part of the screen. Thus, the gain is switched as mentioned to facilitate phase lock after track jump.

The CLK to be output from VCO is not only input to VGA, but also used for creation of a clock of the line memory and D/A, A/D converters. The CLK to the line memory and the A/D converter is created by the gate array (IC224) μPD65006GF-325-3B8. NADC shown in Fig. 3-17 is used as a clock of the A/D converter.

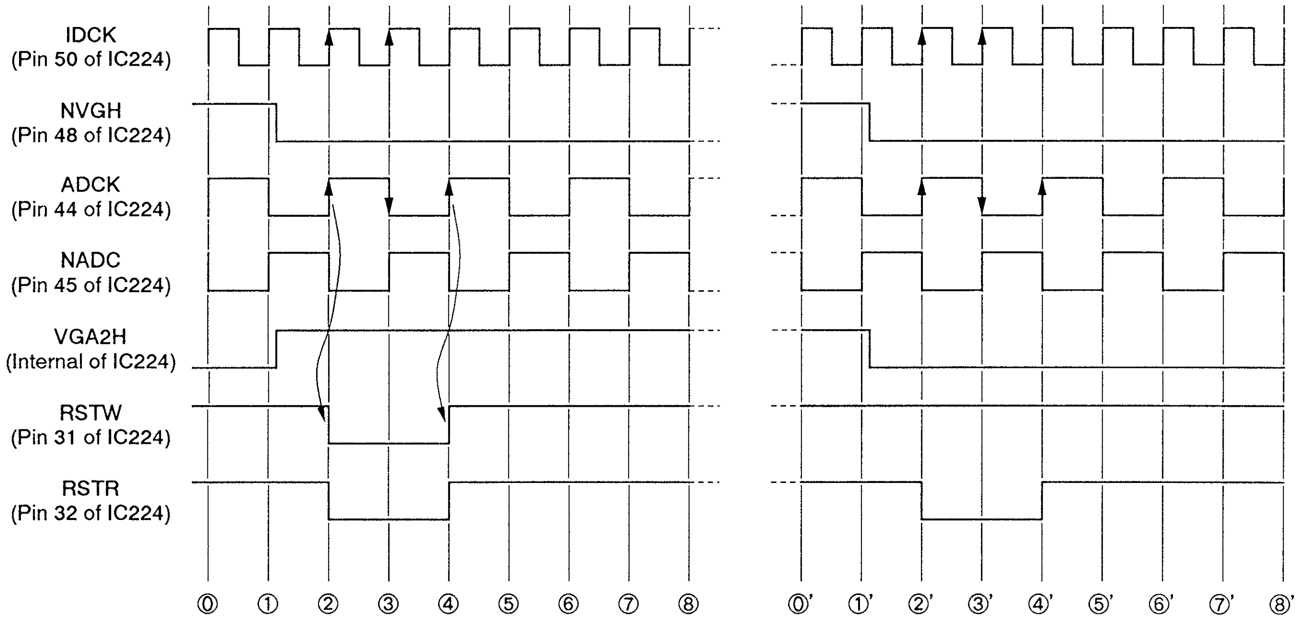
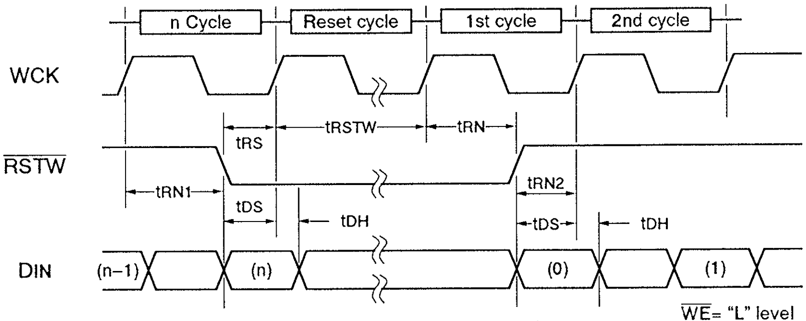

IDCK
(Pin 50 of IC224)
NVGH
(Pin 48 of IC224)
ADCK
(Pin 44 of IC224)
NADC
(Pin 45 of IC224)
VGA2H
(Internal of IC224)
RSTW
(Pin 31 of IC224)
RSTR
(Pin 32 of IC224)
⓪ ① ② ③ ④ ⑤ ⑥ ⑦ ⑧
⓪' ①' ②' ③' ④' ⑤' ⑥' ⑦' ⑧'

Fig. 3-17. Line memory ADC clock generation timing chart

3-2-3-4. Line memory μPD41102G

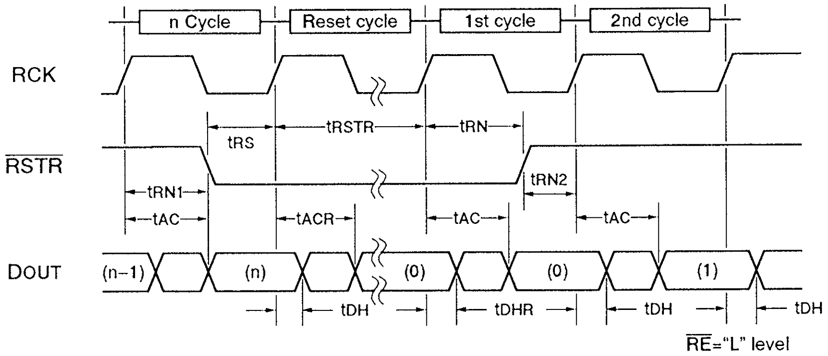
IC221, IC222 and IC223 scan and convert data converted from the A/D converter in VS-39 into 6 bits each of R, G and B signals, respectively and input them to the gate array (IC228) μPD65013S-526. The CLK to the line memory is created by the gate array (IC224) μPD65006GF-325-3B8.

Its timing chart is shown in Fig. 3-17. RSTW, RSTR become timing pulses for data read and write in the memory. The timing of the CLK side is set to WCK (write clock) and RCK (read clock) to meet the setup time and hold time of them, with IC225, R343 and R344, respectively. The characteristics of the line memory μPD42102C-3 are shown in Fig. 3-18.


n Cycle
Reset cycle
1st cycle
2nd cycle
WCK
RSTW
DIN
tRS
tRSTW
tRN
tRN1
tDS
tDH
tRN2
tDS
tDH
(n−1)
(n)
(0)
(1)
WE= "L" level

tRS	12 MIN (ns)
tRSTW	0 MIN (ns)
tRH	5 MIN (ns)
tRN1	5 MIN (ns)
tRN2	12 MIN (ns)
tRSTR	0 MIN (ns)

(A) Write reset cycle


n Cycle
Reset cycle
1st cycle
2nd cycle
RCK
RSTR
DOUT
tRS
tRSTR
tRN
tRN1
tAC
tACR
tAC
tRN2
tAC
(n−1)
(n)
(0)
(0)
(1)
tDH
tDHR
tDH
tDH
RE="L" level

(B) Read reset cycle

Fig. 3-18. Characteristics of the line memory μPD41102C-3

3-2-3-5. D/A converter μPD6902C

The D/A converter makes D/A conversion of the data SR5 to 0, SG5 to 0, and SB5 to 0 superimposed (video image and computer superimposed one on another) from the gate array (IC228) μPD65013S-526 respectively by IC233, IC234 and IC235, and then outputs them to CN110. The CLK of the D/A converter adjusts the timing (setup timing and hold timing) with the data using IC225 and R345 for input purposes.

Also, R380 (1.8K) is connected to pin 12 of IC233 via SW301, but this is intended to prevent the screen picture from being somewhat bluish by the monitor display. The R signal component is increased by 10% for that purpose when the switch is ON (when set to the right as seen from the rear panel).

3-2-3-6. VCO characteristics

The characteristics of the VCO are shown in Fig. 3-19.

The oscillated frequency at the time of genlock varies with VGA CRTC setting. It should be set over a range of approx. 25.7 to 32.3 MHz. To control the frequency within the variable range of the VCO, turn L307 in the display mode 12 until the voltage at TP201 is adjusted to 3.0 ± 0.2V.

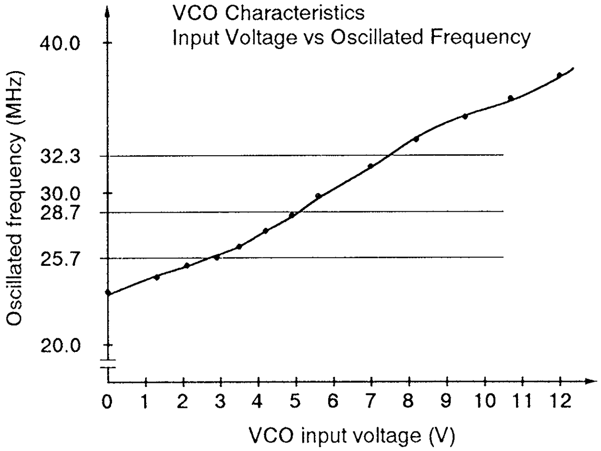


Fig. 3-19. VCO characteristics

3-2-3-7. Timing chart

(1) H 320 mode

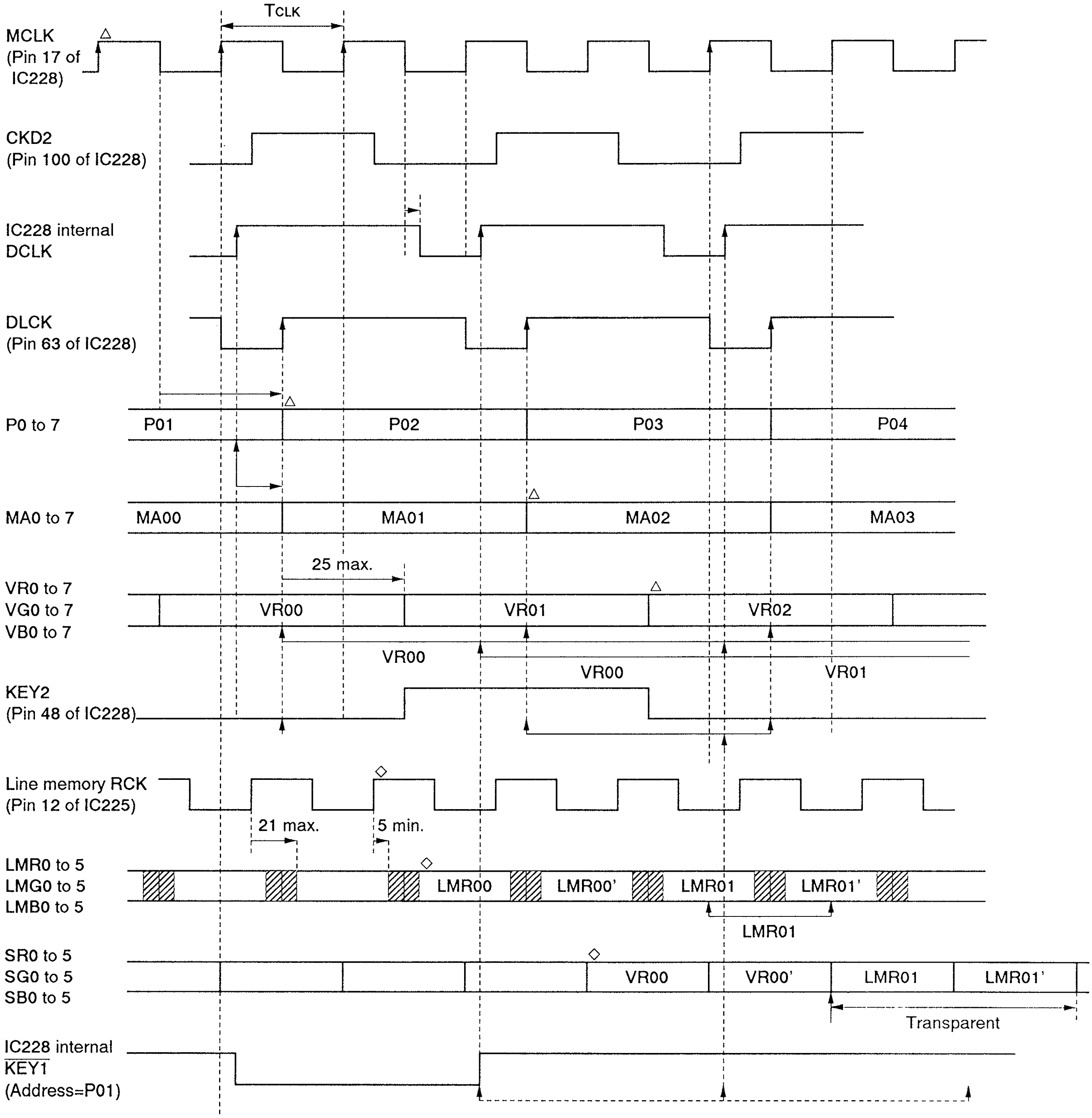

TCLK
MCLK
(Pin 17 of
IC228)
CKD2
(Pin 100 of IC228)
IC228 internal
DCLK
DLCK
(Pin 63 of IC228)
P0 to 7
P01
P02
P03
P04
MA0 to 7
MA00
MA01
MA02
MA03
25 max.
VR0 to 7
VG0 to 7
VB0 to 7
VR00
VR01
VR02
VR00
VR00
VR01
KEY2
(Pin 48 of IC228)
Line memory RCK
(Pin 12 of IC225)
21 max.
5 min.
LMR0 to 5
LMG0 to 5
LMB0 to 5
LMR00
LMR00'
LMR01
LMR01'
LMR01
SR0 to 5
SG0 to 5
SB0 to 5
VR00
VR00'
LMR01
LMR01'
Transparent
IC228 internal
$\overline{\text{KEY1}}$
(Address=P01)

Fig. 3-20.

(2) H 640 mode

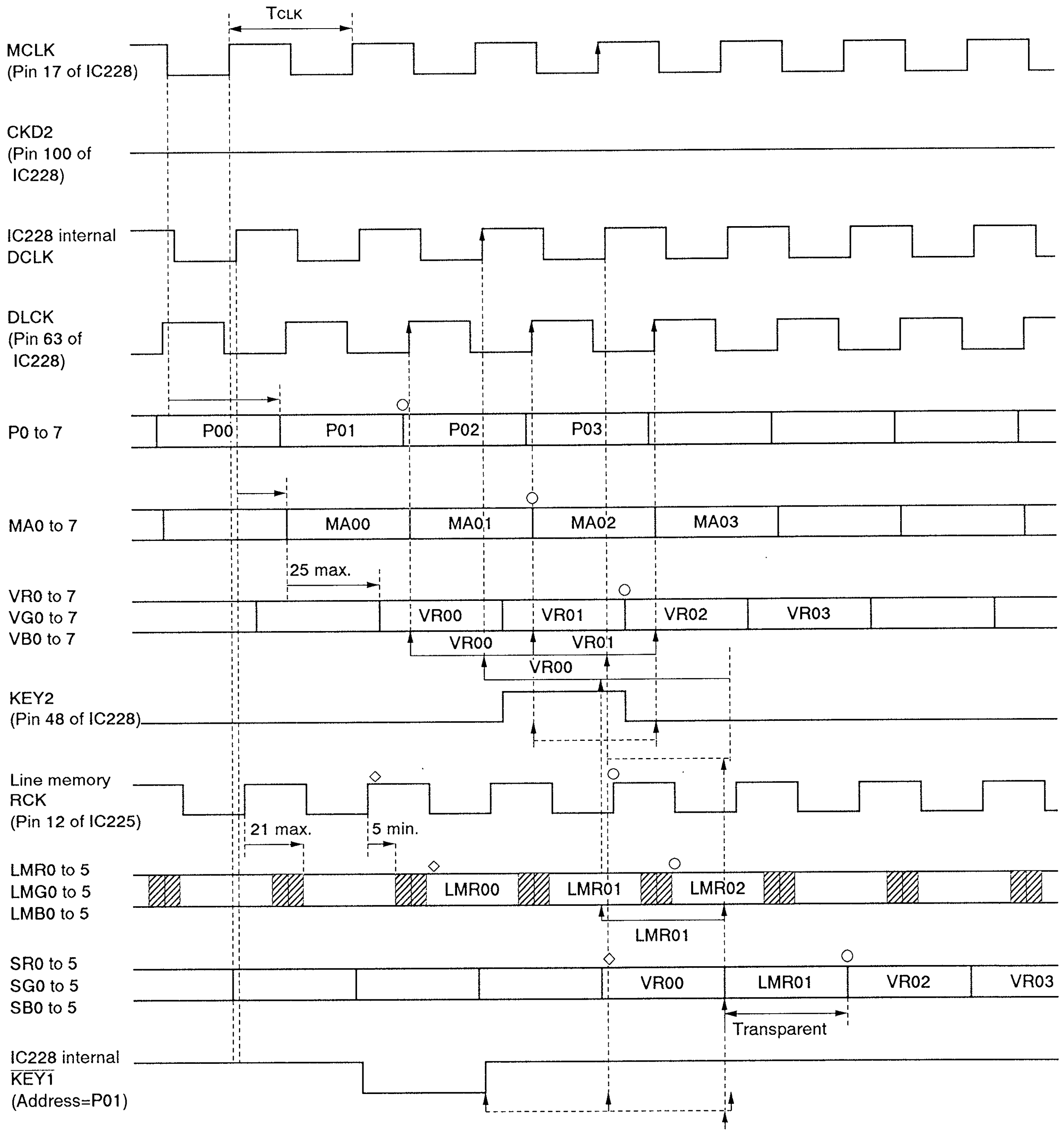

TCLK
MCLK (Pin 17 of IC228)
CKD2 (Pin 100 of IC228)
IC228 internal DCLK
DLCK (Pin 63 of IC228)
P0 to 7
P00
P01
P02
P03
MA0 to 7
MA00
MA01
MA02
MA03
25 max.
VR0 to 7
VG0 to 7
VB0 to 7
VR00
VR01
VR02
VR03
VR00
VR01
VR00
KEY2 (Pin 48 of IC228)
Line memory RCK (Pin 12 of IC225)
21 max.
5 min.
LMR0 to 5
LMG0 to 5
LMB0 to 5
LMR00
LMR01
LMR02
LMR01
SR0 to 5
SG0 to 5
SB0 to 5
VR00
LMR01
VR02
VR03
Transparent
IC228 internal $\overline{\text{KEY1}}$ (Address=P01)

Fig. 3-21.

3-2-4. Display Mode

The VGA superimposer can superimpose the video signal and the computer signal one on another in the modes given in the table below. In the monochrome mode, it cannot make superimposing operation, however. Also, these displays are all converted into vertical frequency of 60 Hz and horizontal frequency of 31.5 kHz so as to accomplish superimposition for the video signal. For this reason, the monitor display size is smaller than that when the VGA board is operated alone. Also, vertical-to-horizontal ratio also differs.

Mode	Type	Colors*1	Alpha format	Box size	PELS	Remarks
0, 1	A/N	16	40 × 25	8 × 8	320 × 200*2	
0*, 1*	A/N	16	40 × 25	8 × 14	320 × 350	
0+, 1+	A/N	16	40 × 25	9 × 16	360 × 400	
2, 3	A/N	16	80 × 25	8 × 8	640 × 200*2	
2*, 3*	A/N	16	80 × 25	8 × 14	640 × 350	
2+, 3+	A/N	16	80 × 25	9 × 16	720 × 400	
4, 5	APA	4	40 × 25	8 × 8	320 × 200*2	
6	APA	2	80 × 25	8 × 8	640 × 200*2	
D	APA	16	40 × 25	8 × 8	320 × 200*2	
E	APA	16	80 × 25	8 × 8	640 × 200*2	
10	APA	16	80 × 25	8 × 14	640 × 350	
11	APA	2	80 × 30	8 × 16	640 × 480	
12	APA	16	80 × 30	8 × 16	640 × 480	
13	APA	256	40 × 25	8 × 8	320 × 200*2	
5F	APA	256	80 × 16	8 × 16	640 × 480	*3, *4

* Enhanced modes form the IBM enhanced graphics adopter
+ Enhanced modes from the IBM personal system/2 VGA display adopter
*1. The color can be chosen from 262,144 colors.
*2. 200 line vertical resolution modes are double-scanned to display 400 line on screen
*3. Enhanced modes from PARADISE VGA PLUS CARD
*4. An expansion VRAM (optional SMI-5051) is required.

Table 3-24.

3-2-5. I/O Ports (VGA S/I Section)

I/O address	Read	Write
3C2 (H)	————	Miscellaneous output reg. D3, D2 only
3C6	Mask reg.	Mask reg.
3C7	DAC state reg.	Read address
3C8	Write address	Write address
3C9	Color reg.	Color reg.

Table 3-25. Input and output ports are compatible with IBM VGA.

I/O address	Read	Write
(H) XXC*1	Control status	Superimpose control port
XXD	B4*2	Board control port
XXE	Superimpose address	Superimpose address
XXF	Palette read port	Palette write port

*1: XX can select either 33 or 26 with the jumper post (JP201).
*2: "B4" fixed data.
*3: To identify the port, read XXD and read/write XXE of the returned address of B4. By so doing, the port can be identified automatically.

Table 3-26. Sony's exclusive I/O ports

3-2-5-1. Sony's exclusive I/O ports

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0

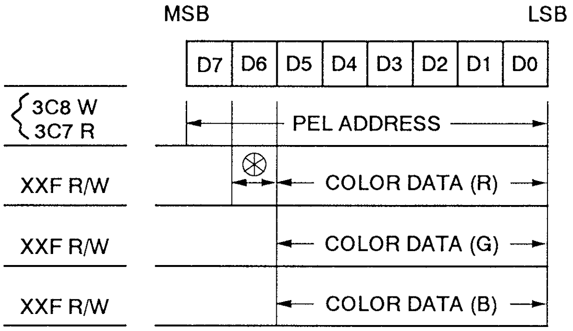
a) Superimpose Control Port XXCH (W)
- D1, D0
  - D0, D0 ············· Displays VGA images only.
  - D0, D1 ············· Superimpose by palette address
  - D1, D0 ············· Superimpose by bits in the palette RAM
  - D1, D1 ············· Displays the video images only.
- D4, D3, D2 ········ Palette Nos. to be displayed. 8 numbers 000 to 111.
- D7, D6, D5 ········ Read/write palette No. 000 to 111. However, for R/W it can perform from XXFH.

b) Control Status XXCH (R)
- D0 to D5 ··········· Reserve
- D6, D7 ············· Blank

c) Board Control Ports XXDH (W)
- D0
  - D0 ···················· Genlock Auto
  - D1 ···················· Genlock Internal
- D1
  - D1 ···················· Mute VGA + Video
- D2
  - D0 ···················· Horizontal 640 mode
  - D1 ···················· Horizontal 320 mode
- D3 to D5 ··········· Reserve
- D6, D7 ············· Blank

d) Superimpose Address XXEH (R/W)
Superimposing is done on the address which coincided with the value written D7 to D0. But it becomes valid when XXCH D1, D0 are 0, 1.

e) Palette Read/Write Ports XXFH (R/W)
After writing PEL address in 3C8H in the case of writing, and in 3C7H in the case of reading, 6 bits of R, G and B signals, and the transparent bit, can read and written by performing read/write operation of this port three times consecutively.
But read/write palettes represent palette Nos. specified by XXCH D7, D6 and D5.



* The transparent bit is assigned to bit 7 (* marked) of the color data (R).

3-2-5-2. I/O ports compatible with IBM VGA

These ports are written at the same time as VGA, but they are read by the gate arrays µPD65006GF-325-3B8 and µPD65013S-526.

a) Miscellaneous output reg. 3C2H (W)
D3 1 } ...... Genlock
D2 0 } Others are in IBM mode.

b) Mask reg. 3C6H (R/W)
The same as VGA.
Superimposing by address is the PEL address before this masking.

c) Read address 3C7H (W)

d) Write address 3C8H (R/W)

e) Color reg. 3C9H (R/W)
When write in this port is made, palette No. "0" is written on the superimposing side irrespectively of the read/write palette No. designation. But the transparent bit is not written in.

f) DAC stage reg. 3C7 (R)
This register indicates whether the palette RAM is during the read cycle or the write cycle.

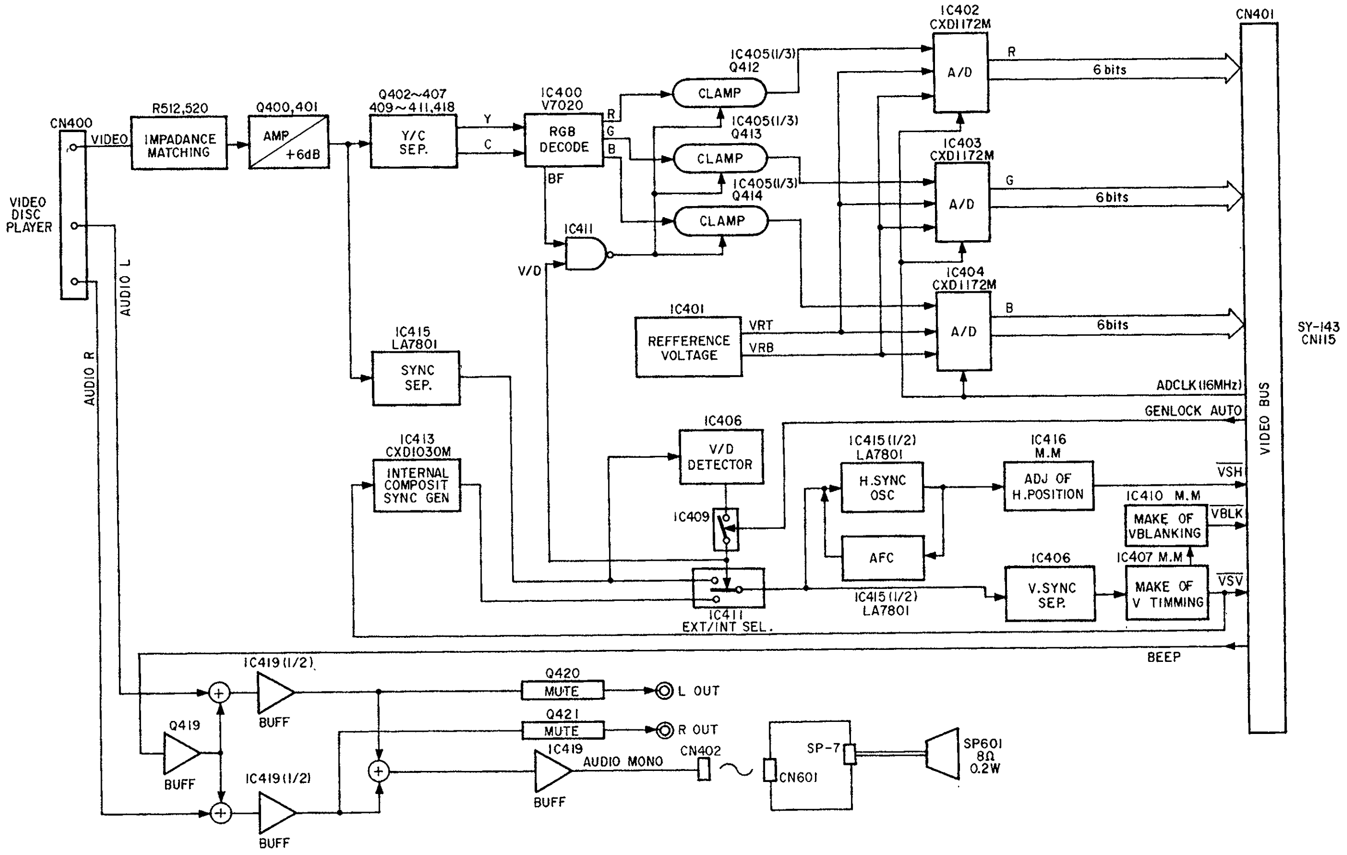
Bit 1	Bit 0	
0	0	...Write palette cycle
1	1	...Read palette cycle

3-3. DECODER, SYNC SIGNAL GENERATOR AND AUDIO CIRCUIT

3-3-1. General

This circuit is mounted on the VS-39 board. It has the following three functions.

1. Decodes the composite video signals of the video disk player into R, G and B signals, and makes analog-to-digital conversion of each signal into a 6 bit digital signal.
2. Generates a composite signal for the internal sync mode.
3. Mixes the audio signal of the video disk player with that of the computer.



CN400
VIDEO
VIDEO DISC PLAYER
AUDIO L
AUDIO R
R512,520
IMPADANCE MATCHING
Q400,401
AMP
+6dB
Q402~407
409~411,418
Y/C SEP.
Y
C
IC400
V7020
RGB DECODE
R
G
B
BF
IC411
V/D
IC405(1/3)
Q412
CLAMP
IC405(1/3)
Q413
CLAMP
IC405(1/3)
Q414
CLAMP
IC402
CXD1172M
A/D
R
6 bits
IC403
CXD1172M
A/D
G
6bits
IC404
CXD1172M
A/D
B
6bits
IC401
REFFERENCE VOLTAGE
VRT
VRB
CN401
VIDEO BUS
SY-143
CN115
ADCLK(16MHz)
GENLOCK AUTO
IC415
LA7801
SYNC SEP.
IC413
CXD1030M
INTERNAL COMPOSIT SYNC GEN
IC406
V/D DETECTOR
IC409
IC411
EXT/INT SEL.
IC415(1/2)
LA7801
H.SYNC OSC
AFC
IC415(1/2)
LA7801
IC416
M.M
ADJ OF H.POSITION
VSH
IC410 M.M
MAKE OF VBLANKING
VBLK
IC406
V.SYNC SEP.
IC407 M.M
MAKE OF V TIMMING
VSV
BEEP
IC419(1/2)
BUFF
Q419
BUFF
IC419(1/2)
BUFF
Q420
MUTE
L OUT
Q421
MUTE
R OUT
IC419
AUDIO MONO
BUFF
CN402
CN601
SP-7
SP601
8Ω
0.2W

Fig. 3-22. Block diagram of VS-39 board

3-3-2. Decoder

3-3-2-1. Video amplifier, Y/C separator circuit

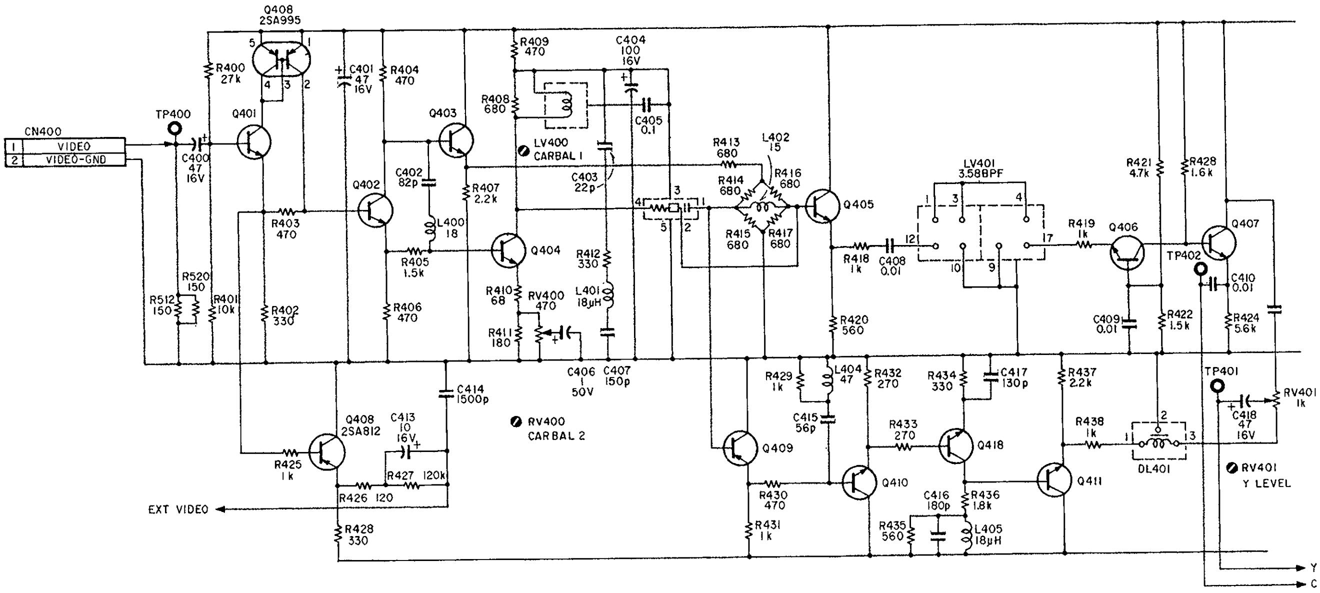

Q408
2SA995
R400
27k
C401
47
16V
R404
470
R409
470
C404
100
16V
R408
680
C405
0.1
TP400
Q401
Q403
CN400
1 VIDEO
2 VIDEO-GND
C400
47
16V
LV400
CARBAL 1
C403
22p
R413
680
L402
15
R414
680
R416
680
Q402
C402
82p
R407
2.2k
Q405
LV401
3.58BPF
R421
4.7k
R428
1.6k
R403
470
L400
18
R415
680
R417
680
R419
1k
Q406
Q407
R405
1.5k
Q404
R412
330
R418
1k
C408
0.01
TP402
C410
0.01
R520
150
R512
150
R401
10k
R402
330
R406
470
R410
68
RV400
470
L401
18µH
R420
560
C409
0.01
R422
1.5k
R424
5.6k
R411
180
C406
1
50V
C407
150p
R429
1k
L404
47
R432
270
R434
330
C417
130p
R437
2.2k
TP401
RV401
1k
C414
1500p
C418
47
16V
Q408
2SA812
C413
10
16V
RV400
CARBAL 2
R433
270
R438
1k
Q409
Q418
DL401
RV401
Y LEVEL
R425
1k
R427 120k
Q410
Q411
R430
470
C416
180p
R436
1.8k
R426 120
EXT VIDEO
R431
1k
R435
560
L405
18µH
R428
330
Y
C

Fig. 3-23.

A video signal is input from the video disk player via pin 1 of CN400 and terminated by R512/R520 (in chips, a 75Ω resistor is not registered) for AC coupling by C400. Q400, Q401 form an amplifier section. By properly selecting the ratio of R402 to R403, the gain is determined, and set to approx. 6 dB by the base of Q402.

Between bases of Q402 to Q405 and Q409 is an Y/C separator circuit. The point is that the video signal 1H delayed by DL400, and a signal from the emitter of Q403 are incremented and decremented by a bridge circuit consisting of R414 to R417 and L402 to create both a luminance signal and a chroma signal. This is explained graphically in Fig. 3-24.

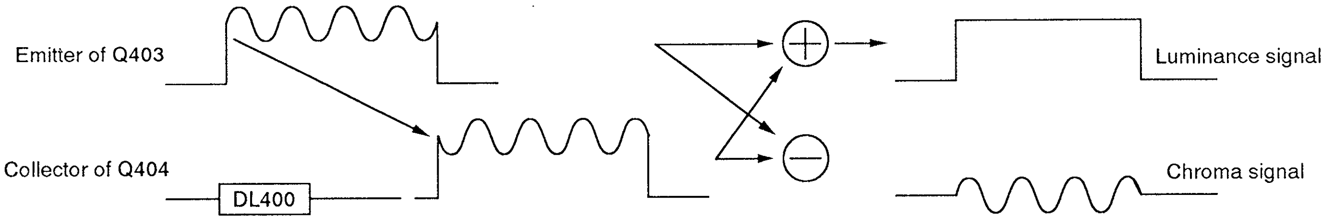

Emitter of Q403
Collector of Q404
DL400
Luminance signal
Chroma signal

Fig. 3-24.

3-3-2-2. RGB decoder

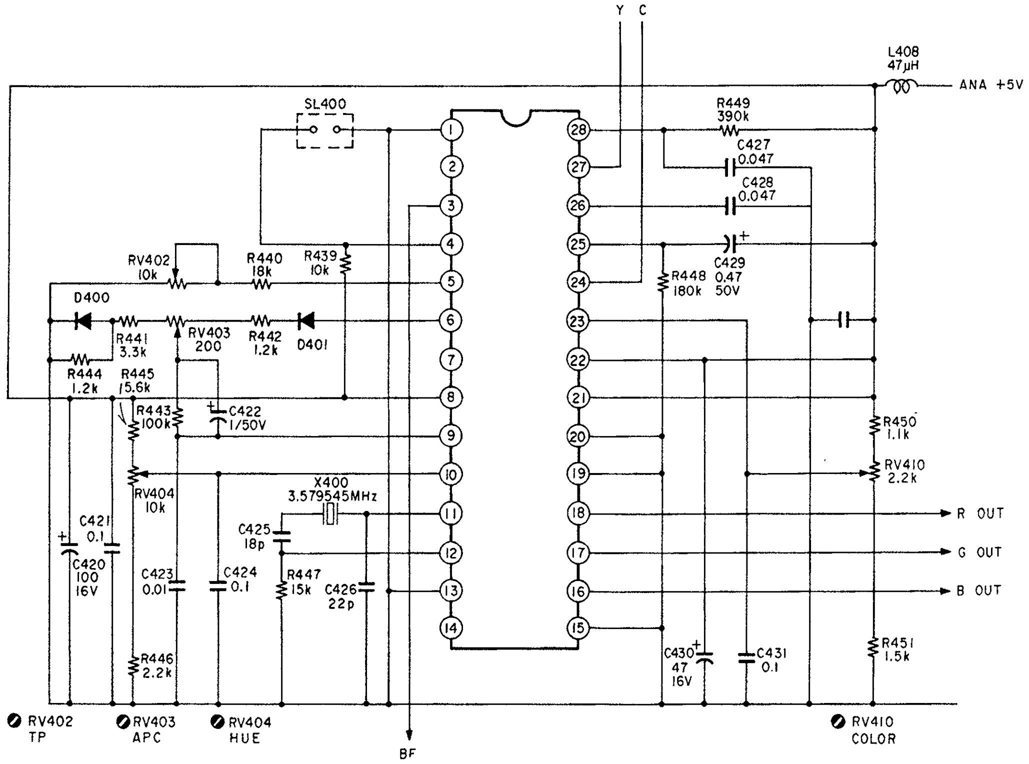
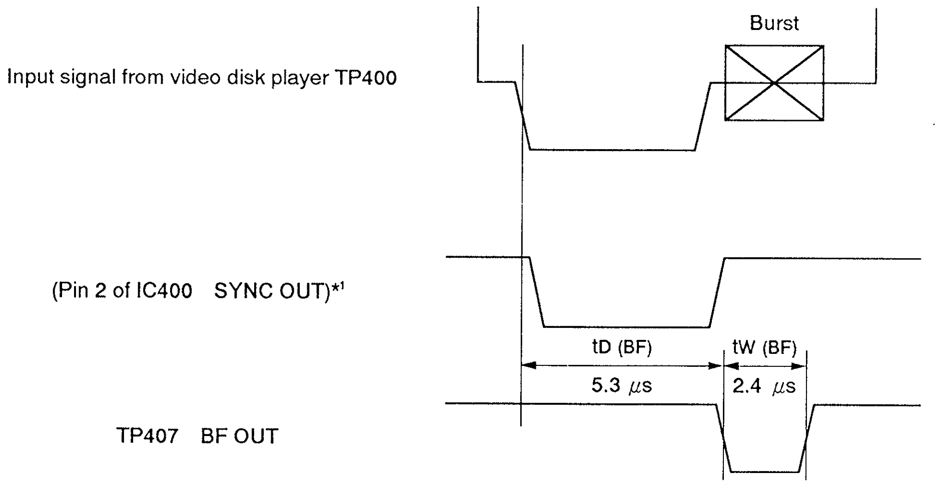

Y
C
L408
47μH
ANA +5V
SL400
R449
390k
C427
0.047
C428
0.047
C429
0.47
50V
R448
180k
RV402
10k
R440
18k
R439
10k
D400
R441
3.3k
RV403
200
R442
1.2k
D401
R444
1.2k
R445
15.6k
R443
100k
C422
1/50V
R450
1.1k
RV410
2.2k
X400
3.579545MHz
RV404
10k
C421
0.1
C420
100
16V
C425
18p
C423
0.01
C424
0.1
R447
15k
C426
22p
R OUT
G OUT
B OUT
C430
47
16V
C431
0.1
R451
1.5k
R446
2.2k
RV402
TP
RV403
APC
RV404
HUE
BF
RV410
COLOR

Fig. 3-25.

IC400 (V7020) is a circuit for converting the Y/C separated signals into analog R, G and B signals. This circuit is enabled only when there is an external video signal from the video disk player in it.

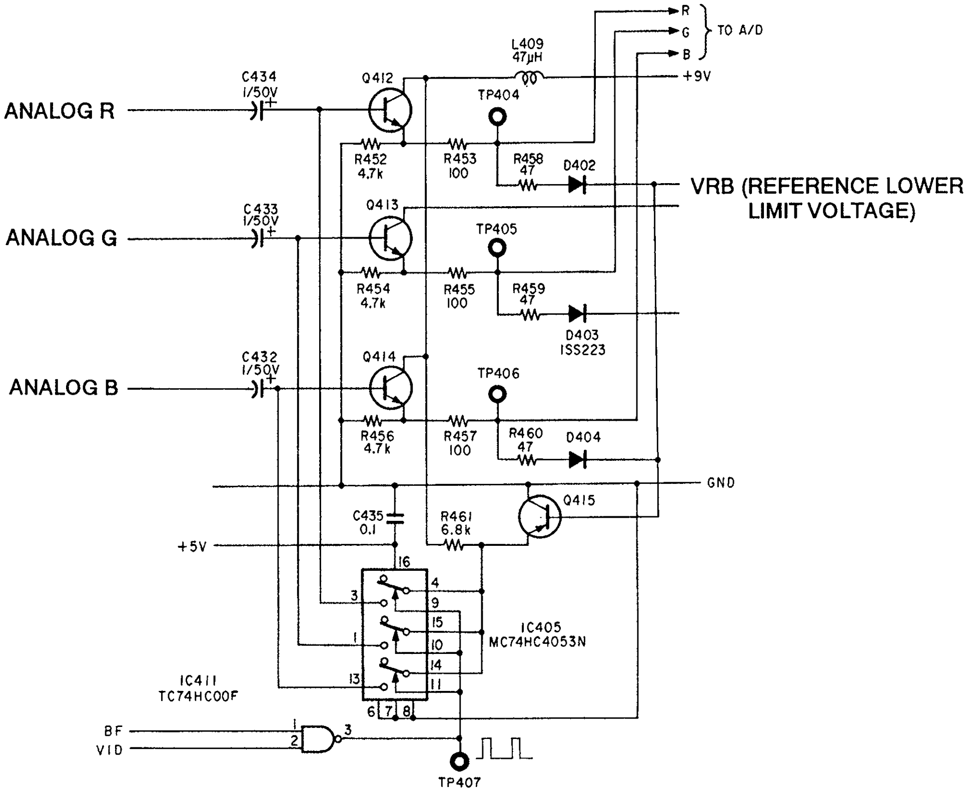
The signal input and output by this IC are BF (burst flag) output to pin 3, APC (Automatic Picture Control) output to pin 5, HUE input to pin 10, in addition to R, G and B signals. Incidentally, Fig. 3-26 shows relations between the input signals of the video disk player and BF.


Burst
Input signal from video disk player TP400
(Pin 2 of IC400 SYNC OUT)*1
tD (BF)
5.3 μs
tW (BF)
2.4 μs
TP407 BF OUT

*1 Unused

Fig. 3-26.

3-3-2-3. Clamp circuit



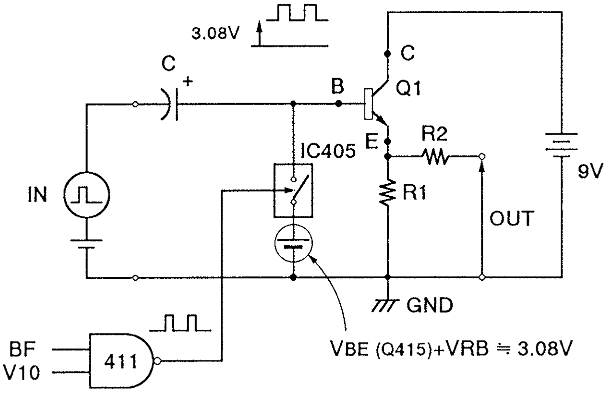
ANALOG R
ANALOG G
ANALOG B
C434
1/50V
C433
1/50V
C432
1/50V
Q412
Q413
Q414
Q415
R452
4.7k
R454
4.7k
R456
4.7k
R453
100
R455
100
R457
100
R458
47
R459
47
R460
47
D402
D403
1SS223
D404
TP404
TP405
TP406
TP407
L409
47μH
+9V
R
G
B
TO A/D
VRB (REFERENCE LOWER LIMIT VOLTAGE)
GND
C435
0.1
R461
6.8k
+5V
IC405
MC74HC4053N
IC411
TC74HC00F
BF
VID
16
4
9
15
10
14
11
3
1
13
6
7
8
1
2
3

Fig. 3-27.

The clamp circuit is for clamping the DC level to certain voltage for input of decoded analog R, G and B signals into the A/D converter described below.

It is Fig. 3-28 where the circuit of Fig. 3-27 is redrawn for better understanding.

The AC component only of the decode signal containing a DC component is passed through by C and fed to the base of Q1. At that time, the output of IC411 repeats H/L level changes with the logical levels of BF and VID. If the level is H, IC405 is turned ON, and the voltage between the base of Q1 and GND is set to the sum (≃ 3.08[V]) of V_{BE} of Q415 and the reference lower limit voltage to be input into the A/D converter. As a result, the DC voltage of 3.08V-V_{BE} (Q1)=2.44[V] is held at the output of Q1. If the output of IC411 is L, the voltage Vc=Q/C ≃ 3.08[V] generated at C is determined, and the output of Q1 is held at 2.44[V] with a voltage drop of V_{BE} (Q1)=0.6[V].



3.08V
C
+
B
C
Q1
E
R2
R1
IC405
IN
OUT
9V
GND
BF
V10
411
VBE (Q415)+VRB ≒ 3.08V

Fig. 3-28.

3-3-2-4. A/D converter and reference voltage circuit

This circuit converts the decoded R, G and B signals into 6 bit ± 1/2 LSB digital signals and outputs them to the SY-143 board. The circuit is necessary for superimposing by the VGA. R, G and B signals are fed to pin 12 of CXD1172M, that is the IC for AD converter, but the input range is dictated by the reference voltage at pins 1 and 7 of IC401. (See Fig. 3-30.) In sampling, the 16 MHz dot clock (ADCLK) created by the SY-143 board is applied to pin 8 of IC402 to IC404 via CN401-A10 on the VS-39 board.

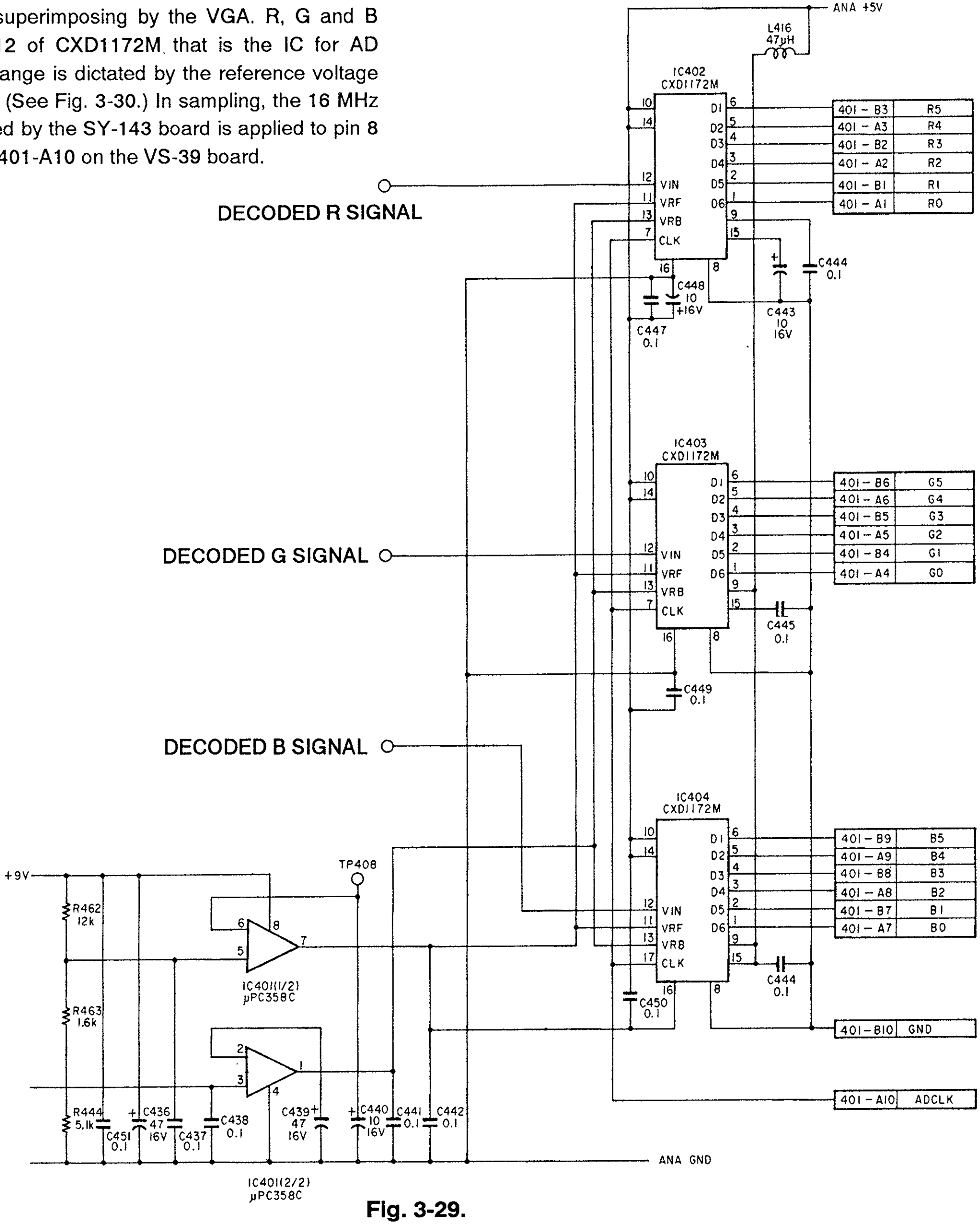

ANA +5V
L416 47μH
IC402 CXD1172M
IC403 CXD1172M
IC404 CXD1172M
VIN VRF VRB CLK
D1 D2 D3 D4 D5 D6
DECODED R SIGNAL
DECODED G SIGNAL
DECODED B SIGNAL
401 - B3 R5
401 - A3 R4
401 - B2 R3
401 - A2 R2
401 - B1 R1
401 - A1 R0
401 - B6 G5
401 - A6 G4
401 - B5 G3
401 - A5 G2
401 - B4 G1
401 - A4 G0
401 - B9 B5
401 - A9 B4
401 - B8 B3
401 - A8 B2
401 - B7 B1
401 - A7 B0
401 - B10 GND
401 - A10 ADCLK
C443 10 16V
C444 0.1
C445 0.1
C447 0.1
C448 10 16V
C449 0.1
C450 0.1
+9V
R462 12k
R463 1.6k
R444 5.1k
TP408
IC401(1/2) μPC358C
IC401(2/2) μPC358C
C451 0.1
C436 47 16V
C437 0.1
C438 0.1
C439 47 16V
C440 10 16V
C441 0.1
C442 0.1
ANA GND

Fig. 3-29.

$$3.22V = \frac{R463+R464}{R462+R463+R464} \times 9V$$

$$2.45V = \frac{R464}{R462+R463+R464} \times 9V$$

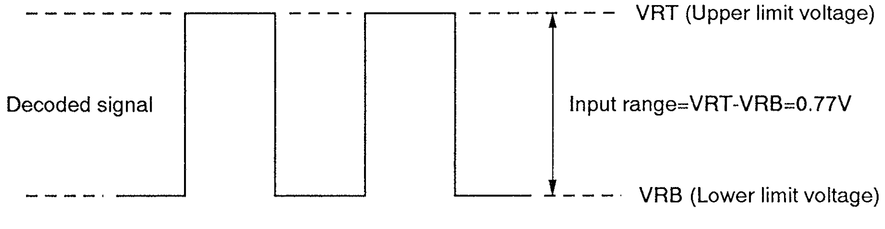

VRT (Upper limit voltage)
Decoded signal
Input range=VRT-VRB=0.77V
VRB (Lower limit voltage)

Fig. 3-30.

3-3-3. Sync Signal Generator Circuit

3-3-3-1. Video ID/Sync select circuit

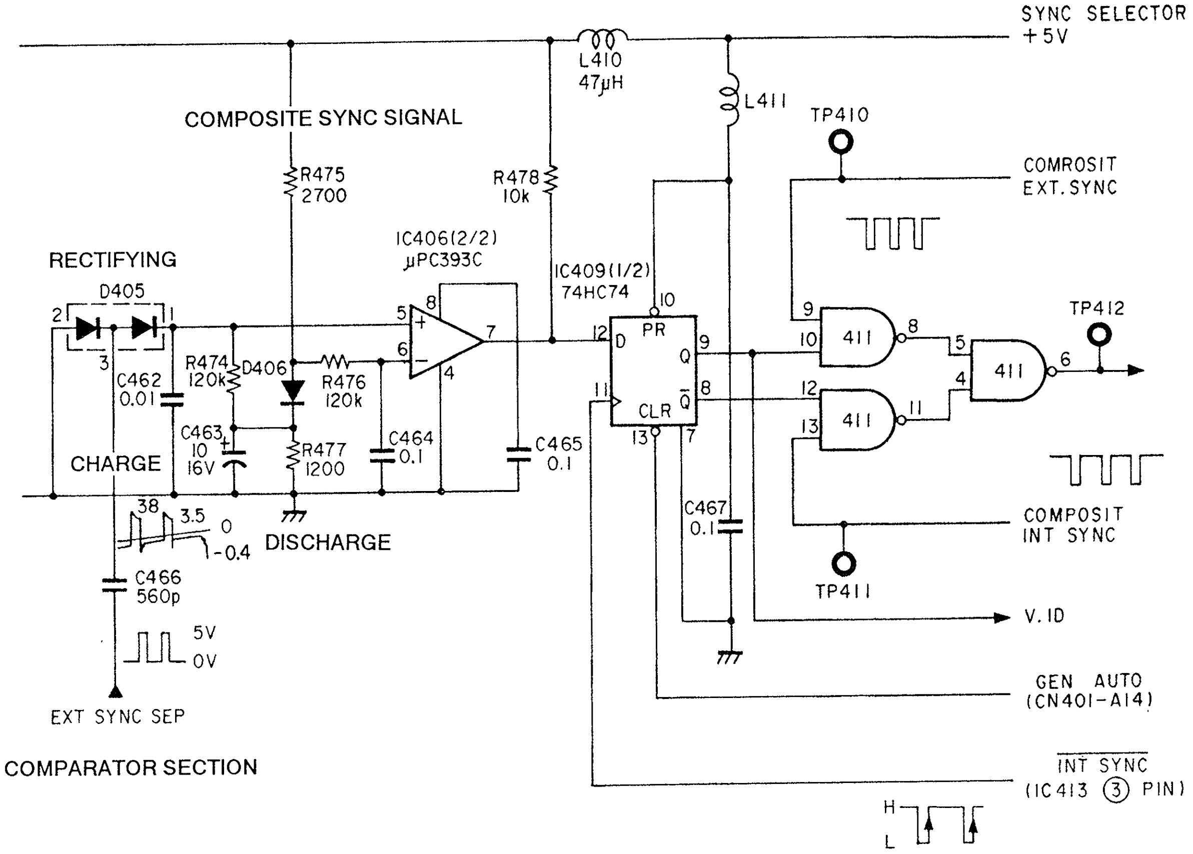

SYNC SELECTOR
+5V
L410
47μH
L411
COMPOSITE SYNC SIGNAL
TP410
R475
2700
R478
10k
COMROSIT
EXT.SYNC
IC406(2/2)
μPC393C
RECTIFYING
D405
IC409(1/2)
74HC74
TP412
R474
120k
D406
R476
120k
C462
0.01
C463
10
16V
R477
1200
C464
0.1
C465
0.1
PR
CLR
D
Q
Q̄
411
CHARGE
38
3.5
0
-0.4
DISCHARGE
C466
560p
5V
0V
C467
0.1
COMPOSIT
INT SYNC
TP411
V. ID
GEN AUTO
(CN401-A14)
INT SYNC
(IC413 ③ PIN)
H
L
EXT SYNC SEP
COMPARATOR SECTION

Fig. 3-31.

This circuit detects the presence or absence of the external sync signal from the video disk player and switches the sync system of the converter between the external side and internal side.

Operation is as follows, providing that the GEN AUTO (CN401-A14) is "H" in level.

- **When Ext. Video signal is present**

  AC coupling by C466 → D405 rectifying → C462 charged to approx. 3 Vdc (so, pin 5 of IC406 is approx. 3 Vdc) → pin 6 of comparator IC406 is 2 Vdc and pin 7 is "H" → as pin 12 of IC409 is brought "H", pin 9 of IC409 is forced "H" and pin 8 "L" in synchronization with the rising edge of internal sync → VID is "H".

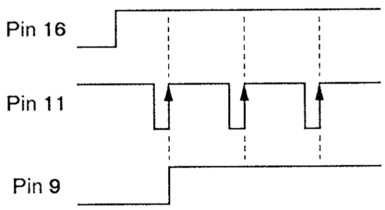

Pin 16
Pin 11
Pin 9

Fig. 3-32.

- **When Ext. Video is absent**

  Pin 5 of IC406 is "L" (Approx. 1.4 Vdc) → pin 7 of IC406 is "L" → as pin 12 of IC409 is brought "L", pin 9 of IC409 is brought "L" and pin 8 "H" in synchronization with the rising edge of the internal sync signal of pin 11 → VID is "L".

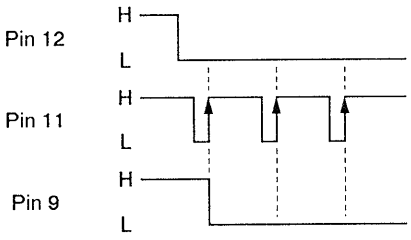

H
Pin 12
L
H
Pin 11
L
H
Pin 9
L

Fig. 3-33.

Next, how the sync selector operates depending upon the VID level is shown below.

- When VID is "H".

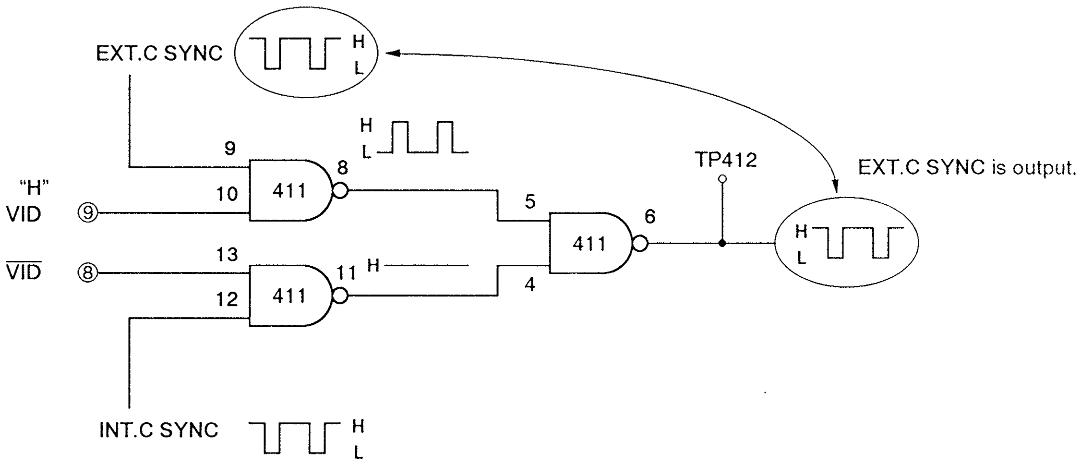

EXT.C SYNC
H
L
9
10
8
H
L
"H"
VID
⑨
411
5
TP412
EXT.C SYNC is output.
6
411
H
L
VID
⑧
13
12
411
11
H
4
INT.C SYNC
H
L

Fig. 3-34.

- When VID is "L".

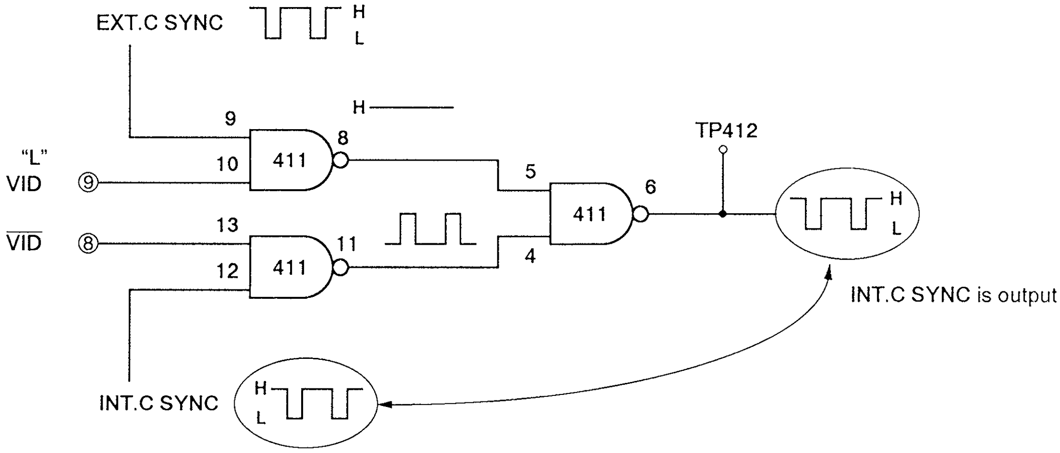

EXT.C SYNC
H
L
H
9
8
TP412
"L"
VID
⑨
10
411
5
6
411
H
L
VID
⑧
13
12
411
11
4
INT.C SYNC is output
INT.C SYNC
H
L

Fig. 3-35.

3-3-3-2. Sync separator and AFC

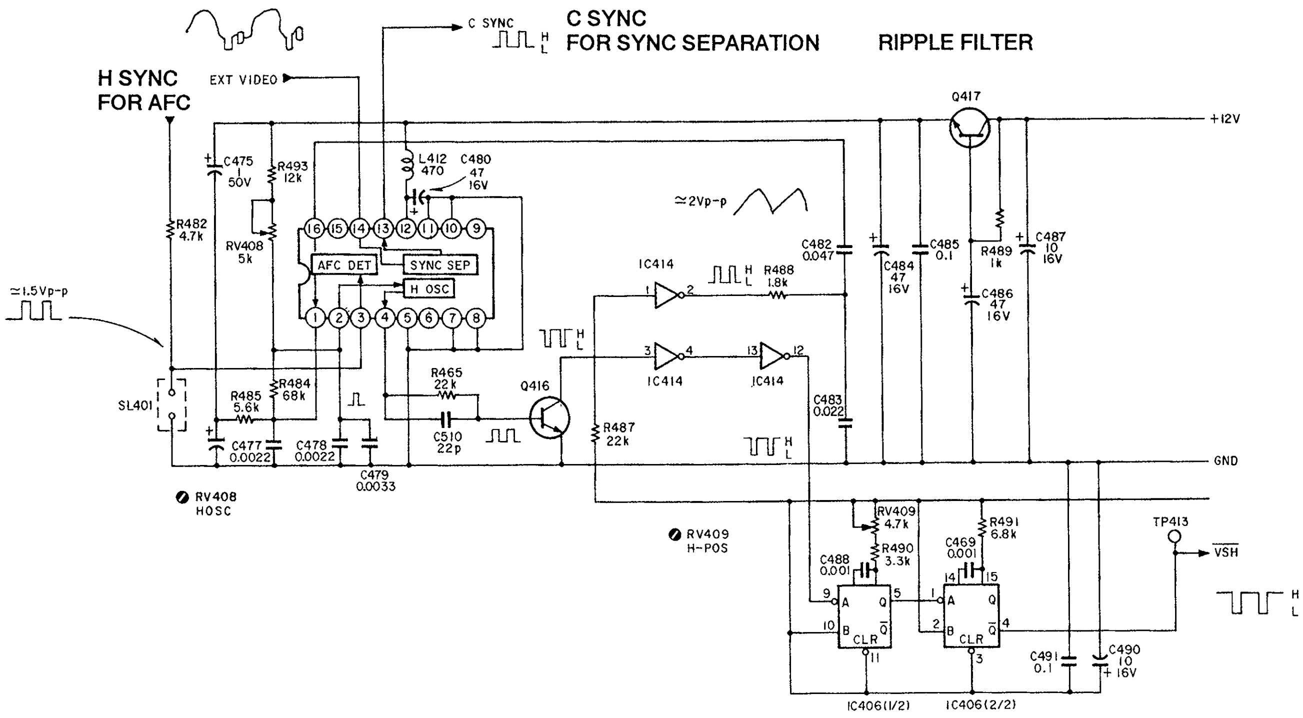

C SYNC
C SYNC
FOR SYNC SEPARATION
RIPPLE FILTER
H SYNC
FOR AFC
EXT VIDEO
Q417
+12V
C475
1
50V
R493
12k
L412
470
C480
47
16V
≃2Vp-p
R482
4.7k
RV408
5k
AFC DET
SYNC SEP
H OSC
C482
0.047
C484
47
16V
C485
0.1
R489
1k
C487
10
16V
C486
47
16V
IC414
R488
1.8k
≃1.5Vp-p
R465
22k
Q416
IC414
IC414
SL401
R485
5.6k
R484
68k
C477
0.0022
C478
0.0022
C510
22p
R487
22k
C483
0.022
GND
C479
0.0033
RV408
HOSC
RV409
H-POS
RV409
4.7k
R490
3.3k
R491
6.8k
C488
0.001
C469
0.001
TP413
VSH
CLR
CLR
C491
0.1
C490
10
16V
IC406(1/2)
IC406(2/2)
H
L

Fig. 3-36.

This circuit has the function (sync separation) of separating the H, V containing composite signal from the external video signal, i.e., a video signal from the video disk player, the automatic frequency control function (AFC), and external video reference sync generation function for stabilizing the external sync lock.

The sync separator circuit is first described. After passing through a buffer consisting of Q401 and Q408, the video signal of the video disk player subjected to sync separating slice level cutting by R426, R427, separation time constant determination by R427, C413, and low-pass filter forming by R426 and R414 and then applied to pin 14 of IC415 shown in Fig. 3-36. Incidentally, slice level resistance setting is done in such a way that operation is enabled even at 1/2 sync (≒ 140 mV). The sync separated signal is output from pin 13.

Next, the AFC is discussed. The phase of the sawtooth wave obtained by integrating the C sync going into pin 3 of IC415 and pin 4 OSC output to pin 16 by R488, C482 and C483 is compared. The phase error current is output from pin 1, and it is smoothed by R485, C476 and C477, phase error voltage is obtained. The phase error voltage is normally set to approx. 6 Vdc. When the sawtooth wave f tends to go up, the phase error voltage goes down. Also, when the sawtooth wave f tends to go down, the phase error voltage goes up. Therefore, the pin 4 output frequency can be stabilized.

3-3-3-3. Vertical sync signal detector circuit

This circuit detects a vertical sync cycle in the composite sync signal to generate a "VSV" signal.

The composite sync signal (C-SYNC), after being integrated by R466 and C454, is voltage compared with the 2.5 Vdc threshold voltage. The detected V sync is masked for approx. one field (13 msec) by the monostable multivibrator to avoid erratic operation of the comparator due to noise etc. on the video signal.

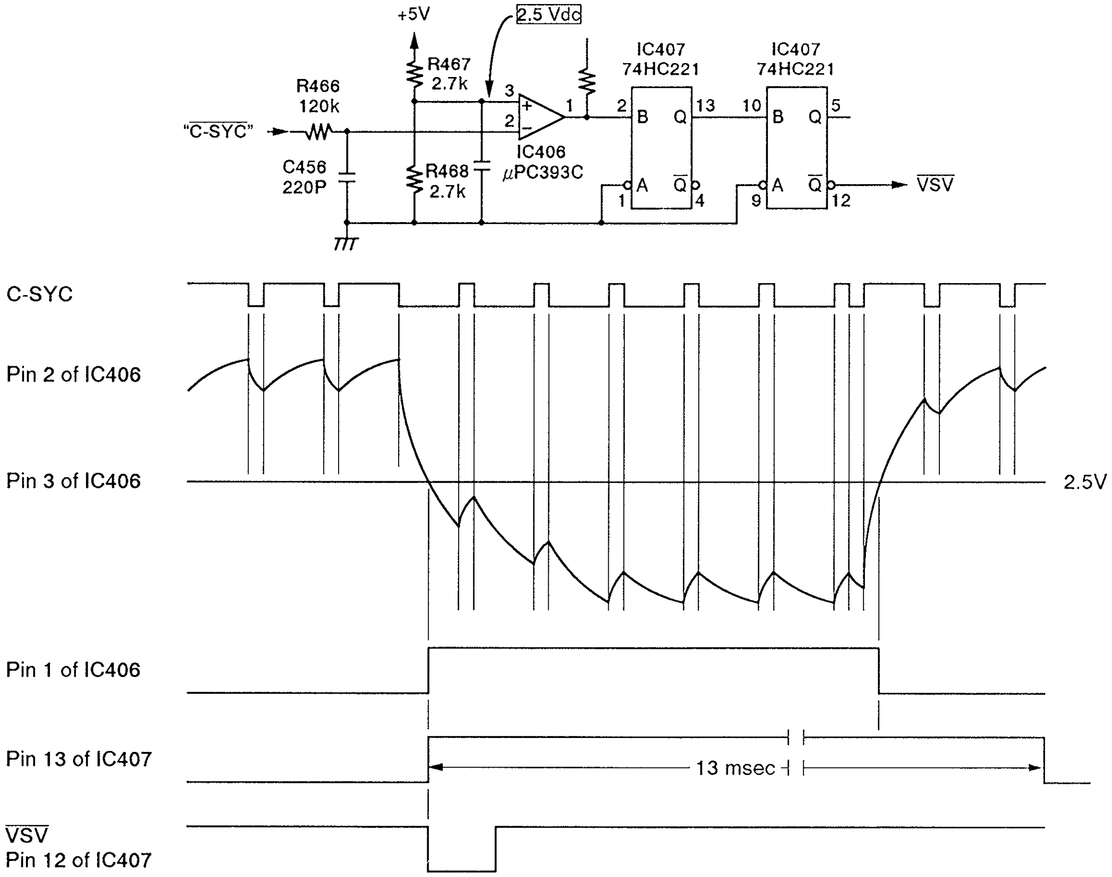


Fig. 3-37.

3-3-3-4. Horizontal sync signal generator circuit (IC408, IC414, IC415 and IC416)

This circuit eliminates equalizing pulses spaced 1/2H from the composite signal (C-SYNC) by IC408, passed through the AFC circuit at pin 3 of IC415, and adjusts the position and width of the H sync signal output from pin 4 by IC416 for use as VSH.

If the H sync is missing in the external video signal, such missing can be interpolated at the cycle averaged by the previous H sync.

3-3-3-5. Internal sync signal generator circuit (IC413)

If there is no input from the video disk player section in the auto-genlock mode, or when it is the forced internal sync mode by the software, the pin 3 (INT C sync) signal of IC413 can be supplied to pin 3 of IC415 (LA7801).

The monostable multivibrator IC412 broadens the pulse width of the H sync to the extent of approx. 32 µsec with C469 and R480 to detect the field by the V sync clock.

IC413 (CXD1030M) accepts the VINT input of pin 17 only when the VID is "L" level (with an input from the video disk player), and initially sets IC413 at the every beginning of the 1st field during which time the VINT signal edge falls.

In RV407, its timing position is adjusted, to bring the external sync into phase with the internal sync.

Incidentally, when the internal sync mode has been selected, VINT ceases to be performed. In the forced internal sync mode, therefore, the internal sync signal is brought out of synchronization with the external sync signal. In this state, however, muting is applied to the video signal from the video disk player software-wise. Thus, the out-of-sync picture is not displayed.

3-3-4. Audio Circuit

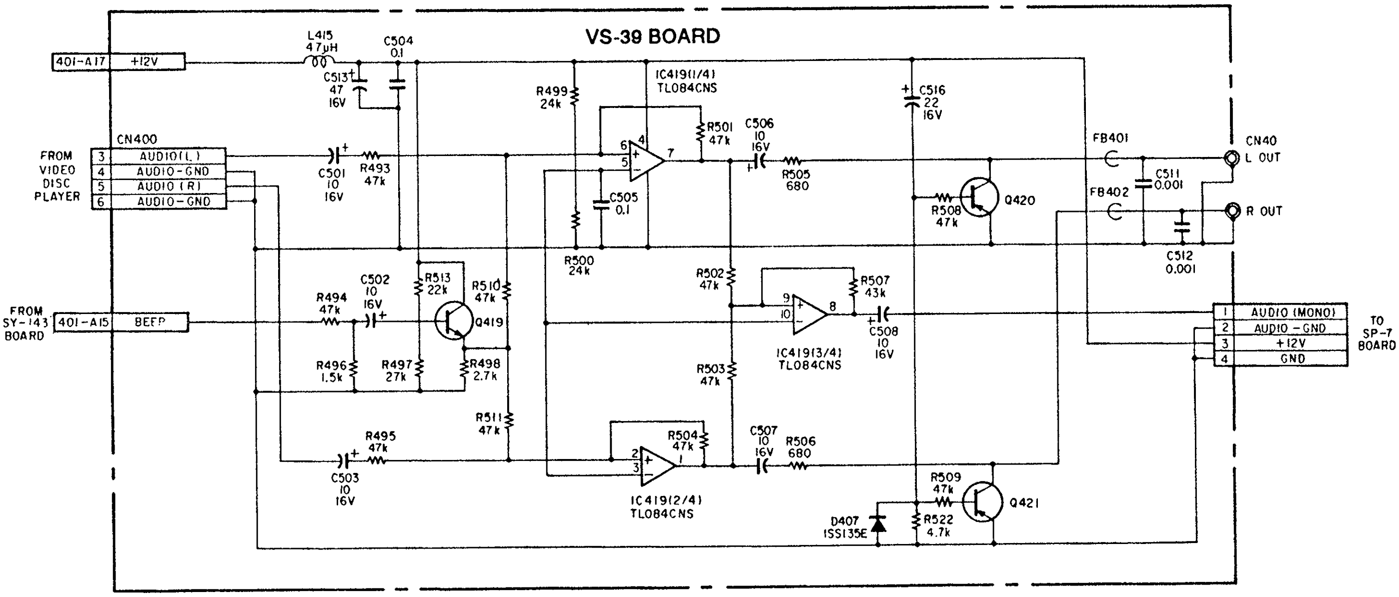

VS-39 BOARD
401-A17
+12V
L415
47μH
C504
0.1
C513
47
16V
R499
24k
IC419(1/4)
TL084CNS
C516
22
16V
CN400
FROM VIDEO DISC PLAYER
3 AUDIO(L)
4 AUDIO-GND
5 AUDIO(R)
6 AUDIO-GND
C501
10
16V
R493
47k
R501
47k
C506
10
16V
R505
680
C505
0.1
R500
24k
FB401
FB402
C511
0.001
C512
0.001
CN40
L OUT
R OUT
R508
47k
Q420
FROM SY-143 BOARD
401-A15
BEEP
C502
10
16V
R494
47k
R513
22k
R510
47k
Q419
R496
1.5k
R497
27k
R498
2.7k
R511
47k
R502
47k
R507
43k
C508
10
16V
IC419(3/4)
TL084CNS
R503
47k
1 AUDIO (MONO)
2 AUDIO-GND
3 +12V
4 GND
TO SP-7 BOARD
R495
47k
C503
10
16V
R504
47k
IC419(2/4)
TL084CNS
C507
10
16V
R506
680
R509
47k
Q421
D407
1SS135E
R522
4.7k

Fig. 3-38.

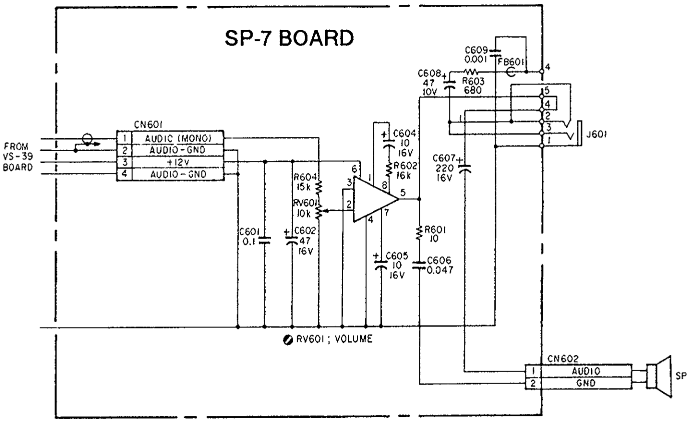

SP-7 BOARD
C609
0.001
FB601
C608
47
10V
R603
680
J601
CN601
FROM VS-39 BOARD
1 AUDIC (MONO)
2 AUDIO-GND
3 +12V
4 AUDIO-GND
C604
10
16V
R602
16k
C607
220
16V
R604
15k
RV601
10k
C601
0.1
C602
47
16V
R601
10
C605
10
16V
C606
0.047
RV601 ; VOLUME
CN602
1 AUDIO
2 GND
SP

Fig. 3-39.

The audio circuit can be divided into a circuit for mixing the sound of the video disk player and that of the computer side for output by stereo from the line out, and a circuit for output of a monaural signal from the speaker built in the equipment body. IC419 (TL084) is used as a buffer of gain 1, and the reference voltage is used for cost reduction of the power with +6V as virtual GND. Generally, if the operational amplifier that requires both powers is used on single power, the input dynamic range is narrowed. In this circuit, however, linearity can be held even if the 5 Vp-p sine wave is input. No practical problem is therefore anticipated. On the other hand, the sound of the computer side is input from CN401-A15 by software control. The sound level takes balance when it is mixed with the sound of the video disk player side. It is thus decided on based on the splitting ratio of R494 to R496. (≃ 0.2 Vp-p)

The monaural sound passes through the sound amplifier LM386 on the SP-7 board, and then branches into the headphone jack J601 and the connector CN602 to the built-in speaker. Incidentally, the SP output is 0.2W, 8Ω . Also, Q420, Q421 form a mute circuit when the power of VIW-5000 is ON.

3-4. POWER CIRCUIT

3-4-1. Power ON/OFF Operation

The AC power fed from the AC inlet is supplied to the video disk player via the power switch of the rear panel, fuses, 2P plug and socket.
With the front power switch of the video disk player turned ON, the 5V line of the video disk player starts, in turn causing the current of approx. 20 mA to be flowed to the computer power starting photocoupler. Now, the switching drive oscillator is started so that the power of the computer is turned on.

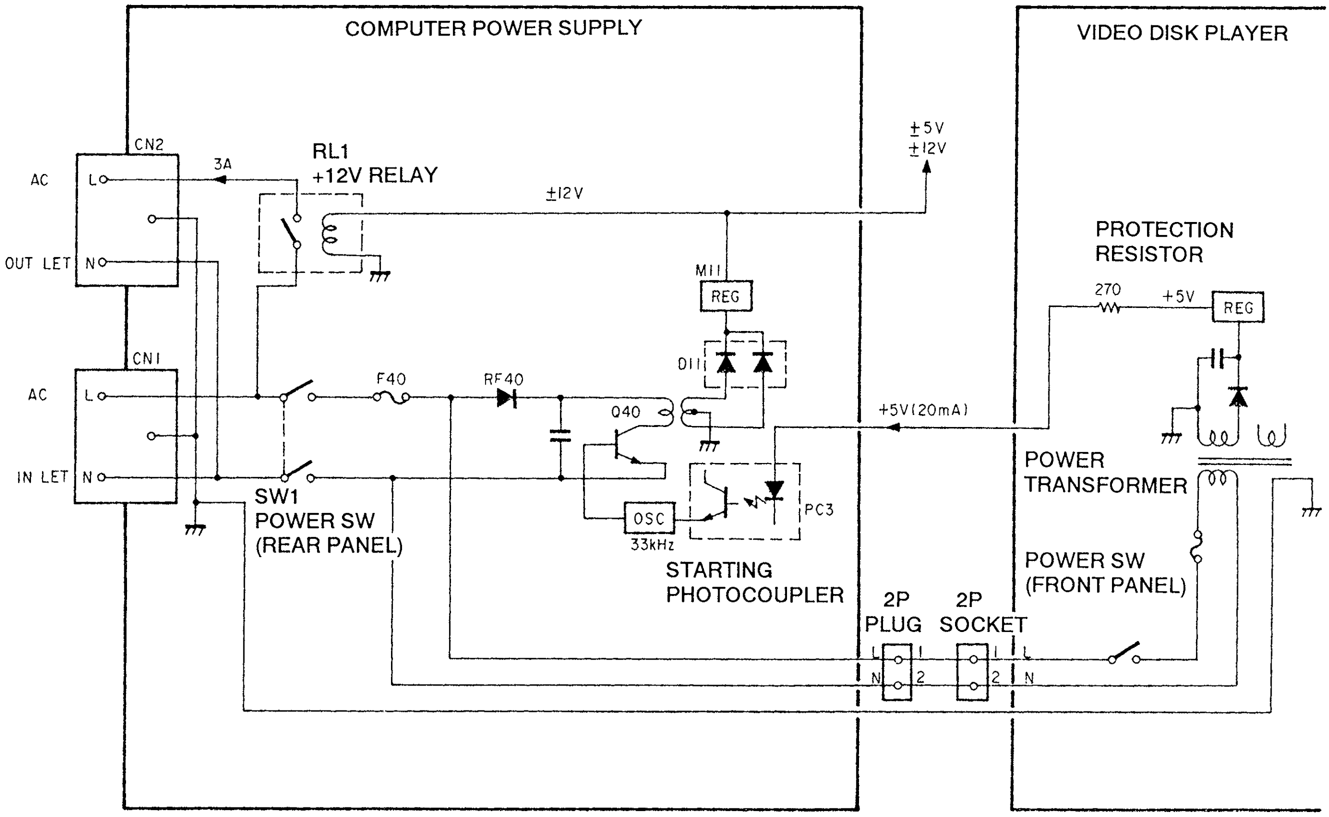

COMPUTER POWER SUPPLY
VIDEO DISK PLAYER
CN2
AC
OUT LET
L
N
3A
RL1
+12V RELAY
±12V
±5V
±12V
M11
REG
D11
CN1
AC
IN LET
F40
RF40
Q40
OSC
33kHz
PC3
SW1
POWER SW
(REAR PANEL)
STARTING
PHOTOCOUPLER
+5V(20mA)
PROTECTION
RESISTOR
270
+5V
REG
POWER
TRANSFORMER
POWER SW
(FRONT PANEL)
2P
PLUG
2P
SOCKET
1
2

Fig. 3-40.

3-4-2. Circuit Descriptions

This power supply is a switching type operating based on the RCC (ringing choke converter) system. The power supply performs switching operation on the ringing of the circuit. It saves energies in its transformer while the primary side switching transistor is ON. It supplies the energies to the load through the rectifying diode when the transistor is turned OFF.

3-4-2-1. Rectifying circuit

This circuit charges the current to the capacitors (C50, C51) based on the full-wave rectification system using RF40 to create DC power.

3-4-2-2. Switching circuit

This circuit causes weak current to be flowed to the base of a switching transistor (Q40) from capacitors (C50,C51) via R40, R41 and R42. With this current, the current h FE times the transistor collector is flowed to excite the transformer (T40). Voltage is built up between base windings 1 and 2 of the transformer T40, so that the current flows to the base of Q40 via D40, R48, R49. As a result, Q40 is turned ON.

(*) When the collector current of Q40 increases, and the voltage drop of the emitter resistor (R44) becomes in excess of the preset value, the voltage is added to the base bias of a drive transistor Q41, to cause Q41 to be turned ON.

When the base current of Q40 ceases to exist, Q40 is turned OFF. As Q40 is turned OFF, flyback voltage is generated at T40 to supply the power to the secondary side. When the current ceases to flow to the secondary side of T40, and when the current begins to flow to the base of Q40 by ringing, Q40 is turned ON once again. The process is now repeated as from (*).

3-4-2-3. Output regulated circuit

This circuit detects the output voltage with R03, R04 and RV01 to control the ON time of Q40 for regulating the output. Assuming that the output voltage has now gone up beyond the preset level, the current flowing to the control IC (M01) increases, in turn causing the diode side current of the photocoupler (PC10) to increase also. With this, the current of the transistor side of PC01 increases, so that the Q41 is turned ON. Now, the ON time of Q40 is shortened, and the output voltage drops.

The output voltage changes according to RV01, however, rotate it as it is set to the specified voltage.

The +12V, −12V, and −5V circuits regulate the output with the respective series regulators (M11, M21, M22).

3-4-2-4. Remote ON/OFF circuit

When +5V is applied to +5V IN with the AC power applied, (PC03) is turned ON, (Q42, Q43) is turned OFF, and the output builds up. Upon removal of this voltage, the operation is reversed, and the output drops.

3-4-2-5. Overvoltage protection circuit

This protection circuit is mounted in the +5V circuit. When the output voltage increases beyond the specified level, the current flows to PC02 to cause TH41 to be turned ON. As a result, the transistor (Q42) which stops frequency oscillation is turned ON, to drop the output. TH41 remains ON unless the AC power is cut off.

3-4-2-6. Overcurrent protection circuit

This protection circuit limits the total output power. It detects the current flowing to Q40 with R44. When the specified current flows, Q41 is turned ON, to shorten the ON time of Q40, thereby causing the output voltage to decrease for power limiting. Power setting can be varied by using RV40, but do not attempt to turn it except when deemed absolutely necessary. Otherwise, a damage to it may result.

3-4-2-7. Overheat protection circuit

This protection circuit detects the temperature of +5V rectifying diode (D01) to preclude the possibility of parts damage when the fan stopped. When the temperature goes up beyond the specified level, the transistor (Q01) is turned ON, and the rest of the process is the same as in the case of the overvoltage protection circuit.

3-4-2-8. Input surge current limiting circuit

This circuit limits the charge current flowing to C50, C51 with R43-1, R43-2 and PT40, PT41 when the AC power is ON.

3-4-2-9. PG signal circuit

This circuit outputs a read signal with the +5V output voltage signal IC (M31). When the output builds up, the level is "H", but when it drops, it is "L" TTL level.

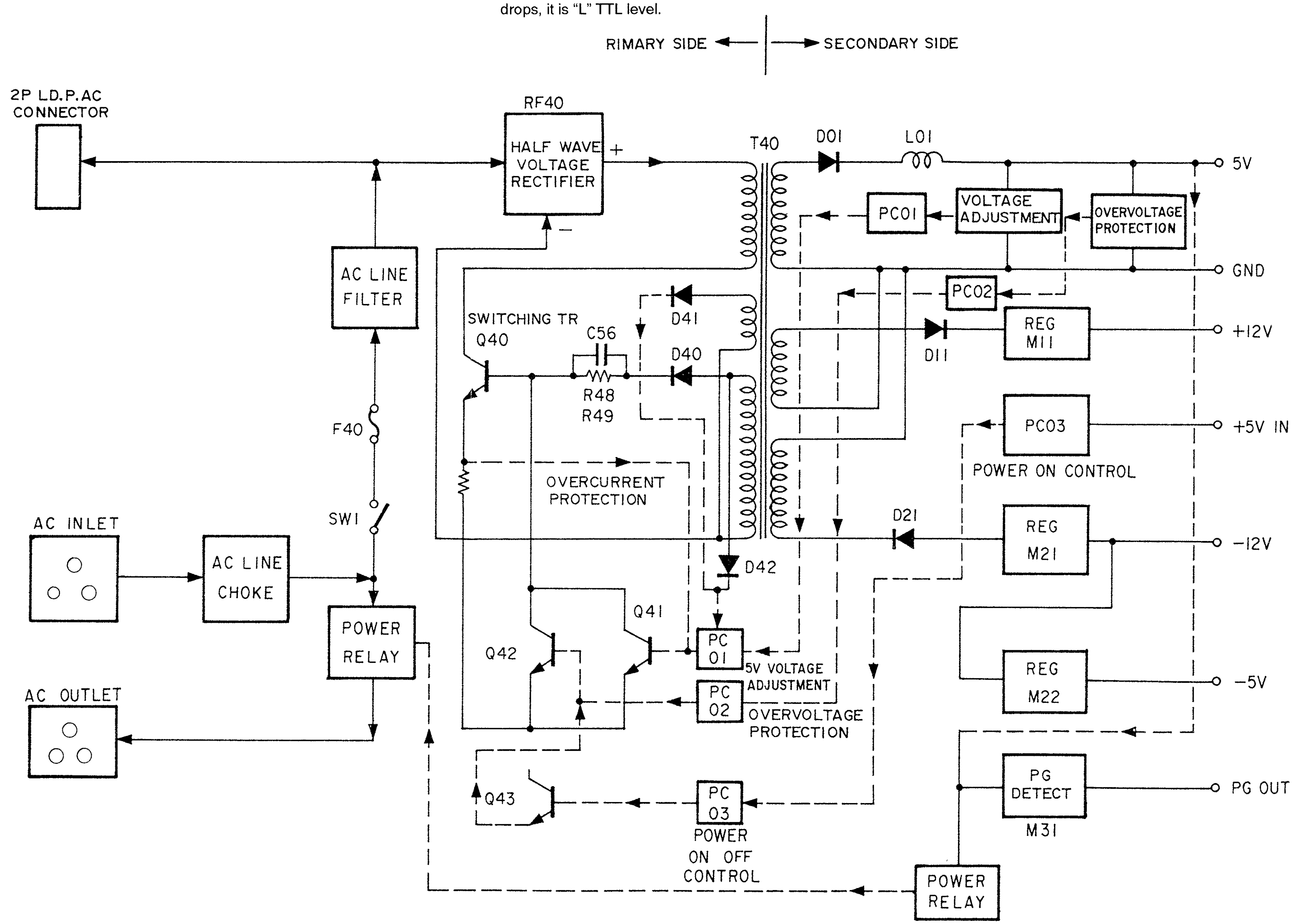
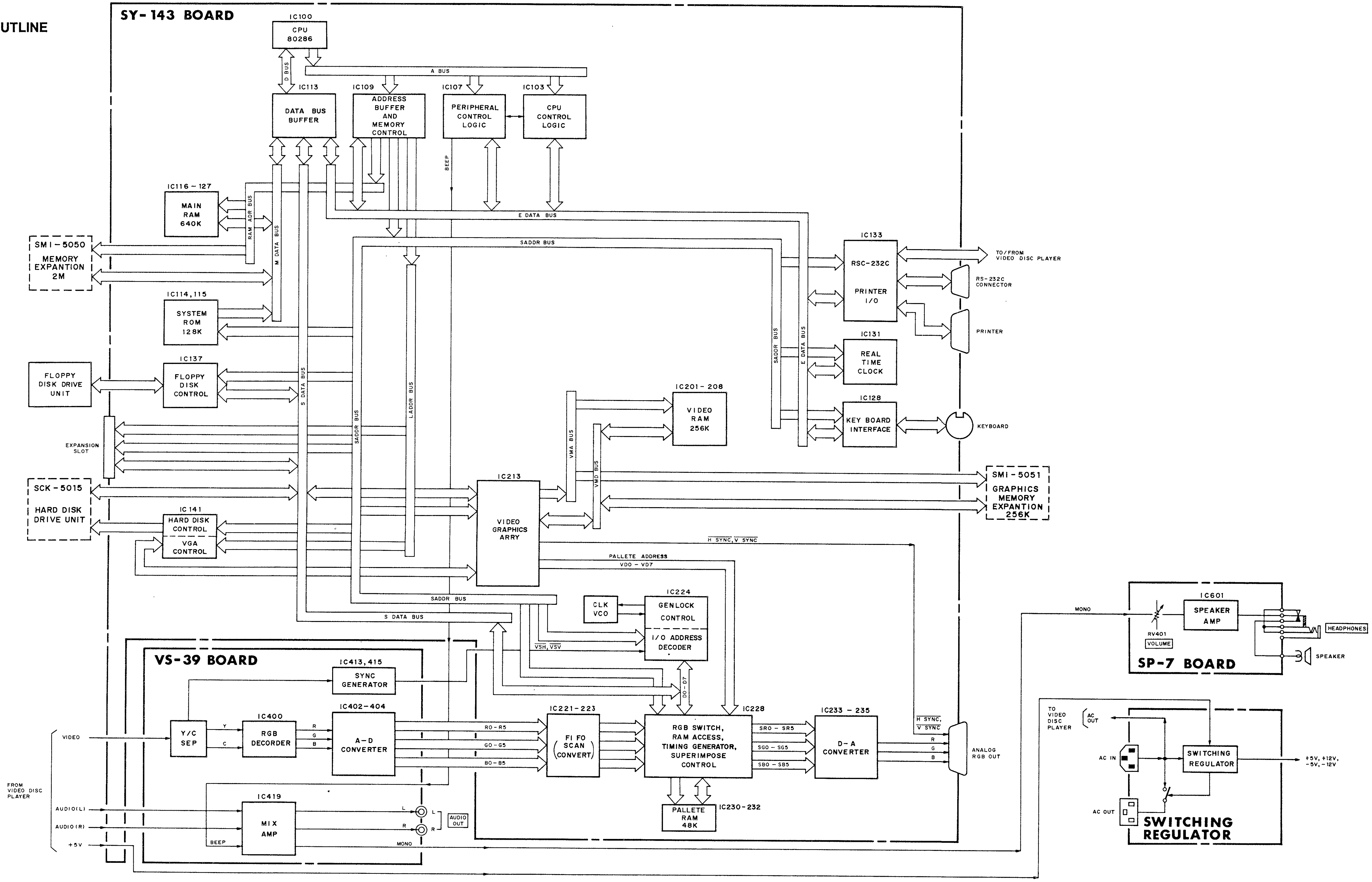

RIMARY SIDE
SECONDARY SIDE
2P LD.P.AC CONNECTOR
RF40
HALF WAVE VOLTAGE RECTIFIER
+
−
T40
D01
L01
5V
VOLTAGE ADJUSTMENT
OVERVOLTAGE PROTECTION
PC01
GND
PC02
REG M11
+12V
D11
AC LINE FILTER
SWITCHING TR Q40
C56
D41
D40
R48
R49
F40
PC03
+5V IN
POWER ON CONTROL
OVERCURRENT PROTECTION
SW1
AC INLET
AC LINE CHOKE
D21
REG M21
−12V
D42
POWER RELAY
Q41
Q42
PC 01
5V VOLTAGE ADJUSTMENT
PC 02
OVERVOLTAGE PROTECTION
REG M22
−5V
AC OUTLET
PG DETECT
M31
PG OUT
Q43
PC 03
POWER ON OFF CONTROL
POWER RELAY

Fig. 3-41. Computer section power supply block diagram

CHAPTER 4
BLOCK DIAGRAM

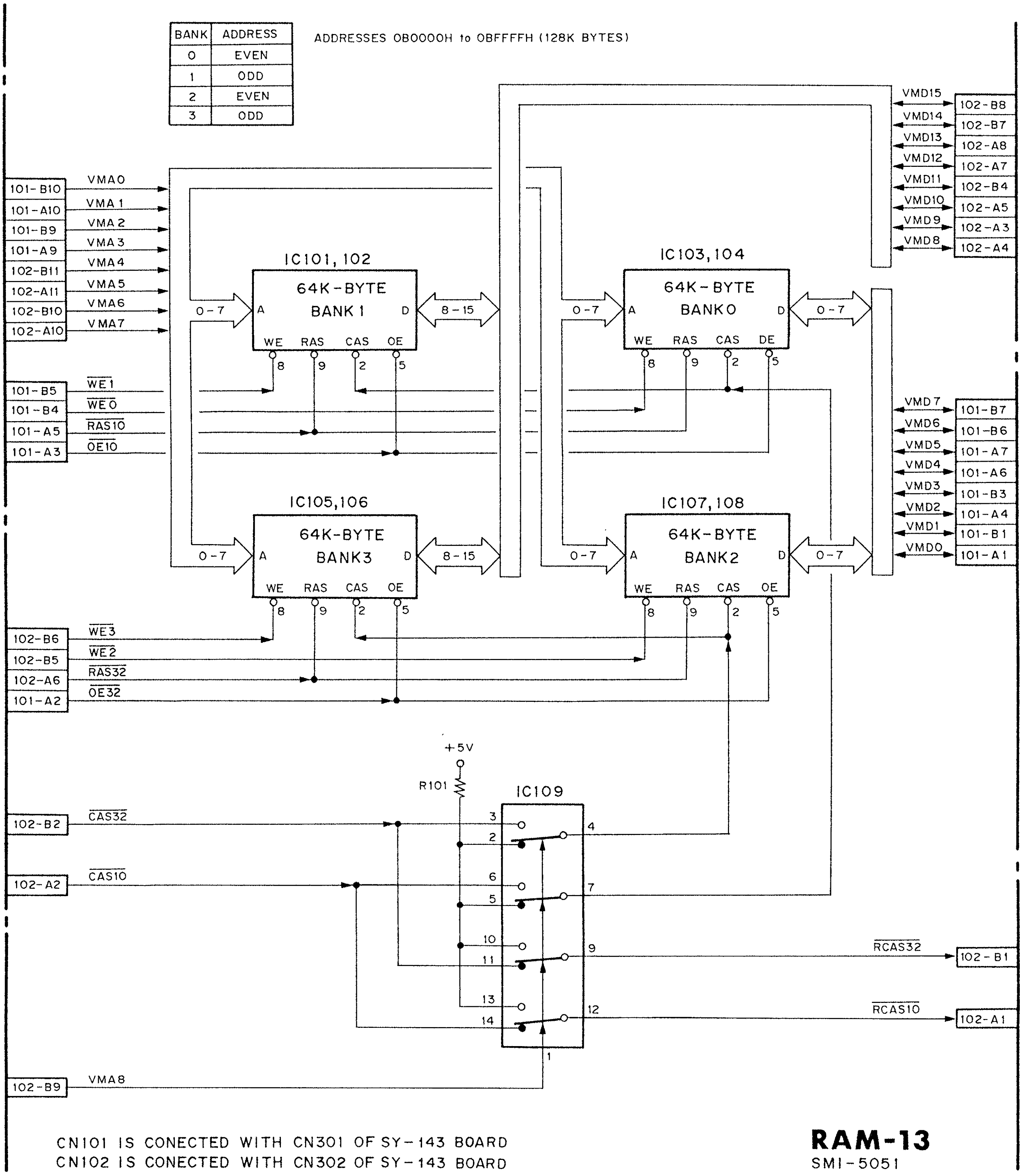
4-1. COMPUTER OUTLINE


SY-143 BOARD
IC100
CPU
80286
D BUS
A BUS
IC113
DATA BUS BUFFER
IC109
ADDRESS BUFFER AND MEMORY CONTROL
IC107
PERIPHERAL CONTROL LOGIC
IC103
CPU CONTROL LOGIC
BEEP
E DATA BUS
IC116 - 127
MAIN RAM 640K
RAM ADR BUS
M DATA BUS
SADDR BUS
SMI - 5050
MEMORY EXPANTION 2M
IC114, 115
SYSTEM ROM 128K
IC137
FLOPPY DISK CONTROL
FLOPPY DISK DRIVE UNIT
S DATA BUS
LADDR BUS
EXPANSION SLOT
SCK - 5015
HARD DISK DRIVE UNIT
IC141
HARD DISK CONTROL
VGA CONTROL
IC133
RSC-232C
PRINTER I/O
TO/FROM VIDEO DISC PLAYER
RS-232C CONNECTOR
PRINTER
IC131
REAL TIME CLOCK
IC128
KEY BOARD INTERFACE
KEYBOARD
IC201 - 208
VIDEO RAM 256K
VMA BUS
VMD BUS
IC213
VIDEO GRAPHICS ARRY
SMI - 5051
GRAPHICS MEMORY EXPANTION 256K
H SYNC, V SYNC
PALLETE ADDRESS
VD0 - VD7
SADDR BUS
S DATA BUS
CLK VCO
IC224
GENLOCK CONTROL
I/O ADDRESS DECODER
VSH, VSV
D0 - D7
VS-39 BOARD
IC413, 415
SYNC GENERATOR
FROM VIDEO DISC PLAYER
VIDEO
AUDIO(L)
AUDIO(R)
+5V
Y/C SEP
Y
C
IC400
RGB DECORDER
R
G
B
IC402-404
A-D CONVERTER
R0 - R5
G0 - G5
B0 - B5
IC221-223
FIFO SCAN (CONVERT)
IC228
RGB SWITCH, RAM ACCESS, TIMING GENERATOR, SUPERIMPOSE CONTROL
IC230-232
PALLETE RAM 48K
SR0 - SR5
SG0 - SG5
SB0 - SB5
IC233 - 235
D-A CONVERTER
H SYNC, V SYNC
R
G
B
ANALOG RGB OUT
IC419
MIX AMP
BEEP
L
R
MONO
AUDIO OUT
MONO
IC601
SPEAKER AMP
RV401
VOLUME
HEADPHONES
SPEAKER
SP-7 BOARD
TO VIDEO DISC PLAYER
AC OUT
AC IN
AC OUT
SWITCHING REGULATOR
+5V, +12V, -5V, -12V
SWITCHING REGULATOR

4-2. SY-143 BOARD

GATE ARRAY
FIFO
SELECTOR
SUPER MODE SELECTER
STATIC RAM
RAM ACCESS CONTROL
ADDRESS SELECT
LATCH
I/O CONTROL
VIDEO RAM
VIDEO GRAPHICS ARRAY
PHASE COMPARATOR
LPF
VCO
BUFFER
CPU
AT CONTROL LOGIC
AT PERIPHERAL CONTROL LOGIC
AT DATA BUFFER
ADDRESS BUFFER AND MEMORY CONTROLLER
REAL TIME CLOCK
DUS-307
OPERATION REGISTER
DATA REGISTER
MASTER STATUS REGISTER
CONTROL REGISTER
HOST INTERFACE
DUAL OSC.
DIGITAL DATA SEPARATOR
CLOCK AND TIMING GENERATOR
DATA ENCODER AND DECODER
CRC GENERATOR
WRITE PRECOM-PENSATION
ALU
RAM
INSTRUCTION DECODE
PROGRAM COUNTER
ROM
FLAG LOGIC
STATE MACHINE
MS TIMER
DISK INTERFACE CONTROL REGISTER
FLOPPY DISK CONTROLLER
DUAL UARTS AND PRINTER PORT
UART
SELECT AND CONTROL LOGIC
PARALLEL PORT
KEYBOARD INTERFACE

4-3. RAM-13



BANK	ADDRESS
0	EVEN
1	ODD
2	EVEN
3	ODD

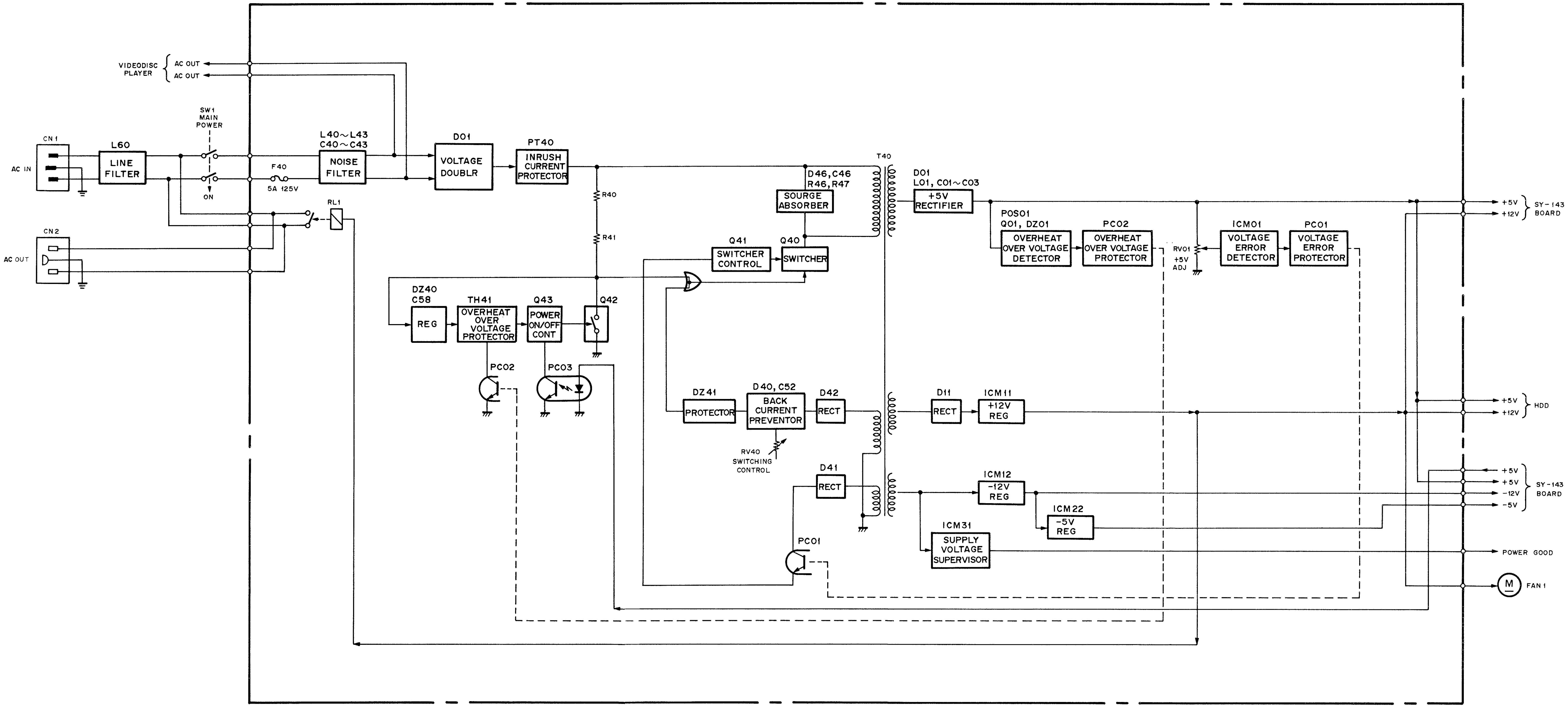
ADDRESSES 0B0000H to 0BFFFFH (128K BYTES)

IC101, 102
64K-BYTE BANK 1
IC103, 104
64K-BYTE BANK0
IC105,106
64K-BYTE BANK3
IC107, 108
64K-BYTE BANK2
A
D
WE RAS CAS OE
WE RAS CAS DE
8 9 2 5
0-7
8-15
101-B10 VMA0
101-A10 VMA 1
101-B9 VMA 2
101-A9 VMA 3
102-B11 VMA4
102-A11 VMA5
102-B10 VMA6
102-A10 VMA7
101-B5 WE1
101-B4 WE0
101-A5 RAS10
101-A3 OE10
102-B6 WE3
102-B5 WE2
102-A6 RAS32
101-A2 OE32
VMD15 102-B8
VMD14 102-B7
VMD13 102-A8
VMD12 102-A7
VMD11 102-B4
VMD10 102-A5
VMD9 102-A3
VMD8 102-A4
VMD7 101-B7
VMD6 101-B6
VMD5 101-A7
VMD4 101-A6
VMD3 101-B3
VMD2 101-A4
VMD1 101-B1
VMD0 101-A1
+5V
R101
IC109
1 2 3 4 5 6 7 9 10 11 12 13 14
102-B2 CAS32
102-A2 CAS10
RCAS32 102-B1
RCAS10 102-A1
102-B9 VMA8

CN101 IS CONECTED WITH CN301 OF SY-143 BOARD
CN102 IS CONECTED WITH CN302 OF SY-143 BOARD

RAM-13
SMI-5051

4-4. SWITCHING REG


VIDEODISC PLAYER
AC OUT
AC OUT
SW1 MAIN POWER
ON
CN1
AC IN
L60
LINE FILTER
CN2
AC OUT
F40
5A 125V
L40～L43
C40～C43
NOISE FILTER
RL1
D01
VOLTAGE DOUBLR
PT40
INRUSH CURRENT PROTECTOR
R40
R41
D46, C46
R46, R47
SOURGE ABSORBER
T40
Q41
SWITCHER CONTROL
Q40
SWITCHER
DZ40
C58
REG
TH41
OVERHEAT OVER VOLTAGE PROTECTOR
Q43
POWER ON/OFF CONT
Q42
PC02
PC03
DZ41
PROTECTOR
D40, C52
BACK CURRENT PREVENTOR
RV40
SWITCHING CONTROL
D42
RECT
D41
RECT
PC01
D01
L01, C01～C03
+5V RECTIFIER
POS01
Q01, DZ01
OVERHEAT OVER VOLTAGE DETECTOR
PC02
OVERHEAT OVER VOLTAGE PROTECTOR
RV01
+5V ADJ
ICM01
VOLTAGE ERROR DETECTOR
PC01
VOLTAGE ERROR PROTECTOR
D11
RECT
ICM11
+12V REG
ICM12
-12V REG
ICM22
-5V REG
ICM31
SUPPLY VOLTAGE SUPERVISOR
+5V
+12V
SY-143 BOARD
+5V
+12V
HDD
+5V
+5V
-12V
-5V
SY-143 BOARD
POWER GOOD
M
FAN1

SES-P/S UC
SWITCHING REG
1-413-426-11
VIW-5000 (UC)

VIW-5000 (UC)

9-972-805-82

Sony Corporation
Home Video Group

English
89H0910-1
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VIW-5000

SERVICE MANUAL

SUPPLEMENT-3

File this supplement with the service manual.

- This supplement-3 describes following items.

(1) 6-3. SELF-DIAGNOSTIC PERFORMED WITH THE INITIALIZATION.
(2) Videodisc player section of VIW-5000.

Sony VIEW System

SONY®

[SELF-DIAGNOSTIC PERFORMED WITH THE INITIALIZATION]

6-3. SELF-DIAGNOSTIC PERFORMED WITH THE INITIALIZATION

The following subsection discusses ROM initialization procedures. An explanation of POST tests and diagnostics follows. The boot message facilities are then discussed.

6-3-1. Power-On Self Tests

Power-on self tests (POST) are the system test and component initialization processes performed by AT-Compatible ROM. POST begins when system power is applied. It is followed by a system boot load, which loads an operating system into RAM. The self test and initialization functions of POST are tightly interwoven. The most central hardware is tested and initialized first.

Proper functioning of the central hardware is required before further system tests can be run.

6-3-2. System Board Failure

In general, a failure in a test of critical system-board circuitry or components resuits in sounding a beep code (if used) and in a halted system.

The Beep Codes for fatal and non-fatal system board errors are listed separately on the following page.

6-3-2-1. Fatal System Board Errors

Note: No beep code is sounded if a test is aborted while in progress. The contents of port 80h can be read to identify the area of failure.

Beep Code	Contents Port 80h	Description
none	01h	CPU register test in progress
1-1-3	02h	CMOS write/read failure
1-1-4	03h	ROM BIOS checksum failure
1-2-1	04h	Programmable interval timer failure
1-2-2	05h	DMA initialization failure
1-2-3	06h	DMA page register write/read failure
1-3-1	08h	RAM refresh verification failure
none	09h	First 64K RAM test in progress
1-3-3	0Ah	First 64K RAM chip or data line failure multi-bit
1-3-4	0Bh	First 64K RAM odd/even logic failure
1-4-1	0Ch	Address line failure first 64K RAM
1-4-2	0Dh	Parity failure first 64K RAM
2-1-1	10h	Bit 0 first 64K RAM failure
2-1-2	11h	Bit 1 first 64K RAM failure
2-1-3	12h	Bit 2 first 64K RAM failure
2-1-4	13h	Bit 3 first 64K RAM failure
2-2-1	14h	Bit 4 first 64K RAM failure
2-2-2	15h	Bit 5 first 64K RAM failure
2-2-3	16h	Bit 6 first 64K RAM failure
2-2-4	17h	Bit 7 first 64K RAM failure
2-3-1	18h	Bit 8 first 64K RAM failure
2-3-2	19h	Bit 9 first 64K RAM failure
2-3-3	1Ah	Bit A first 64K RAM failure
2-3-4	1Bh	Bit B first 64K RAM failure
2-4-1	1Ch	Bit C first 64K RAM failure
2-4-2	1Dh	Bit D first 64K RAM failure
2-4-3	1Eh	Bit E first 64K RAM failure

6-3-2-2. Fatal System Board Errors, cont'd

Beep Code	Contents Port 80h	Description
2-4-4	1Fh	Bit F first 64K RAM failure
3-1-1	20h	Slave DMA register failure
3-1-2	21h	Master DMA register failure
3-1-3	22h	Master interrupt mask register failure
3-1-4	23h	Slave interrupt mask register failure
none	25h	Interrupt vector loading in progress
3-2-4	27h	Keyboard controller test failure
none	28h	CMOS power failure and checksum calculation in progress
none	29h	CMOS configuration vaildation in progress
3-3-4	2Bh	Screen initialization failure
3-4-1	2Ch	Screen retrace test failure
3-4-2	2Dh	Search for video ROM in progress
none	2Eh	Screen running with video ROM
none	30h	Screen operable
none	30h	Screen runnig with video ROM
none	31h	Monochrome monitor operable
none	32h	Color monitor (40 column) operable
none	33h	Color monitor (80 column) operable

6-3-2-3. Non-Fatal System Board Errors

A failure in add-on boards or memory is reported on the monitor. These error-messages help isolate the failed subsystem.

The following table describes the beep codes and error codes that are written to Port 80h for non-fatal system board errors.

Message	Meaning
Hex-value Base Memory	The amount of base memory that tested successfully.
Hex-value Expanded Memory	The amount of expanded memory that tested successfully.
Hex-value Extra Memory	The amount of extra memory that tested successfully.
Hex-value Standard Memory	The amount of standard memory that tested successfully.
Decreasing available memory	This message immediately follows any memory error message. Informing you that failed memory chips means you have less memory available.
Memory Tests terminated by keystroke	You have pressed the spacebar while memory tests were runnig, stopping the memory tests.
Strike the F1 key to continue	An error was found during POST. Pressing the F1 key allows the system to boot.

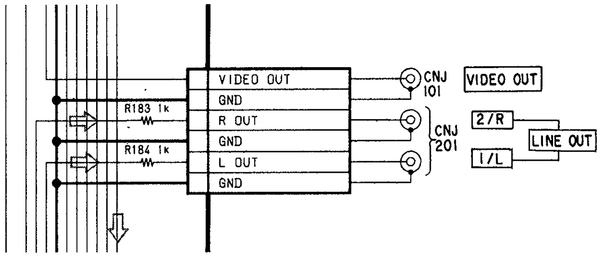
[VIDEO PLAYER SECTION OF VIW-5000]

Videodiac player section of VIW-5000 is almost same specification as that LDP-1200 (9-972-629-01). This service manual discribes the difference between videodisc player section of VIW-5000 and LDP-1200.

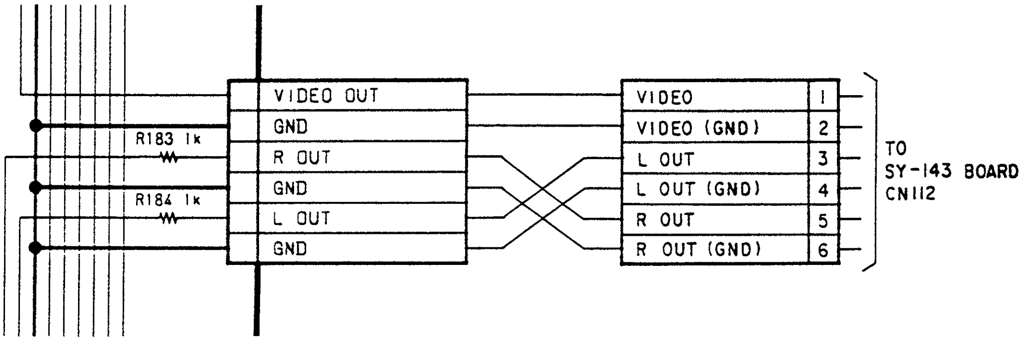
For repair, please read this manual with LDP-1200 service manual.

Ref. No.	Description	Videodisc player section of VIW-5000	LDP-1200 (9-972-629-01)	Refer to page of service manual (LDP-1200)
	MB-12 BOARD, COMPLETE	*A-6421-186-A	*A-6421-186-A	104
C771	ELECT 22MF 20% 25V	———	1-124-908-11	106
C772	ELECT 22MF 20% 25V	———	1-124-908-11	106
CNJ101	RECEPTACLE, BCN	———	1-562-635-11	107
CNJ201	JACK, PIN 2P	———	*1-562-999-21	107
R771	METAL GLAZE 220 5% 1/10W	———	1-216-033-00	113
R772	METAL GLAZE 1K 5% 1/10W	———	1-216-049-00	
R773	METAL GLAZE 1K 5% 1/10W	———	1-216-049-00	
R774	METAL GLAZE 220 5% 1/10W	———	1-216-033-00	
R (JW366)			———	
	SY-32 BOARD, COMPLETE	*A-6426-322-A	*A-6421-189-A	116
IC003	IC MC145406P	———	8-759-011-83	116
	FP-88 BOARD	*1-625-963-11	*1-625-963-11	117
D011	DIODE TLR113A	———	8-719-821-13	117
R011	CARBON 270 5% 1/4W	———	1-249-410-11	117
T901	TRANSFORMER, POWER	⚠1-449-152-11	⚠1-449-152-21	118

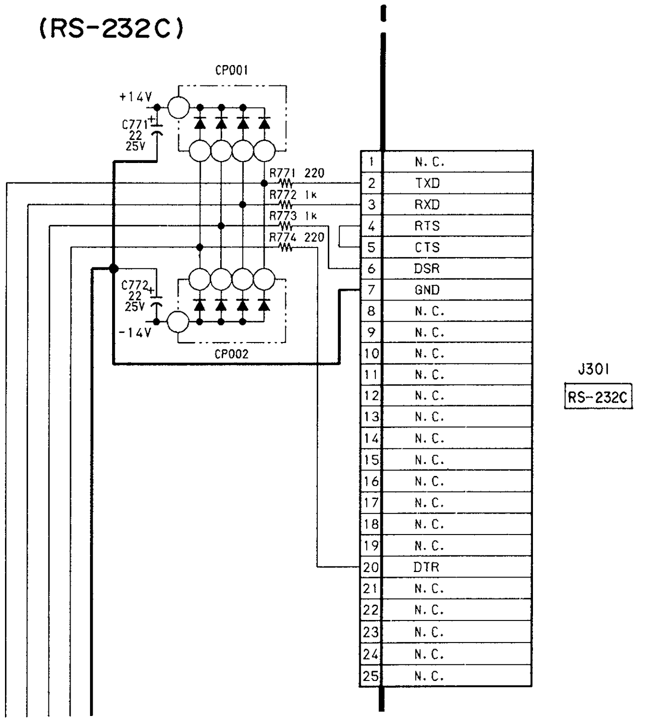
LDP-1200 (page 47): MB-12 SCHEMATIC DIAGRAM


VIDEO OUT
GND
R183 1k
R OUT
GND
R184 1k
L OUT
GND
CNJ 101
VIDEO OUT
CNJ 201
2/R
1/L
LINE OUT

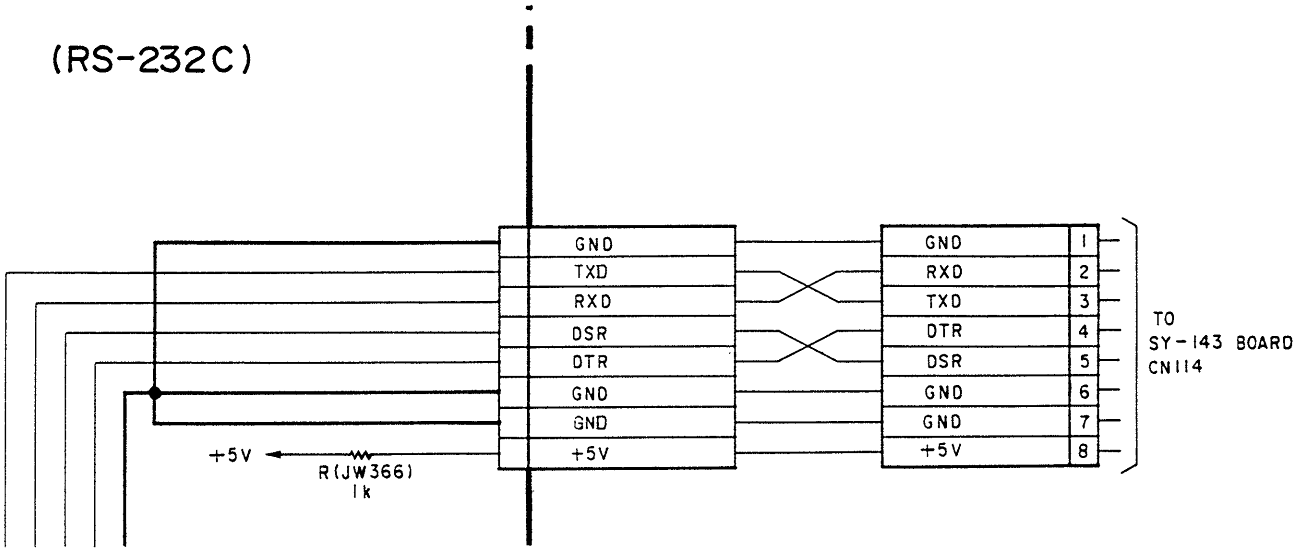
VIDEODISC PLAYER SECTION of VIW-5000: MB-12 SCHEMATIC DIAGRAM


VIDEO OUT
GND
R183 1k
R OUT
GND
R184 1k
L OUT
GND
VIDEO 1
VIDEO (GND) 2
L OUT 3
L OUT (GND) 4
R OUT 5
R OUT (GND) 6
TO SY-143 BOARD CN112

LDP-1200 (page 79): MB-12 SCHEMATIC DIAGRAM

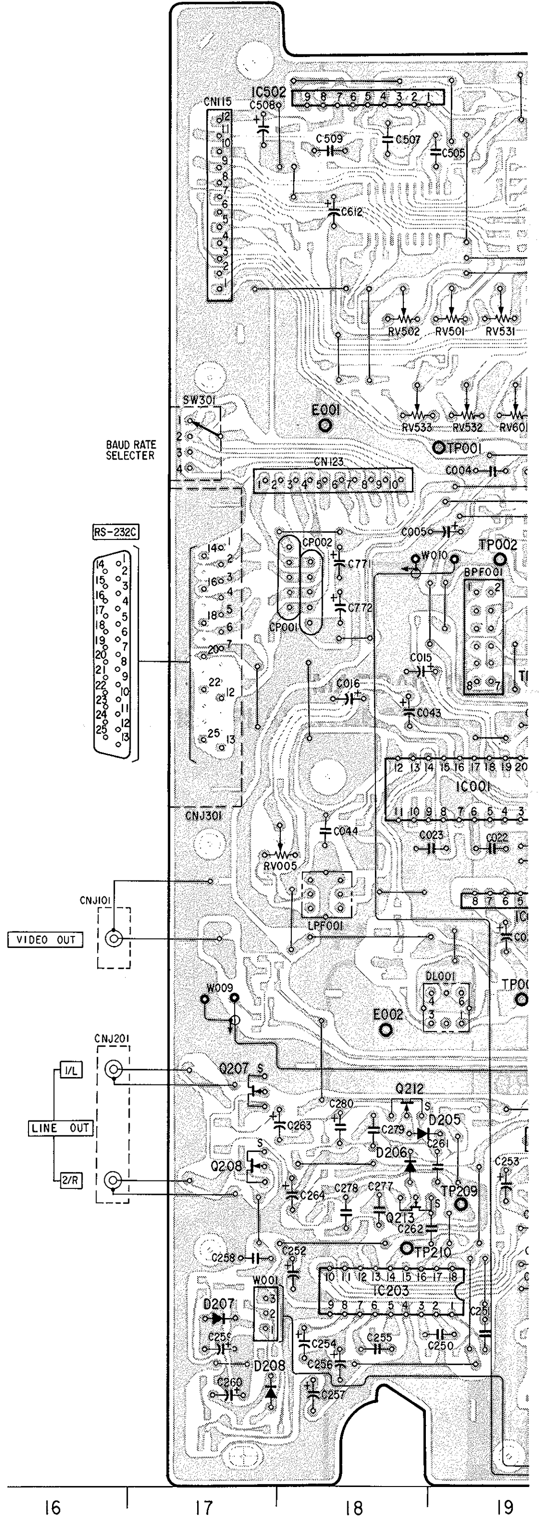

(RS-232C)
CP001
+14V
C771 22 25V
R771 220
R772 1k
R773 1k
R774 220
C772 22 25V
-14V
CP002
1 N.C.
2 TXD
3 RXD
4 RTS
5 CTS
6 DSR
7 GND
8 N.C.
9 N.C.
10 N.C.
11 N.C.
12 N.C.
13 N.C.
14 N.C.
15 N.C.
16 N.C.
17 N.C.
18 N.C.
19 N.C.
20 DTR
21 N.C.
22 N.C.
23 N.C.
24 N.C.
25 N.C.
J301
RS-232C

VIDEODISC PLAYER SECTION of VIW-5000: MB-12 SCHEMATIC DIAGRAM


(RS-232C)
GND
TXD
RXD
DSR
DTR
GND
GND
+5V
+5V
R(JW366) 1k
GND 1
RXD 2
TXD 3
DTR 4
DSR 5
GND 6
GND 7
+5V 8
TO SY-143 BOARD CN114

LDP-1200 (page 75): MB-12 PRINTED WIRING BOARD

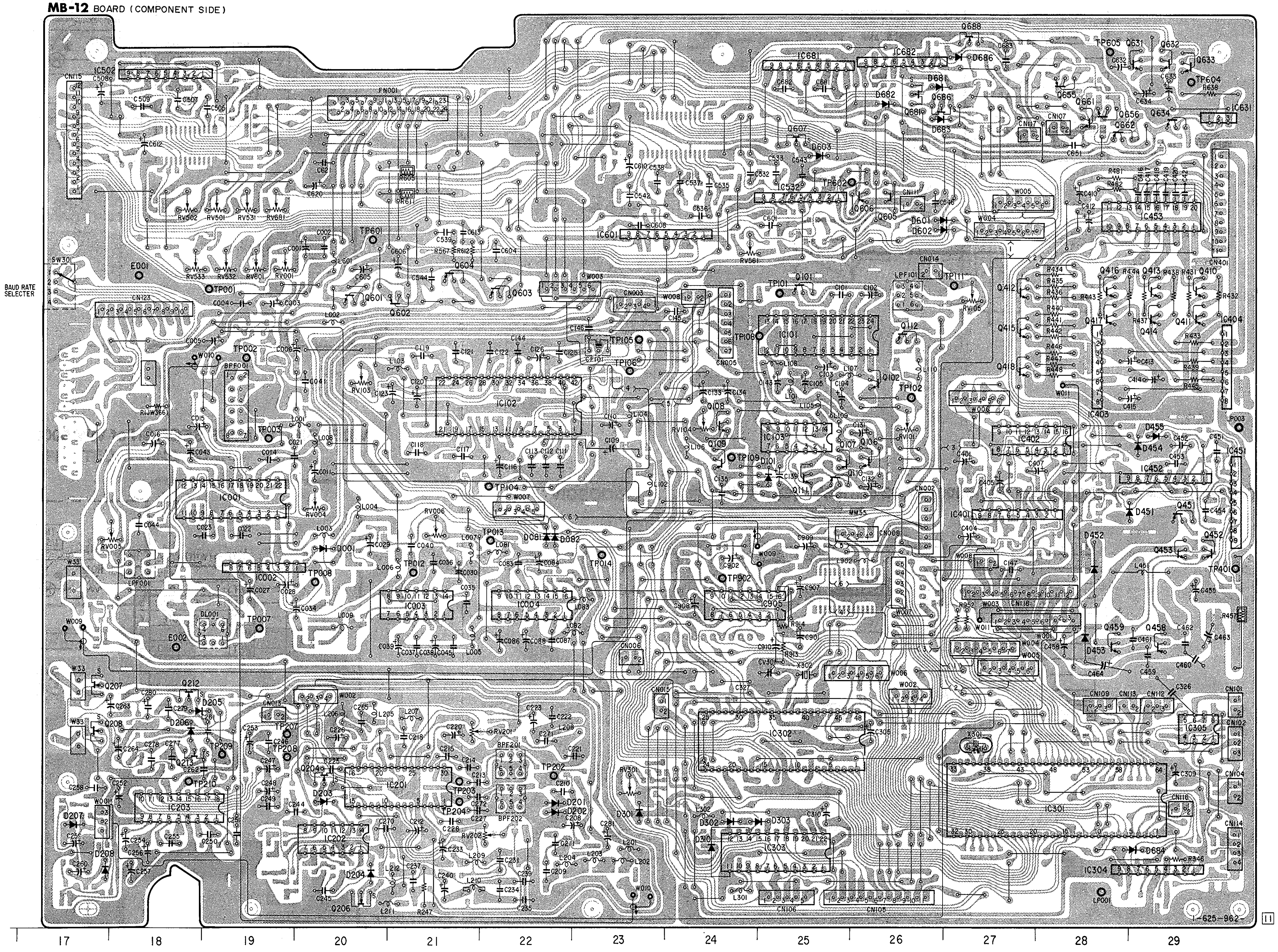
MB-12 BOARD (COMPONENT SIDE)


BAUD RATE SELECTER
RS-232C
VIDEO OUT
1/L
LINE OUT
2/R
16
17
18
19

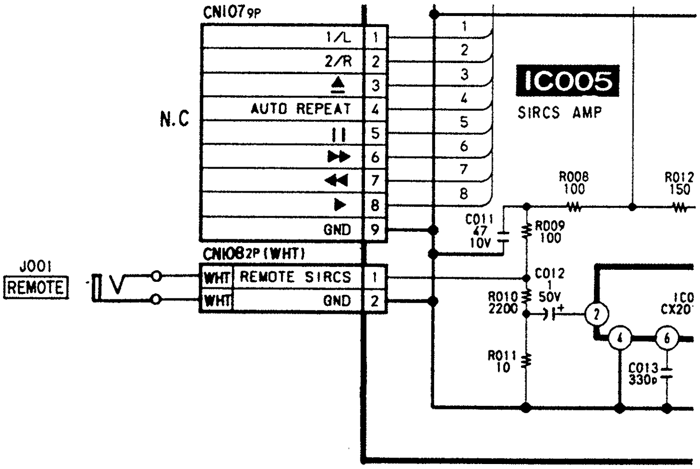
VIDEODISC PLAYER SECTION of VIW-5000: MB-12 PRINTED WIRING BOARD

(R771 to R774 have been removed for CONDUCTOR SIDE)

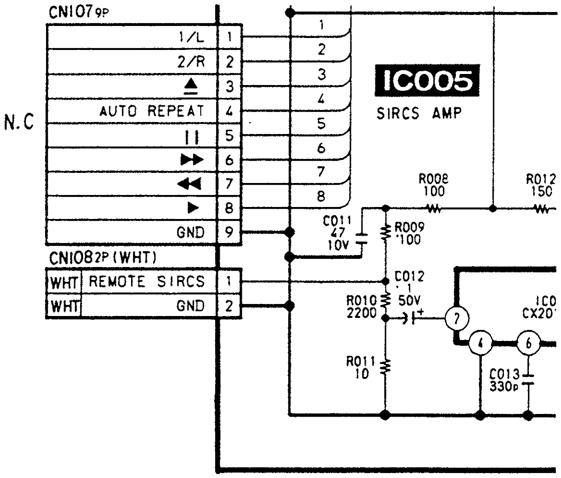
MB-12 BOARD (COMPONENT SIDE)


BAUD RATE SELECTER
1-625-962-11
17
18
19
20
21
22
23
24
25
26
27
28
29

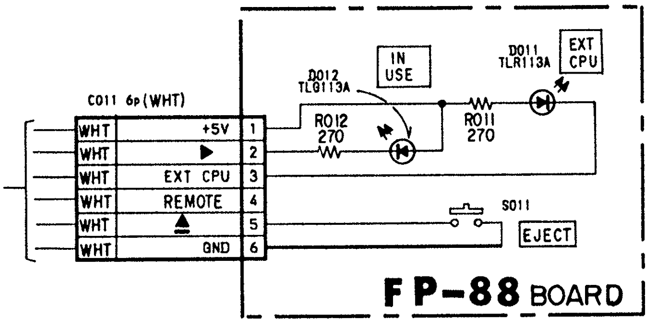
LDP-1200 (page 83): SY-32 SCHEMATIC DIAGRAM


CN107 9P
1/L
2/R
AUTO REPEAT
GND
N.C
CN108 2P (WHT)
WHT REMOTE SIRCS
WHT GND
J001
REMOTE
IC005
SIRCS AMP
R008 100
R012 150
C011 47 10V
R009 100
C012 1 50V
R010 2200
R011 10
C013 330p
ICO
CX20

VIDEODISC PLAYER SECTION of VIW-5000: SY-32 SCHEMATIC DIAGRAM

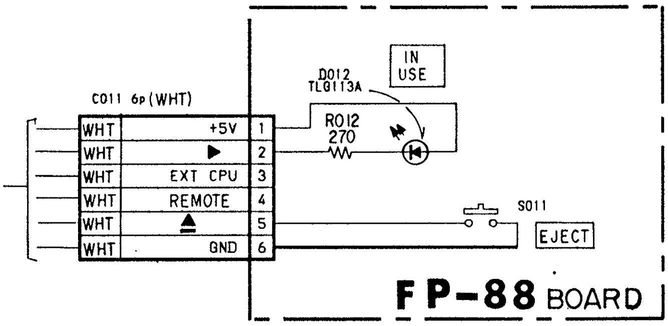

CN107 9P
1/L
2/R
AUTO REPEAT
GND
N.C
CN108 2P (WHT)
WHT REMOTE SIRCS
WHT GND
IC005
SIRCS AMP
R008 100
R012 150
C011 47 10V
R009 100
C012 1 50V
R010 2200
R011 10
C013 330p
ICO
CX20

LDP-1200 (page 83): FP-88 SCHEMATIC DIAGRAM



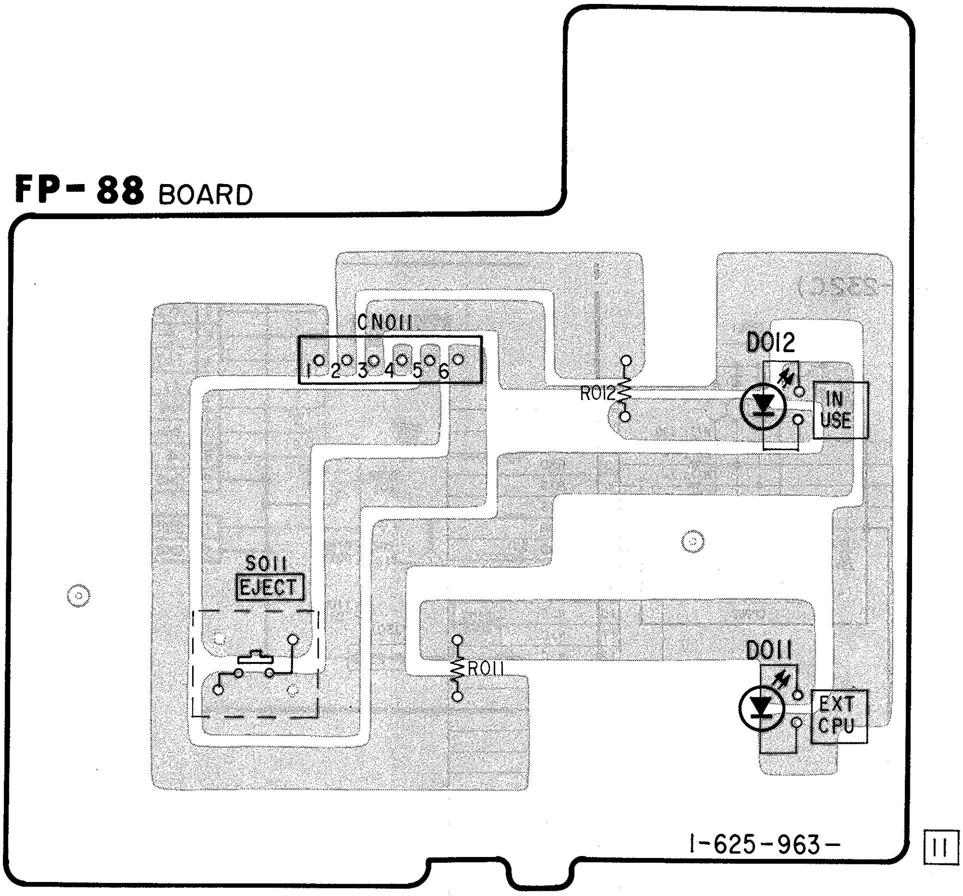
C011 6P (WHT)
WHT
+5V
▶
EXT CPU
REMOTE
GND
1
2
3
4
5
6
D012
TLG113A
IN USE
R012
270
D011
TLR113A
EXT CPU
R011
270
S011
EJECT
FP-88 BOARD

VIDEODISC PLAYER SECTION of VIW-5000: FP-88 SCHEMATIC DIAGRAM

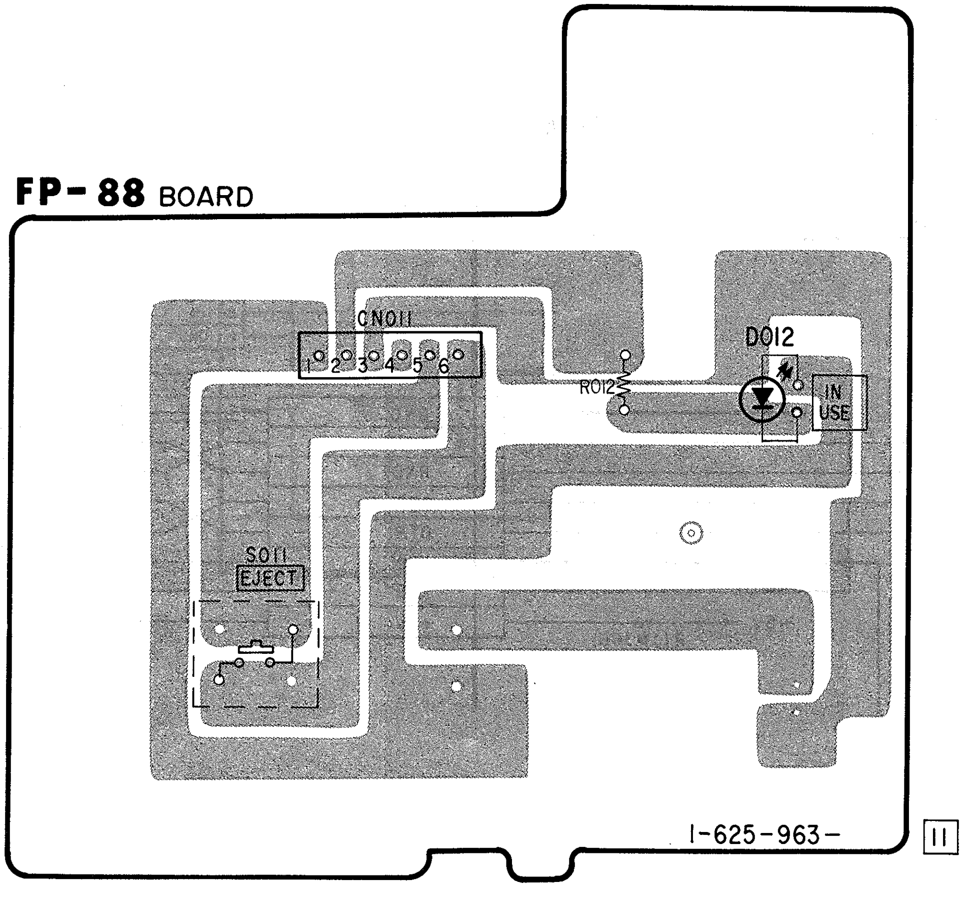


C011 6P (WHT)
WHT
+5V
▶
EXT CPU
REMOTE
GND
1
2
3
4
5
6
D012
TLG113A
IN USE
R012
270
S011
EJECT
FP-88 BOARD

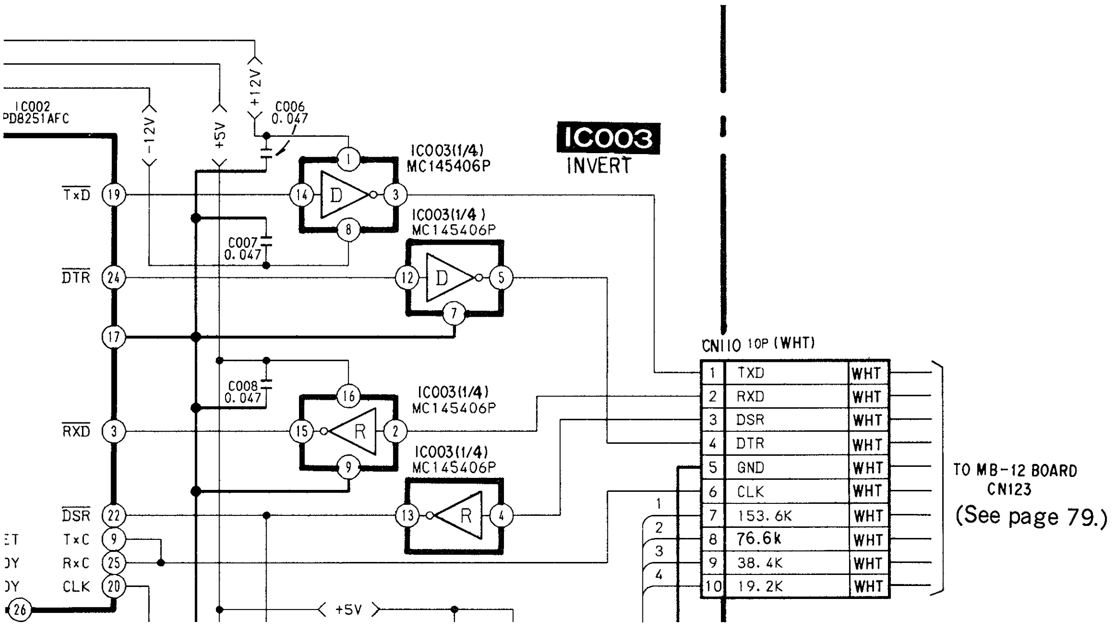
LDP-1200 (page 82): FP-88 PRINTED WIRING BOARD


FP-88 BOARD
CN011
1
2
3
4
5
6
D012
R012
IN USE
S011
EJECT
D011
R011
EXT CPU
1-625-963-
11

VIDEODISC PLAYER SECTION of VIW-5000: FP-88 PRINTED WIRING BOARD

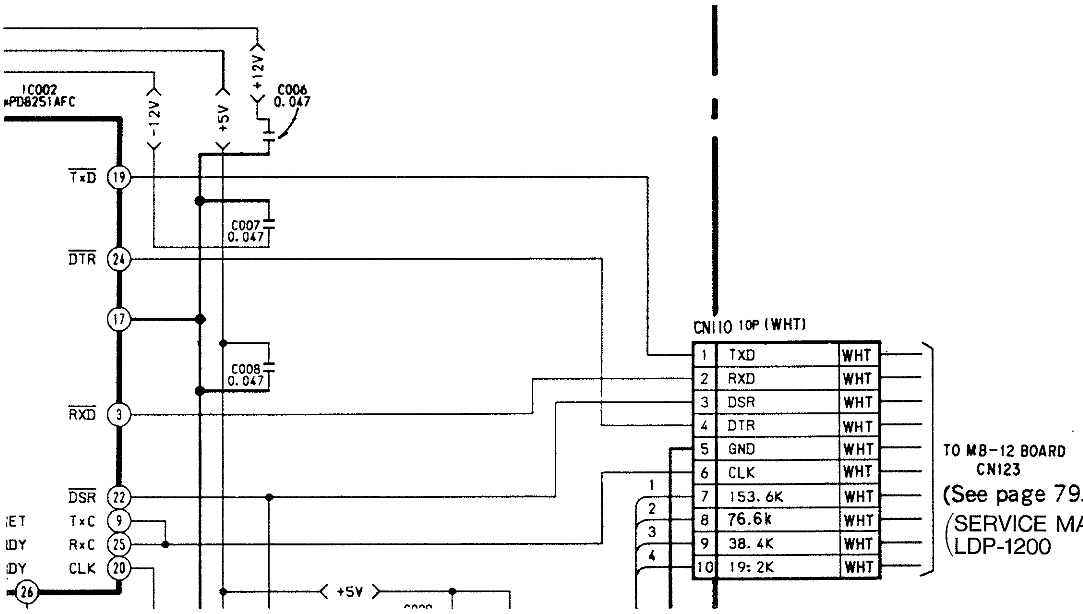

FP-88 BOARD
CN011
1
2
3
4
5
6
D012
R012
IN USE
S011
EJECT
1-625-963-
11

LDP-1200 (page 84): SY-32 SCHEMATIC DIAGRAM


IC002
PD8251AFC
-12V
+5V
+12V
C006
0.047
IC003(1/4)
MC145406P
IC003
INVERT
TxD
DTR
RXD
DSR
TxC
RxC
CLK
C007
0.047
C008
0.047
+5V
CN110 10P (WHT)
1 TXD WHT
2 RXD WHT
3 DSR WHT
4 DTR WHT
5 GND WHT
6 CLK WHT
7 153.6K WHT
8 76.6k WHT
9 38.4K WHT
10 19.2K WHT

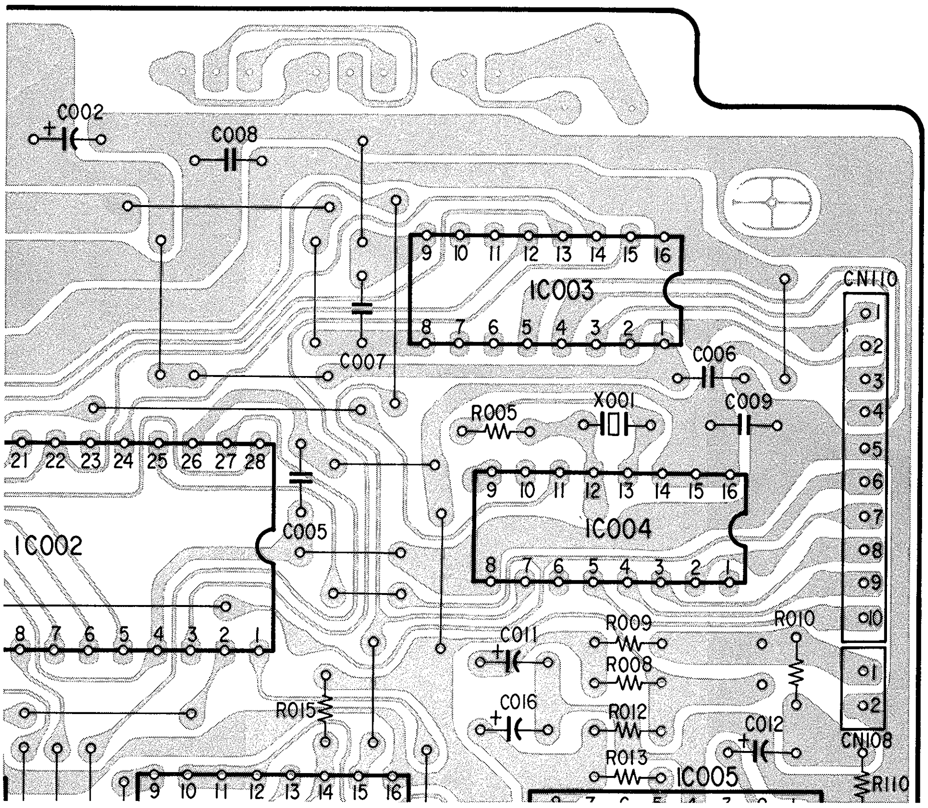
TO MB-12 BOARD
CN123
(See page 79.)

VIDEODISC PLAYER SECTION of VIW-5000: SY-32 SCHEMATIC DIAGRAM

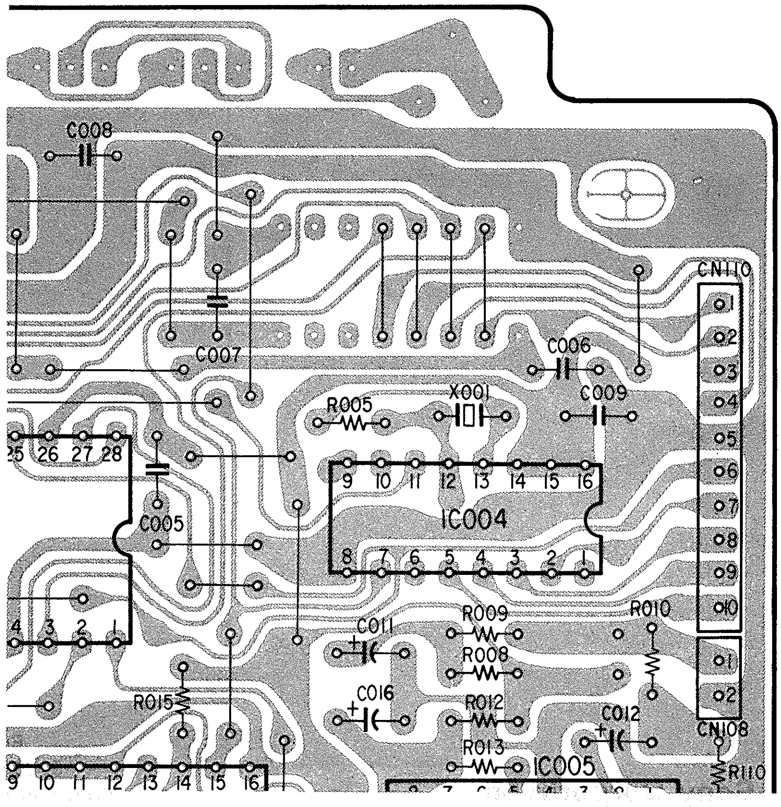

IC002
μPD8251AFC
-12V
+5V
+12V
C006
0.047
TxD
DTR
RXD
DSR
TxC
RxC
CLK
C007
0.047
C008
0.047
+5V
CN110 10P (WHT)
1 TXD WHT
2 RXD WHT
3 DSR WHT
4 DTR WHT
5 GND WHT
6 CLK WHT
7 153.6K WHT
8 76.6k WHT
9 38.4K WHT
10 19:2K WHT

TO MB-12 BOARD
CN123
(See page 79.)
(SERVICE MANUAL of
LDP-1200)

LDP-1200 (page 81): SY-32 PRINTED WIRING BOARD


C002
C008
IC003
CN110
C007
C006
X001
R005
C009
IC002
C005
IC004
C011
R009
R010
R008
C016
R015
R012
C012
CN108
R013
IC005
R110

VIDEODISC PLAYER SECTION of VIW-5000: SY-32 PRINTED WIRING BOARD


C008
CN110
C007
C006
R005
X001
C009
C005
IC004
C011
R009
R010
R008
C016
R015
R012
C012
CN108
R013
IC005
R110

VIW-5000(UC)
9-972-805-83

Sony Corporation
Home Video Group

English
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Published by Customer Relations and Service Group

VIW-5000

SONY®

SERVICE MANUAL

SUPPLEMENT-4

Subject:
ELECTRICAL PARTS LIST OF
REGULATOR BLOCK

File this supplement with the service manual. (9-972-805-11)

• ELECTRICAL PARTS LIST

NOTE:

- Due to standardization, replacements in the parts list may be different from the parts specified in the diagrams or the components used on the set.
- -XX and -X mean standardized parts, so they may have some difference from the original one.
- RESISTORS
  All resistors are in ohms.
  METAL:Metal-film resistor.
  METAL OXIDE: Metal oxide-film resistor.
  F:nonflammable
- Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
- SEMICONDUCTORS
  In each case, u:μ, for example:
  uA..: μA.. uPA..: μPA..
  uPB..: μPB.. uPC..: μPC.. uPD..: μPD..
- CAPACITORS
  uF: μF
- COILS
  uH: μH

When indicating parts by reference number, please include the board.

The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety.
Replace only with part number specified.

Les composants identifiés par une marque ⚠ sont critiques pour la sécurité.
Ne les remplacer que par une pièce portant le numéro spécifié.

Ref. No.	Part No.	Description			Remark
*	1-413-426-12	REGULATOR, SWITCHING *******************			
		< CAPACITOR >			
C01	1-126-624-11	ELECT (SMALL TYPE)	2700uF	20%	16V
C02	1-126-624-11	ELECT (SMALL TYPE)	2700uF	20%	16V
C03	1-126-624-11	ELECT (SMALL TYPE)	2700uF	20%	16V
C04	1-126-623-11	ELECT	1200uF	20%	10V
C05	1-126-163-11	ELECT	4.7uF	20%	50V
C06	1-124-791-11	ELECT	1uF	20%	50V
C11	1-126-145-11	ELECT (SMALL TYPE)	680uF	20%	35V
C12	1-126-336-11	ELECT	220uF	20%	25V
C21	1-126-142-11	ELECT (SMALL TYPE)	100uF	20%	35V
C22	1-126-375-11	ELECT	100uF	20%	25V
C23	1-126-375-11	ELECT	100uF	20%	25V
C32	1-126-163-11	ELECT	4.7uF	20%	50V
C33	1-126-163-11	ELECT	4.7uF	20%	50V
⚠C40	1-161-741-00	CERAMIC	1000PF	10%	400V
⚠C41	1-161-741-00	CERAMIC	1000PF	10%	400V
⚠C42	1-136-537-11	POLYESTER FILM	0.47uF	20%	250V
⚠C43	1-130-711-00	POLYESTER FILM	0.22uF	20%	250V
C46	1-136-207-11	METALIZED PE FILM	0.047uF	10%	630V
⚠C48	1-162-599-12	CERAMIC	4700PF	20%	400V
C49	1-130-495-00	POLYESTER FILM	0.1uF	10%	50V
C50	1-125-567-11	ELECT	390uF	20%	250V
C51	1-125-567-11	ELECT	390uF	20%	250V
C52	1-130-489-00	POLYESTER FILM	0.033uF	20%	250V
C53	1-130-493-00	POLYESTER FILM	0.068uF	10%	50V
C54	1-130-489-00	POLYESTER FILM	0.033uF	20%	250V
C55	1-130-475-00	POLYESTER FILM	0.0022uF	10%	50V
C56	1-130-479-00	POLYESTER FILM	0.0047uF	10%	50V
C57	1-130-493-00	POLYESTER FILM	0.068uF	10%	50V
C58	1-126-163-11	ELECT	4.7uF	20%	50V
⚠C80	1-164-292-11	CERAMIC	680PF	10%	3.15KV
C99	1-130-821-11	METALIZED PE FILM	0.15uF	10%	630V

Ref. No.	Part No.	Description	Remark
		< CONNECTOR >	
⚠CN1	1-540-088-11	AC INLET	
⚠CN2	1-540-079-11	AC OUTLET	
		< DIODE >	
D01	8-719-510-24	DIODE S15SC4M	
D11	8-719-510-25	DIODE D10LCA20	
D21	8-719-510-26	DIODE DINL20	
D40	8-719-901-92	DIODE V19C	
D41	8-719-949-29	DIODE 1S2075K	
D42	8-719-949-29	DIODE 1S2075K	
D46	8-719-510-23	DIODE DFG1A8	
DZ01	8-719-994-53	DIODE HZ5C3	
DZ40	8-719-994-62	DIODE HZ6B2	
DZ41	8-719-991-53	DIODE HZ5A3	
RF40	8-719-510-22	DIODE D3SB60	
		< FUSE >	
⚠F40	1-532-747-11	FUSE, GLASS TUBE 5A 125V	
		< FAN >	
FAN1	1-541-678-11	FAN	
		< COIL >	
L01	1-424-238-11	COIL, CHOKE 3.4uH	
⚠L40	1-424-239-11	COIL, CHOKE 72uH	
⚠L41	1-424-239-11	COIL, CHOKE 72uH	
⚠L42	1-424-237-11	COIL, CHOKE 7MMH	
⚠L43	1-424-237-11	COIL, CHOKE 7MMH	
⚠L60	1-543-637-11	DATA LINE CHOKE	
		< IC >	
M01	8-759-988-44	IC STR9012	
M11	8-749-990-12	IC UPC79M05H	

Ref. No.	Part No.	Description			Remark
M21	8-759-105-40	IC UPC79M12H			
M22	8-759-105-38	IC AN1431T			
M31	8-759-988-44	IC MB3771DIP			
		< PHOTO COUPLER >			
⚠PC01	8-719-510-21	PHOTO COUPLER PC111S			
⚠PC02	8-719-510-21	PHOTO COUPLER PC111S			
⚠PC03	8-719-510-21	PHOTO COUPLER PC111S			
		< THERMISTOR >			
POS1	1-808-738-11	THERMISTOR			
⚠PT40	1-808-737-11	POWER THERMISTOR			
⚠PT41	1-808-737-11	POWER THERMISTOR			
		< TRANSISTOR >			
Q01	8-729-922-82	TRANSISTOR 2SC458C			
Q40	8-729-922-81	TRANSISTOR 2SC4237			
Q41	8-729-265-52	TRANSISTOR 2SC2655-Y			
Q42	8-729-265-52	TRANSISTOR 2SC2655-Y			
Q43	8-729-922-82	TRANSISTOR 2SC458C			
TH41	8-729-101-31	TRANSISTOR N13T1			
		< RESISTOR >			
R01	1-247-690-11	CARBON	15	5%	1/4W
R02	1-247-698-11	CARBON	68	5%	1/4W
R03	1-247-711-11	CARBON	680	5%	1/4W
R04	1-247-707-11	CARBON	390	5%	1/4W
R05	1-247-705-11	CARBON	270	5%	1/4W
R07	1-216-472-00	METAL OXIDE FILM	39	5%	3W
R08	1-247-719-11	CARBON	3.3K	5%	1/4W
R09	1-247-707-11	CARBON	390	5%	1/4W
R11	1-247-713-11	CARBON	1K	5%	1/4W
R12	1-247-705-11	CARBON	270	5%	1/4W
R21	1-247-713-11	CARBON	1K	5%	1/4W
R22	1-247-704-11	CARBON	220	5%	1/4W
R35	1-247-725-11	CARBON	10K	5%	1/4W
R40	1-216-492-11	METAL OXIDE FILM	82K	5%	3W
R41	1-216-492-11	METAL OXIDE FILM	82K	5%	3W
R42	1-247-721-11	CARBON	4.7K	5%	1/4W
⚠R43-1	1-219-111-11	WIREWOUND	0.56		5W
⚠R43-2	1-219-111-11	WIREWOUND	0.56		5W
R44	1-217-151-00	METAL PLATE	0.22		2W
R46	1-215-928-11	METAL OXIDE FILM	68K	5%	3W
R47	1-215-928-11	METAL OXIDE FILM	68K	5%	3W
R48	1-215-909-11	METAL OXIDE FILM	47	5%	3W
R49	1-215-909-11	METAL OXIDE FILM	47	5%	3W
R51	1-247-712-11	CARBON	820	5%	1/4W
R52	1-247-725-11	CARBON	10K	5%	1/4W
R53	1-247-704-11	CARBON	220	5%	1/4W
R54	1-247-719-11	CARBON	3.3K	5%	1/4W
R55	1-247-706-11	CARBON	330	5%	1/4W
R56	1-247-712-11	CARBON	820	5%	1/4W
R57	1-247-697-11	CARBON	56	5%	1/4W
R58	1-247-712-11	CARBON	820	5%	1/4W
⚠R60	1-259-886-11	CARBON	220K	5%	1W
R61	1-247-717-11	CARBON	2.2K	5%	1/4W
R80	1-215-912-11	METAL OXIDE FILM	150	5%	3W
R81	1-215-912-11	METAL OXIDE FILM	150	5%	3W
		< RELAY >			
⚠RL1	1-515-739-12	RELAY, POWER			
		< VARIABLE RESISTOR >			
RV01	1-237-514-21	ADJ, CARBON 500			
RV40	1-237-515-21	ADJ, CARBON 1K			
		< SPARK KILLER >			
⚠SQ40	1-136-908-11	SPARK KILLER	0.033uF	20%	250V
		< SWITCH >			
⚠SW1	1-571-947-11	POWER SWITCH			
		< TRANSFORMER >			
⚠T40	1-449-684-11	TRANSFORMER, SWITCHING			

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